ORGANIC METAL-SEMICONDUCTOR FIELD-EFFECT TRANSISTOR (OMESFET)

by

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Abstract

Organic electronics offers the possibility of producing ultra-low-cost and large-area electronics using printing methods. Two challenges limiting the utility of printed electronic circuits are the high operating voltage and the relatively poor performance of printed transistors. It is shown that voltages can be reduced by replacing the capacitive gate used in Organic Field- Effect Transistors (OFETs) with a Schottky contact, creating a thin-film Organic Metal-Semiconductor Field-Effect Transistor (OMESFET). This geometry solves the voltage issue, and promises to be useful in situations where low voltage operation is important, but good performance is not essential. In cases where high voltage is acceptable or required, it is shown that OFET performance can be greatly improved by employing a Schottky contact as a second gate.

The relatively thick insulating layer between the gate and the semiconductor in OFETs makes it necessary to employ a large change of gate voltage (~40 V) to control the drain current. In order to reduce the voltage to less than 5 V a very thin (<10 nm) insulating layer and/or high-k dielectric materials can be used, but these solutions are not compatible with current printing technology. Simulations and implementations of OMESFET devices demonstrate low voltage operation (<5 V) and improved sub-threshold swing compared to the OFET. However, these benefits are achieved at the expense of mobility.

In order to achieve good performance in an OFET, including threshold voltage, current ratio and output resistance, the semiconductor thickness has to be less than 50 nm, whereas the thickness of a printed semiconductor is typically larger than 200 nm. The addition of a top Schottky contact on the OFET creates a depletion region thereby reducing the effective thickness of the semiconductor, and resulting in enhanced transistor performance. Simulations and experimental results show improvements in the threshold voltage, the current ratio, and the output resistance of a dual gate transistor, when compared to those in an OFET of the same thickness.

The transistors introduced in this work demonstrate means of improving the performance of thick-film OFETs and of achieving substantially lower operation voltage in organic transistors.

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Abbreviation list

AFM -- atomic force microscope

AMD -- Active Matrix Displays

a-Si:H -- hydrogenated amorphous silicon

DI --Deionized (DI water = Deionized water)

DOS -- Density of States

FET -- Field Effect Transistor

GPIB -- General Purpose Interface Bus

HOMO -- Highest Occupied Molecular Orbital

IC -- Integrated Circuit

IGFET -- Isolated Gate Field Effect Transistor

LCD -- Liquid Crystal Displays

LUMO -- Lowest Unoccupied Molecular Orbital

MESFET -- Metal Semiconductor Field Effect Transistor

MIS -- Metal- Insulator-Semiconductor

MOS -- Metal Oxide Semiconductor

MOSFET -- Metal Oxide Semiconductor Field Effect Transistor

MS -- Metal-Semiconductor

MTR – Multiple Trapping and Release

OBD -- Organic Bistable Device

OFET -- Organic Field Effect Transistor

OLED -- Organic Light Emitting Diode

OMESFET -- Organic Metal Semiconductor Field Effect Transistor

PEDOT-PSS -- Poly(3,4-ethylenedioxythiophene) - Polystyrene Sulfonate

RFID -- Radio Frequency Identification

rr-P3HT – Regioregular poly(3-hexylthiophene)

SCLC -- Space Charge Limited Current

TC-AAM -- Trapped Charge Advanced Application Module

TFT -- Thin-film Transistor

VLSI -- Very Large Scale Integrated circuits

VRH – Variable Range Hopping

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Chapter 1

Introduction

Despite the widespread use of crystalline silicon to fabricate electronic devices, for some applications the market is demanding ultra low-cost, large-area and flexible electronics for which silicon is not a good choice. Therefore in the last few decades extensive research has been done on various materials to find an appropriate alternative semiconductor for such applications. Organic semiconductors are promising materials because of a few special properties. Mechanical flexibility of organics is an important feature for some future products such as roll-able displays [1] and wearable electronics [2, 3]. Also, low capital cost methods of depositing organics such as printing and casting should enable production of electronics at ultra-low cost and/or over very large areas (much larger than silicon wafers). These production methods make organic electronics good candidates for producing very cheap radio frequency identification (RFID) tags (as an alternative to the bar code tags) and very large-area displays. Indeed large-screen organic displays and organic RFIDs have planned product-launch dates in 2007 [4-6]. The chemical and electrical tuneabilities of organics allow the design of various chemical sensors and optical devices such as electronic noses [7] and organic light emitting diodes (OLEDs) [8]. Such interesting properties of organic semiconductors have attracted a lot of attention all around the world. As a result the organic electronics industry has had very rapid growth in the last decade [9], and its market is expected to increase from $1.4 billion in 2007 to $19.7 billion in 2012, which is about a 70% annual growth [10]. There are some challenges preventing widespread adoption of organic electronics, and in particular it is difficult to attain reasonable performance using low cost methods.

Transistors as the building blocks of any electronic circuit are the main concern in developing organic electronics. The thin-film transistor (TFT) structure is extensively used to build organic transistors which are known as organic field-effect transistors (OFETs). Although recent research results have shown a lot of progress in demonstrating effective prototype OFETs [11], most of these are produced using expensive methods similar to those used in the amorphous silicon technology.

Mobility of carriers, current ratio between on and off states, and the operational voltage range are important parameters in organic transistors. These properties can all be adversely affected by the use of printing methods. In order to apply a printing method such as inkjet printing, screen printing or microcontact printing a soluble organic semiconductor has to be used as the ink. Spin coated soluble organics have shown mobilities as high as 0.1 $cm^2/V{\cdot}s$ [12]. The application of printing methods rather than spin coating reduces the mobility to less than 0.02 $cm^2/V{\cdot}s$ [13-15]. Also, the current ratio in printed OFETs is usually much lower than that in the OFETs fabricated with other methods [15, 16]. The reason is that a very thin semiconductor layer (<50 nm) is required for high current ratio (10^5), whereas printed layers are typically a few hundred nanometres thick. This results in current ratios of less than 10^3 [13, 15, 16].

The thickness of the semiconductor layer is limited not only by the deposition method but also by the roughness of the substrate. To deposit a layer thinner than 50 nm the substrate surface has to be smooth enough to obtain an electrically continuous film. Such a limitation makes it a challenge to fabricate OFETs on low cost flexible substrates and fabrics.

The use of a high voltage (~40 V) is very common to drive OFETs [17], whereas low voltage operation is preferred because of the lower power consumption and ease of use with batteries. To reduce the voltage range to about 5 V the insulating layer between the semiconductor and the gate electrode has to be very thin (a few tens of nanometres), which again is a challenge in printing methods. The use of high dielectric materials has been suggested to reduce the voltage needed for a given thickness of insulating layer [18], but so far the deposition of such materials with printing techniques has not been effective.

The need for relatively thin layers in order to obtain good performance in OFETs has meant that relatively expensive deposition methods such as evaporation are preferred because these offer more control over the thickness and quality of deposited layers. Amorphous silicon transistors use similar deposition techniques and currently have better performance at lower prices than organic devices. Hence the focus must be on lower cost fabrication methods such as printing if widespread use of organics is to be achieved [11].

Two types of transistors are suggested in this thesis that can show good performance when the semiconductor layer is relatively thick: the organic metal-semiconductor field-effect transistor (OMESFET) and dual gate organic transistor. OMESFET is a low voltage thick-film transistor.

The direct contact between the gate and the semiconductor in a OMESFET creates a depletion region controlled by a relatively low voltage. Organic MESFETs had previously been reported in two scientific papers [19, 20]. The first report was in 1991. The current ratio was ~ 5 and the mobility was ~10^{-3} $cm^2/V{\cdot}s$ [19]. In 2001 an OMESFET was shown to operate as a phototransistor [20]. Based on these reports it was clear that low voltage operation is possible in relatively thick structures. What was not clear was whether reasonable performance could be obtained. In this thesis the aim is to study OMESFETs as alternative to OFETs in cases where operational voltage range and semiconductor thickness are limiting parameters. A voltage range of 5 V or less is the target. A 200 nm layer thickness is taken to be an appropriate minimum thickness which is achievable with a low-cost printing method, based on literature reports [13, 21].

A second approach, the dual gate organic transistor, is devised for thick-film semiconductors. The new device is an OFET in which the effective thickness of semiconductor is controlled by a secondary gate. This secondary gate is a Schottky contact which is intended to produce a depletion region, reducing the source-drain leakage in the off state. For a thick-film semiconductor (> 200 nm) in which the current ratio in the OFET is usually low (< 1000) [13, 16], the second gate is implemented in order to enhance the current ratio and also to tune the transistor parameters [22]. This design does not improve the voltage range of the OFET, but is otherwise expected to show better performance than the OFET, because of the thinner effective semiconductor layer.

An essential part of both OMESFETs and dual gate organic transistors is the Schottky contact between a metal and an organic semiconductor. This junction is studied through theory and experiments described in chapter 4. In chapter 5 the structure and operation of the OFET and the OMESFET are explained. Also, the OMESFET characteristics are compared with those in an OFET through simulation and experiment. The effect of the semiconductor thickness on OFET characteristics are studied by analytical modeling and simulation in chapter 6. The structure of the dual gate organic transistor is then explained and its characteristics are compared with those of a thick film OFET through simulation and experiment. The basics of the organic semiconductors and the charge transport mechanism in non-crystalline semiconductors are reviewed in chapter 2. The CAD tool used for the simulation and the microfabrication process used for electrode fabrication are explained in chapter 3.

The structure of this thesis is somewhat unusual in that the background theory relevant to each device (diode, MESFET and OMESFET) is discussed at the beginning of the chapters presenting the results from these devices rather than being included in a single chapter near the beginning of the thesis. Included in this discussion is a review of models that apply to crystalline semiconductors followed by a discussion of whether or not these concepts are applicable to describe organic devices. In some cases models not previously used in organic semiconductors are suggested.

Simulations are also presented in each device-related chapter. These simulations were performed in order to guide and motivate device fabrication. The devices that were subsequently fabricated used a polymer that had a much higher level of (unintentional) doping. As a result the effective mobilities, conductances and transconductances in transistors were much higher than those predicted in the model.

Chapter 2

Organic Semiconductors

Energy band theory is a common model applied to crystalline semiconductors to explain electrical properties, including the carrier concentration and the mobility. Also, the model is extensively used to explain the behaviour of various devices. The band structure in crystalline semiconductors results from very strong covalent bonds between atoms in the lattice, which keep the interatomic spacing short enough to produce wide conduction and valence bands. In addition, the periodic structure of a crystal produces sharp band edges with a negligible density of states in the band gap. In contrast, most organic molecules are bonded with weak intermolecular forces and have relatively poor periodicity. Therefore, the energy structure in organics is different from that in a crystalline semiconductor, which affects charge transport in the organics. To study and design organic electronic devices these differences should be considered.

In this chapter, the conduction mechanisms in organic molecules and in bulk organic semiconductors are briefly described. Conducting polymers and short organic molecules are then introduced as two choices from which to build organic devices. The energy structure of organic semiconductors is then presented, followed by a review of different models of charge transport mechanisms in organics. A charge transport model is selected from amongst these that is readily applied to the simulation of organic devices. The key concepts in this chapter that are used repeatedly in later chapters are: (1) soluble conjugated polymers are preferred over small organic molecules due to the ease of deposition for low-cost applications, (2) application of a deposition method compatible to the reel-to-reel process such as printing or casting has relatively poor control on the thickness of the deposited film, (3) the large density of localized states and the very narrow energy bands affect the charge transport in organics and as a result the classical semiconductor equations are not necessarily applicable in organics (4) the effective mobility is highly dependent on the position of the Fermi level (figure 2.8) and (5) the multiple trapping and release model (MTR) (equation 2.9) provides a reasonable description of the effective mobility of carriers as a function of density of states (at fixed temperature).

2.1 Introduction

Carbon-based polymers were known as insulting materials for a long time, and we still use them widely to insulate cables and wires. Polymers were almost universally considered insulators until 1977, when a conductivity of 10^5 S/m was reported for polyacetylene [23]. Such a conductivity is only 1000 times lower than that observed in copper and it is more than 13 orders of magnitude larger than the conductivity of reasonable insulators [23].

Although polyacetylene has shown nearly metallic properties when it is highly doped, its energy structure resembles that of a semiconductor, showing a relatively large band gap in the undoped state. Indeed, the semiconducting properties of organics were reported on as far back as the early 1980s when a Schottky diode was built from a lightly doped polyacetylene film [24].

The poor chemical stability of polyacetylene in the presence of oxygen has been the major obstacle to practical applications of this polymer. Instead, many other more stable polymers are now synthesized. These polymers form a class known as intrinsically conducting polymers. Also discussed in this chapter are short versions of these polymers that contain only a small number of repeating units. The focus of this thesis however is on polymers, and in particular poly(3-hexylthiophene), due to compatibility with printing methods.

2.2 Conduction mechanism in polyacetylene

As a requirement for electrical conduction, a solid needs to have delocalized electrons. The molecular structure of polyacetylene is shown in figure 2.1. In polyacetylene each carbon atom exhibits sp^2 hybridization to form three σ bonds with two carbon atoms and one hydrogen atom. One of the p-orbitals in each carbon is not hybridized and it is making a π bond with one of the adjacent carbon atoms, which appears as a double bond between two carbon atoms. The alternating single-double bond structure in polyacetylene is referred to as being conjugated. Any polymer with a conjugated structure in its backbone is called a conjugated polymer. Conducting polymers have conjugated double bond structures.

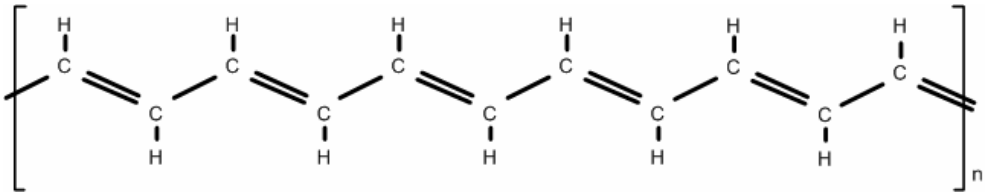


Figure 2.1. The chemical structure of polyacetylene.

In figure 2.2.a and b two forms of polyacetylene are shown and these are degenerate. Therefore, one can assume that instead of the conjugated double bonds there is a uniform distribution of electrons all along the polymer backbone (figure 2.2.c), which results in delocalized electrons in the polymer and it can explain the conductivity in polyacetylene. Although this explanation seems satisfactory, it is inconsistent with the instability of one-dimensional metals introduced by Peierls [25]. According to the Peierls distortion theory the spacing between carbon atoms in polyacetylene is alternately short and long to achieve an energetically stable structure [25]. Indeed the C=C bond is shorter than C-C, which means that the real structure of polyacetylene is closer to one shown in either figure 2.2.a or b as opposed to 2.2.c.

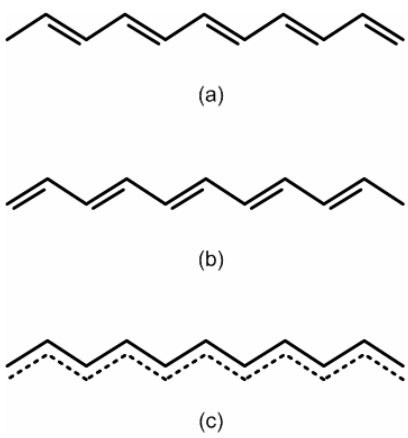


Figure 2.2. (a) (b) Degenerate forms of polyacetylene. (c) Delocalized electrons all along the polyacetylene back bone instead of the conjugated double bonds.

As a result of the Peierls distortion, a band gap is produced in the energy structure of polyacetylene leading to semiconducting behaviour. The value of the band gap is determined by the energy difference between the pi bonding states (π) and the pi anti-bonding states (π^*) in the molecular orbital. In such a case the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) resemble the edges of valence and conduction bands respectively in a crystalline semiconductor.

2.3 Dopants in organic semiconductors

Similar to the intrinsic semiconductors, an organic semiconductor has a few thermally excited carriers in its natural state, which result in very low conductivity. The conductivity in a conducting polymer is increased by producing more carriers. These carriers can either be induced by an external field or be generated by changing the oxidation states of the polymer [26]. The former is used in organic field-effect transistors, in which the surface conductivity of an organic film is controlled by an electric field produced from the gate terminal. The second approach is achieved by doping the polymer. Dopants in polymers are mostly in the form of ions. For example adding iodine to polyacetylene as an oxidizing agent dopes the polymer by removing an electron from polyacetylene and converting iodine to I_3^- (figure 2.3). Adding a dopant produces a state (polaron state) in which the generated carrier resides.

Oxygen and water molecules can cause unintentional doping in most conducting polymers. These dopants can increase the carrier density in the organic either by an oxidation process or by the field effect. The former case is similar to the iodine doping process in polyacetylene, , and as in the iodine case, reversing the doping involves a chemical reaction (reduction). In the later case the strong electron-electron repulsion from lone pair electrons in an oxygen atom (either in O_2 or H_2O) produces a hole in an organic semiconductor if the oxygen is very close to the polymer. In this case removing oxygen and water molecules by applying a high vacuum can undope the organic semiconductor [27].

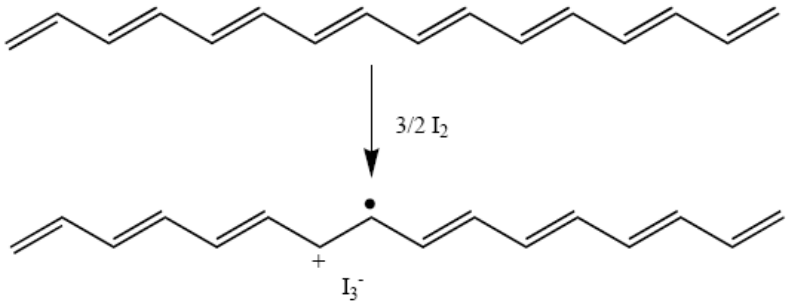


Figure 2.3. Generation of a hole in polyacetylene by oxidizing the polymer. The iodine acts as a dopant for the polymer.

2.4 Conduction in bulk semiconductor

Although the carriers are mobile along the backbone of a conjugated polymer, in order to observe a reasonable conductivity in a bulk material the carriers should be able to move between molecules easily. This generally happens either by hopping electrons from one molecule to another (described below) or by the overlap of p-orbitals of adjacent molecules.

The experimental results suggest that the hopping rate increases with the length of the polymer chain [28] because it is more likely to find a low enough barrier somewhere between two long polymer molecules than it is in two short ones. Also the hopping rate increases with dopant concentration [25].

The overlap of p-orbitals, known as π-π stacking, is another way to transfer charges between molecules. In this case the charge is delocalized both along the conjugated backbone and between molecules which have π-π stacking. As a result, a two dimensional charge transport is produced. If many of the molecules can be stacked on top of each other, they can form a domain (grain) with a high mobility. Then the mobility is limited by the barrier between domains rather than by intermolecular mobility [29]. To achieve a high mobility in a film of the material the molecules have to be well stacked. To do so, a relatively short conjugated molecule with a flat structure is preferred over a long polymer molecule. A controllable deposition process has to be applied in order to produce a well-ordered molecular film. In fact, the sublimation of some small molecules have shown a single crystal structure with a mobility only one order of magnitude lower than that in silicon [30].

There are thus two approaches to maximizing mobility in organic semiconductors. One is to use long molecules, relying on the in-chain conductivity and the eventual charge transfer due to the length of the molecule and dopants. The second is to maximize the degree of order, thereby increasing π stacking between molecules, which is most easily done by using short molecules that can be deposited under highly controlled conditions. There are two corresponding types of organic semiconductors: conducting polymers and small organic molecules. Each type has its own advantages that are preferred in some specific applications. In the next section each type is briefly introduced and the factors influencing the mobility in a few of the most promising semiconductors for organic electronics are mentioned.

2.5 Organic semiconductors

Two materials dominate the literature on organic transistors: regioregular poly(3-hexylthiophene) (rr-P3HT) and pentacene. The first is a polymer and the second is a small molecule. The properties and practicalities of use of these materials are now briefly reviewed.

2.5.1 Conducting polymers: rr-P3HT

A number of conducting polymers have been employed in organic electronics including polypyrrole, polyaniline and polythiophene. Polythiophene (figure 2.4.a) is a chemically stable conducting polymer, which is widely used in organic electronic devices, and probably the most widely used polymer in transistors. The discussion that follows focuses on polythiophene and its derivative poly(3-hexylthiophene).

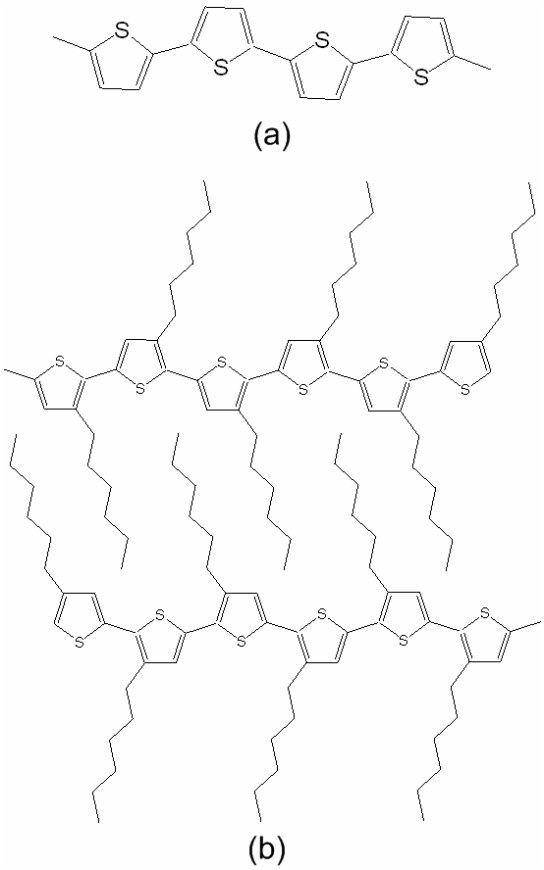


Figure 2.4. (a) Chemical structure of polythiophene (b) rr-P3HT with an interdigitated molecular structure.

Polythiophene is an insoluble polymer, but adding hexyl groups as the side chains to the thiophene rings makes the polymer soluble in chloroform and a few other organic solvents [31]. The new polymer is called poly(3-hexylthiophene) (P3HT). If the side chains are regularly arranged head-to-tail all along the chain, the polymer is called regioregular P3HT (rr-P3HT) (figure 2.4.b), whereas a random head-to-head or tail-to-tail produces a regiorandom P3HT. Although both polymers are soluble, the regioregular is preferred over the regiorandom because rr-P3HT has a flat structure and the interaction between the side chains produces an interdigitated molecular structure [12]. The interdigitated molecules produce planar sheets that can stack together to allow effective π-π stacking between molecules. As a result a crystalline structure can be achieved with a relatively high mobility [32].

Sirringhaus and his co-workers found that highly regioregular polymers can produce crystal grains as large as 130 Å [33]. Surprisingly, such a molecular order can be achieved using spin coating [33]. The availability of simple deposition methods that nevertheless produce good electrical properties is critical for achieving low-cost organic electronics. The molecular order is observed only in a thin film of rr-P3HT when silicon dioxide is used as the substrate [33]. In the upper layers, the polymer has a more amorphous structure. Indeed, the interaction between SiO_2 and the polymer arranges the molecules on the surface, greatly increasing order. In addition to the substrate the solvent has an important role in the structure of the deposited film [31]. Application of a low boiling point solvent causes a rapid evaporation of the solvent during the polymer deposition. Therefore, rr-P3HT molecules do not have enough time to arrange in a crystalline form. Hence, a high boiling point solvent is preferred [31].

So far, rr-P3HT has shown the best mobility among conjugated semiconducting polymers, exhibiting a mobility of ≈0.1 $cm^2/V \cdot s$ in an organic transistor [31]. The good π-π stacking, the long conjugation length and the high hopping rate in rr-P3HT are reasons for the high mobility [34]. At the present time rr-P3HT is the most promising material for low cost organic devices because of its solubility, relatively high mobility and chemical stability. Nevertheless, the mobility in rr-P3HT is not high enough to build high-speed devices.

2.5.2 **Small organic molecules: Pentacene**

An experiment on rr-P3HT of different molecular weights has shown that the grain size increases when the molecular weight is reduced [34]. In other words, short length molecules

form a more crystalline film. However, the grains are so widely separated that the bulk mobility is very low, with individual grains acting like isolated islands [28]. To enhance the mobility in an organic film the grains have to be expanded to reduce the space between them. To do so a more controlled deposition method is required. Evaporation in high vacuum is a well-known method to deposit a thin film of various materials with a resolution of a few nanometers and a controllable rate down to a fraction of angstrom per second. The evaporation method is not applicable for long polymer chains, but in very short lengths (known as oligomers) the organics can be deposited by this method. In general, small conjugated organic molecules are applied to achieve a more crystalline semiconductor. A key point in the deposition of small organic molecules is the purity of the material. Because of the very short conjugation length, any impurity can produce a defect in the film which lowers the mobility. Therefore undoped small molecules are preferred over the doped material.

Although thiophene oligomers are among the best small organic molecules in terms of mobility [35], pentacene has shown the highest mobility among the organics [35]. A mobility as high as 35 $cm^2/V \cdot s$ has been obtained in a single crystal pentacene deposited by vacuum sublimation [30], which is two orders of magnitude higher than is observed in rr-P3HT [11]. Use of an evaporation method produces a pentacene film with a mobility of about 1 $cm^2/V \cdot s$, which is the same as the mobility in amorphous silicon [21].

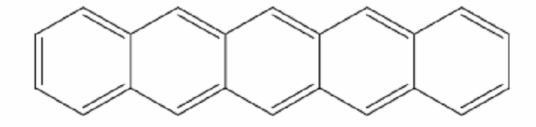


Figure 2.5. Chemical structure of pentacene

The chemical structure of pentacene is shown in figure 2.5. The conjugated structure produces a delocalized carrier over the entire molecule. However, the conjugation length is limited to a very short range by the size of the molecule. The X-ray diffraction patterns of various pentacene films indicate a well ordered crystalline structure for a film deposited at 27 °C [18]. Such an achievement is a breakthrough in efforts to build active matrix displays (AMDs) on plastic substrates, as the major obstacle for amorphous silicon technology is the high temperature of the process [18]. However, the deposition method for pentacene is still as expensive as the amorphous silicon technology.

Pentacene is widely used to study organic semiconductors and demonstrate prototype organic transistors and circuits [36], but it and other small organics are inferior to rr-P3HT when low cost, solution processible methods of fabrication are desired.

2.6 Fabrication techniques

Application of easy and low-cost fabrication process is a key to reduce the capital cost of electronics. The most promising method to produce low-cost electronics is the application of organics in a reel-to-reel process. Small molecules are not suitable for this purpose as the deposition methods applied for them are too expensive. In contrast soluble conducting polymers can be deposited with simple methods such as spin coating, dip casting, and printing techniques. Among those methods, spin coating has been applied extensively to deposit organic semiconductors in organic transistors, because it produces high molecular order in a deposited film particularly when rr-P3HT is applied [33]. Also, as it is explained in chapter 6 a very thin semiconducting layer (< 50nm) is demanded in traditional type of organic transistors (OFETs), which spin coating is a reliable method to deposit such a thin film with no defect. However, spin coating is not compatible with a reel-to-reel process. Therefore, dip casting and printing are preferred [11]. Various methods of printing including screen printing, micro-contact printing, and inkjet printing have been applied to fabricate prototype organic transistors [11]. In most cases the printing method is utilized for patterning the electrodes and connections and the semiconductor layer is deposited with other methods such as spin coating [14, 37, 38] and even evaporation [39]. The reason is that printing methods have relatively poor control on the molecular order, thickness, and roughness of the deposited layer.

Printing a dot with an inkjet printer usually produces a doughnut shape deposited polymer on the surface with a thickness difference of a few hundred nanometers between the outer circular edge and the center of the dot [15, 40]. In micro-contact printing method a relatively thick polymer layer is stamped on the substrate to produce an electrically continuous film. Using this method Park et al. have deposited rr-P3HT films with a thickness of 200 to 500 nm [13]. In dip casting the substrate is dipped in the polymer solution and pulled out with a constant speed. After the evaporation of the solvent a solid film of polymer is left on the substrate. In this method the thickness of the film is controlled by the pulling speed and the concentration of polymer in the solution. As has been experienced by the author, films with thicknesses in the range of 200 nm to 400 nm can be produced by the dip casting method. In the doctor blade

method a film of polymer is deposited by spreading the solution over the substrate using a blade. The gap between the blade and the substrate determines the film thickness. Using this method a polymer film can be having a thickness of a few hundred nanometers [41].

In summary, a printing or casting method is demanded for deposition of semiconductor layer in a reel-to-reel process to fabricate organic transistors. However, these methods generally have poor control on the thickness of the deposited layer with a resolution of a few hundred nanometers. The characteristics of conventional types of organic transistors are very dependent on the thicknesses and quality of deposited semiconductor.

2.7 Energy structure in organic semiconductors

Although the energy gap between LUMO and HOMO in the organics resembles the band gap in the crystalline semiconductors, their energy structure (in the bulk semiconductor) is quite different. As a result the charge transport is different. Instead, the energy structure in organics is similar to that in amorphous silicon hydrogenated (a-Si:H). More than 70 years of study of amorphous semiconductors has been of great assistance to the understanding of energy structure in organics and in the development of organic semiconductors.

In a perfect silicon crystal the conduction and valence bands have a band gap between them. The strong covalent bonds between atoms in the lattice form energy bands in the semiconductor in which carriers are highly delocalized. The absence of any available energy level (state) in the band gap is another feature of a perfect crystal. Any disorder in the crystal lattice produces states in the band gap close to the band edges [42]. The distribution and the density of states change with the level of the disorder in the lattice and the concentration of impurities. Plots of the density of states (DOS) versus energy show a decline in the density of these localized states from the band edges toward the centre of the band gap. The slope region is known as the band tail. Figure 2.6 depicts the density of states in a hypothetical amorphous semiconductor. The width of the tail represents the disorder level in the semiconductor. A semiconductor with a high molecular order has a sharp slope (narrow band tail), whereas in a disordered material the band tail is wide. The states located in the band tails are localized states. Moving toward the band edges (E_C or E_V) the density of states increases and the charge is more mobile. At a certain energy level, which is called the mobility edge, the charge is delocalized. The states located beyond the mobility edge are extended states in which the mobility is limited by the scattering.

For a crystalline semiconductor with some disorder in its structure the mobility edge is same as the band edge and the extended states are located in the bands.

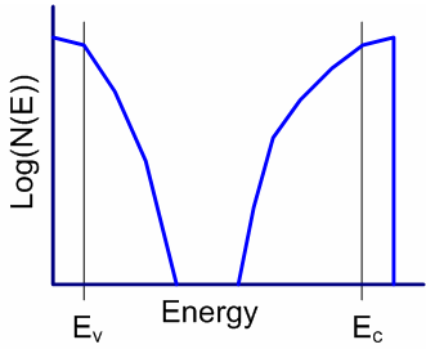


Figure 2.6. The density of states (DOS) in a semilog plot for a hypothetical amorphous semiconductor.

In addition to the disorder, any defects or impurities in a semiconductor generate localized states in the band gap. The states generated from defects are mostly located in the mid band gap with a Gaussian distribution [43] (not shown in figure 2.6). Such localized states are very common in silicon, particularly in amorphous silicon, because of the dangling bonds. In contrast, the localized states from impurities appear as tail states which are closer to the mobility edge [44].

For a largely amorphous organic semiconductor the situation is different in some aspects. The very limited periodicity in these materials causes them to have either very narrow bands or even no bands at all [45]. Consequently, the mobility edge is not well defined or it does not exist at all. Using the DOS plot, the energy level at which the density of states starts to drop off is taken as the mobility edge. Since there are no dangling bonds in most organic semiconductors, the localized states are mostly in form of tail states close to the mobility edges. However, dopants in organics act like impurities and produce extra localized states in the tail states. Such an energy structure affects the carrier transport in the semiconductor, which is discussed in the next section.

The application of different deposition methods produces organic films with different molecular order. Therefore, the distribution of density of states changes with the deposition method. Indeed, the density of states is not very reproducible even when repeating a given process because of the many parameters that affect the molecular order in a deposited layer of organics.

It has been observed that most organic semiconductors are *p*-type. This is because the band tails are not in general symmetric for electrons and holes, so the carrier that has a wider band tail is more localized. As a result, the semiconductor often behaves as a single type carrier material. In amorphous silicon electrons are the mobile carrier, whereas in most organic semiconductors, including rr-P3HT and pentacene, holes are the main carriers. Depending on the dominant carrier type the semiconductor is introduced as intrinsic n-type or p-type material e.g. rr-P3HT and pentacene are p-type organic semiconductors. Also, as is explained in section 2.3 oxygen and water act as dopants. Since they typically produce a density of holes in the semiconductors far in excess of the intrinsic carrier density (by a few orders of magnitude even if processing is done in an inert environment) [44], the effective carrier density is equal to the dopant density in a doped organic semiconductor.

2.8 Carrier transport mechanism in organic semiconductors

In a crystalline material the mobility is limited by scattering mechanisms. In an intrinsic semiconductor the mobility drops with increasing temperature. In contrast the effective mobility increases with temperature in most intrinsic organic materials, indicating a different mechanism of charge transport [46]. In fact the free-electron approximation is not applicable for organic semiconductors because the carriers are not as delocalized as those in crystalline materials. In these materials the concept of effective mass is no longer applicable, and the 'mobility' that is derived is really an indication of how easily carriers move between localized states. A variety of mechanisms that account for localized states are used to model the charge transport in amorphous materials. Application of an appropriate model is necessary to study and simulate organic devices. In this section three important mechanisms used to model charge transport in amorphous materials are reviewed. The multiple trapping and release model is later used in simulations.

2.8.1 Nearest-neighbour hopping

Since the conductivity of amorphous materials increases with temperature (even in disordered 'metals'), Miller and Abraham (1960) initiated a model for carrier transport assisted by phonons [45] called nearest-neighbour hopping. In the model it is assumed that a charge is transferring from an occupied to a nearest unoccupied state with the same energy level. Assuming that the two states are spatially so far from each other that the tunneling probability is low, the charge

can instead hop to the unoccupied states by passing over the barrier. Of course, if the barrier is very low, thermal energy (kT) is sufficient for the carrier to pass over the barrier. In the case that the barrier is high the charge has the option of borrowing extra energy from the lattice (phonons) to surmount the barrier, releasing the energy back to the lattice after the hop [47]. The diagram in figure 2.7 indicates the difference between the tunneling and hopping processes. Such a charge transport mechanism requires strong electron-phonon coupling. According to this model the conductivity changes exponentially with temperature [45]:

$$\sigma_h = \sigma_{h0} \exp\left(-\frac{E_b}{kT}\right) \tag{2.2}$$

where σ_h is the conductivity due to nearest-neighbour hopping, σ_{h0} is the conductivity in the absence of barrier between states, E_b is the barrier height, k is the Boltzmann constant and T is the absolute temperature in Kelvin.

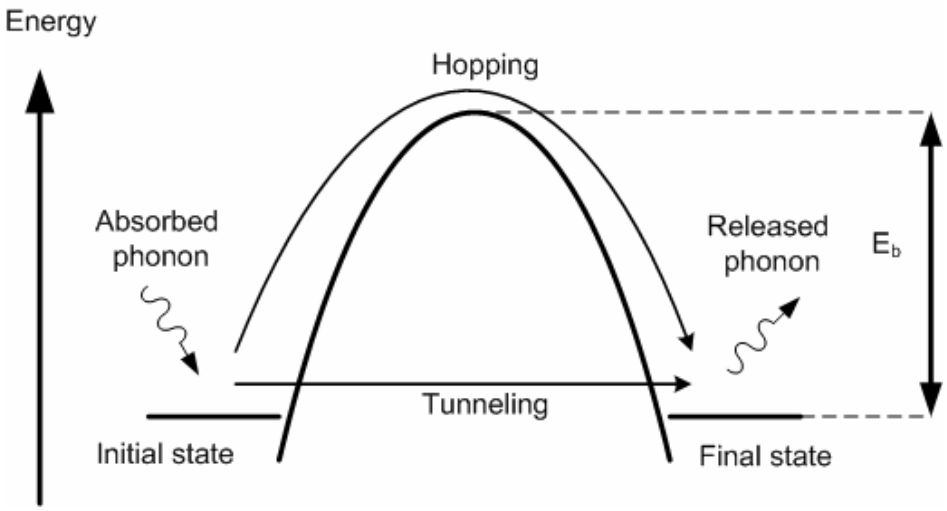


Figure 2.7. Hopping versus tunneling between two localized states.

2.8.2 **Variable Range Hopping (VRH)**

The nearest-neighbour hopping model was further developed by Mott (1969) for a more general case known as variable range hopping. In this model the hopping process is not limited to nearest neighbours. Also the energy difference between the source and the destination levels are considered. The derivation is provided here, following the approach used by Morigaki [45] in

order to provide some insight into the mechanisms suggested by Mott. According to VRH model the jumping frequency, *p*, from state *i* to state *j* is given by [45]:

$$p = \nu_{ph} \exp\left(\frac{E_i - E_j}{kT}\right)\exp\left(-\frac{2R_{ij}}{a}\right) \tag{2.3}$$

where v_{ph} is the phonon frequency, and E_i and E_j are the source and the destination energies, respectively. R_{ij} is the spatial distance between two states and a is the localization length.

The diffusion coefficient in one direction , *D*, can be estimated by [43]:

$$D = \frac{pR^2}{6} \tag{2.4}$$

and using the Einstein relation the mobility, μ, is expressed by:

$$\mu = \frac{qD}{kT} = \frac{qpR^2}{6kT} \tag{2.5}$$

The carrier density is approximated as the product of the density of states at the Fermi level and the range of allowable energies, which is approximately *kT* [45]:

$$n \cong N(E_F)kT \tag{2.6}$$

Therefore the conductivity is:

$$\sigma = \frac{1}{6}q^2 pR^2 N(E_F) \tag{2.7}$$

In equation 2.3 the energy difference (E_i-E_j) can be replaced with a function of density of states, *N(E)*, and the spatial distance, *R*. Obtaining the most probable distance for hopping by setting $\partial p/\partial R$=0, it can be shown that the conductivity depends on temperature as follows [45]:

$$\ln\sigma \propto T^{-1/4} \tag{2.8}$$

This is called the $T^{-1/4}$ law. The law has been experimentally confirmed in amorphous silicon [45]. Vissenberg and Matters (1998) showed that the conductivity both in solution-processed organic semiconductors and vapour deposited small molecules follows the $T^{-1/4}$ law which indicates the dominance of VRH as the charge transport mechanism in those organics [48].

2.8.3 **Multiple Trapping and Release (MTR)**

In crystalline semiconductors like silicon, some impurities (e.g. gold) produce localized states in the band gap. These states are known as traps because they capture mobile carriers very often. After being trapped a charge might be thermally released or be recombined. The average time that a charge stays in the trap level is called the relaxation time. Generally the relaxation time is longer in deep traps than that in shallow traps [49]. Since the density of traps in crystalline semiconductors is usually low compared to the carrier concentration, the effect of traps on the mobility is negligible. However, in amorphous semiconductors the density of localized states is quite significant relative to the carrier density. Therefore, the carrier motion is frequently interrupted by capture and release processes. Such a carrier transport mechanism is known as Multiple Trapping and Release (MTR) and has been suggested by Horowitz as a practical model for charge transport in organic devices [50]. In this model the drift mobility, μ_D, is related to the mobility in the delocalized band, μ_0, by:

$$\mu_D = \alpha\mu_0 \exp\left(-\frac{\Delta E_t}{kT}\right) \tag{2.9}$$

where in a single trap level ΔE_t is the activation energy of the trap (the energy difference between the trap level and the mobility edge) and α is the ratio between the density of states at the edge of the energy band and the density of traps.

The MTR model is good at describing the charge transport in a semiconductor with wide bands and with tail states when the Fermi level is close to the band edge. The model can also be used for an amorphous semiconductor with a very narrow band (or even no band) assuming that μ_0 is the mobility at the mobility edge. Although the model indicates an increase of the mobility with temperature, it is not in general as effective as the variable range hopping model at predicting change in conductivity with temperature. In addition, the relaxation time is simply correlated to the trap level in the MTR model, whereas in reality it is likely to be strongly dependent on the electron-phonon interactions. Therefore, the model is not appropriate for time analyses, However experimental results strongly support the application of the trapping model for DC analysis of organic devices at a constant temperature [51, 52]. The model is widely used to simulate organic electronic devices under DC biases at room temperature [51]. The MTR model is used to simulate organic transistors in this thesis. The compatibility of the simulation results

with the experimental results obtained by others [16, 81] supports the application of the model, as discussed in section 5.2.2.2.

2.9 Bulk mobility versus field-effect mobility

The mobility depends on the distribution of states in the energy gap, as mentioned in section 2.7. The mobility also changes with the Fermi level. For a given density of states the mobility increases when the Fermi level approaches the mobility edge. Figure 2.8 shows the density of states in a hypothetical doped p-type organic semiconductor in which E_i represents the intrinsic Fermi level in the semiconductor. By shifting the Fermi level toward E_i (figure 2.8.b) the conductivity of the semiconductor drops significantly because both mobility and carrier concentrations (equation 2.6) are decreased. In contrast, if the Fermi level moves toward the mobility edge (figure 2.8.c) the conductivity increases. Such an effect is applied in OFETs to turn on and off the transistor. In an OFET the position of the Fermi level relative to the mobility edge is controlled at the surface of the semiconductor layer by the electric field emanating from the gate electrode. As a result of this effect the mobility measured in an OFET when the transistor is on is usually much higher than the mobility in the bulk semiconductor. This mobility, represented by μ_f, is known as field-effect mobility. For rr-P3HT a field-effect mobility as high as 0.1 $cm^2/V{\cdot}s$ has been reported [12], whereas the bulk mobility is usually about 10^{-4} $cm^2/V{\cdot}s$ [53].

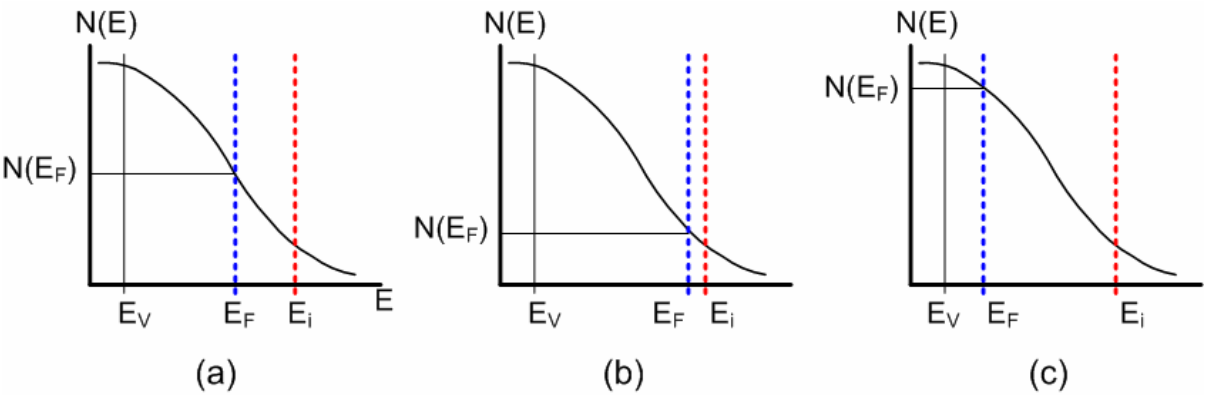


Figure 2.8. (a) Density of states and position of the Fermi level in a hypothetical doped p-type organic semiconductor. Carrier density and mobility (b) reduce or (c) increase when the Fermi level changes.

The bulk mobility in an organic semiconductor can be enhanced by doping the semiconductor (shifting the Fermi level towards the mobility edge). Indeed, experiments show that the bulk mobility in conducting polymers can be increased by three orders of magnitude through doping processes [44]. Increasing the doping density might be expected to ultimately bring bulk mobility as high as the field-effect mobility. However increasing the concentration of dopants increases disorder in the semiconductor and broadens the density of states, so that the mobility in the bulk generally is not as high as the field effect values observed in OFETs.

2.10 Summary

A conjugated structure enables organic molecules to have semiconductor characteristics. However, if the carriers are delocalized in a conjugated organic molecule, the organic molecules must form a well-ordered structure (π-π stacking) to achieve a reasonable bulk mobility. Organic semiconductors are classified as either conducting polymers or small molecules. Conducting polymers are generally used for low-cost fabrication. A soluble conducting polymer such as rr-P3HT produces a reasonably ordered film when spin coated. The highest reported mobility for rr-P3HT is about 0.1 $cm^2/V \cdot s$. In contrast, small organic molecules are used when the cost is not a critical issue and higher mobility is required. The mobility in a pentacene film is typically about 1 $cm^2/V \cdot s$ when it is deposited by an evaporation method. Since the aim of this thesis is to help enable low-cost organic electronics, rr-P3HT is chosen as the semiconductor material for the various devices.

The energy structure of organics is different from that in crystalline semiconductors. A poor periodicity in organics and a very weak interaction between molecules in a film cause them to have either narrow or non-existent energy bands. Instead, there are many localized states in the energy gap between the HOMO and LUMO. These states are mostly distributed close to the original molecular energy levels (HOMO and LUMO) and form band tails. The band edge with the less dense band tails provides the most mobile carrier, resulting a single carrier type semiconductor (usually p-type).

A few of the most important mechanisms of charge transport in organics are reviewed in this chapter. Among them variable range hopping is the most appropriate mechanism which can often explain the temperature dependence of conductivity in organics. The challenge is that the phonon frequency and the density of states are needed to fully quantify the model. The multiple

trapping and release (MTR) mechanism is more readily applicable. Although, MTR cannot completely explain the semiconductor behaviour, it can be used for the DC analysis of a device at constant temperature.

An important aspect of organic semiconductors is that the mobility is dependent on the distribution of localized states and position of the Fermi level. For a given density of states the mobility increases when the Fermi level is shifted towards the mobility edge. Enhancement in mobility can be achieved either by application of an external electric field or by a doping process.

Chapter 3

CAD tool and experimental methods

The work performed in this thesis involves the simulation and fabrication of organic electronic devices. In this chapter the capabilities of the CAD tool used for simulation of organic devices are discussed. Then the material characteristics required to model the electronic properties of organic semiconductors are introduced. The origin and values of these characteristics are presented. The microelectrode design on which all devices are built is explained. In addition, the experimental setup used to fabricate and test organic devices is described. Details specific to particular devices and simulations, as well as the measured and simulated characteristics, are described in later chapters.

3.1 CAD tool

Medici version 4.0 (produced by Synopsys [54]) is used as the CAD tool for device simulation. Medici is a powerful device simulation program that can be used to simulate the behaviour of various semiconductor devices. It models the two-dimensional distributions of potential and carrier concentrations in a device. The program can be used to predict electrical characteristics for arbitrary bias conditions. The program solves Poisson's equation and the current continuity equation to analyze devices such as diodes and transistors. Medici can also analyze devices in which current flow is dominated by a single carrier. Such a feature is an advantage to simulate organic based devices. Medici uses a non-uniform triangular simulation grid, and can model arbitrary device geometries with both planar and non-planar surface topographies. The simulation grid can also be refined automatically during the solution process. This flexibility makes modeling of complicated devices and structures possible. Also, electrodes can be placed anywhere in the device structure, which is useful to simulate a device with an arbitrary geometry.

Furthermore Medici is capable of simulating non-crystalline semiconductor devices by the application of a specific module called Trapped Charge Advanced Application Module (TC-AAM). TC-AAM allows detailed analysis of semiconductor devices containing traps, such as

thin-film transistors (TFTs). Also the module allows simulation of carrier trapping and de-trapping mechanisms within semiconductor materials. For the analysis of traps, the energy gap is divided in up to 50 discrete energy levels. The trapping process is then analyzed at each trap level. Although none of the models for the charge transport in amorphous semiconductors described in section 2.7 is explicitly applied in Medici 4.0, the MTR model is implicitly utilized as is explained in the following section.

3.1.1 **MTR model in Medici**

The drift-diffusion current density (in direction x) for electrons, J_e, in a semiconductor is expressed by [55]:

$$J_e = n\mu_e \frac{dE_{Fn}}{dx} \tag{3.1}$$

where n is the free carrier density, μ_e is the mobility of electrons in the conduction band and E_{Fn} is the quasi-Fermi level for electrons. Equation 3.1 is used in Medici, where n includes carriers contributed to the conduction band. Considering n_t as the trapped charge density, the total carrier concentration, n_{tot}, is equal to $n+n_t$. Therefore, n/n_{tot} represents the fraction of the total charge which is delocalized. Since in amorphous semiconductors $n_t >> n$ the ratio can be written as n/n_t. For a single trap level n and n_t can be replaced with the equations described in Ref. [43]:

$$\frac{n}{n_t} = \frac{N_C \exp\left(-\frac{E_C - E_{Fn}}{kT}\right)}{N_t \exp\left(-\frac{E_t - E_{Fn}}{kT}\right)} = \frac{N_C}{N_t}\exp\left(-\frac{\Delta E_t}{kT}\right) = \alpha \exp\left(-\frac{\Delta E_t}{kT}\right) \tag{3.2}$$

where N_C and N_t are effective density of states at the edge of the conduction band and at the trap level, respectively. E_C and E_t are energy levels at the conduction band edge and the trap level. ΔE_t is the activation energy of the trap (the energy difference between the trap level and the mobility edge). Therefore equation 3.1 can be written as:

$$J_e = n_{tot}\alpha\mu_e \exp\left(-\frac{\Delta E_t}{kT}\right)\frac{dE_{Fn}}{dx} \tag{3.3}$$

Equation 3.3 represents the approach used in Medici to describe conduction resulting from carriers occasionally released by trapped states. This is equivalent to the MTR treatment. Substituting the drift mobility from equation 2.9 (MTR model) gives:

$$J_e = n_{tot}\mu_D \frac{dE_{Fn}}{dx} \tag{3.4}$$

Medici implies equation 3.1 by distinguishing between n and n_t and application of mobility in the delocalized band, whereas in the MTR model all carriers (n_{tot}) are assumed to be mobile with a lower mobility (drift mobility). Therefore, Medici is mimicking the MTR model as equations 3.1 and 3.4 are the same. The same conclusion is deduced for holes if electrons are replaced with holes in equations 3.1 to 3.4. The discussion is also valid if the localized states are distributed in energy. In such a case n_t represents the total density of trapped charges. Hence, Medici 4.0 is capable of simulating an organic device, which is done through the TC-AAM module.

3.1.2 **Semiconductor parameters**

To apply Medici as a CAD tool for simulation of organic devices, the semiconductor has to be properly characterized. Since our aim is to fabricate organic devices with solution-processible materials, regioregular-poly(3-hexylthiophene) (rr-P3HT) is chosen as the semiconductor. For a DC analysis the band gap, electron affinity, density of states, carrier mobility, permittivity, and dopant density of rr-P3HT are required. These values have been extracted from the literature.

The band gap of rr-P3HT is measured to be 1.7 eV by Chen et al. [56]. To measure the band gap they used a UV-Visible spectroscopy method in which the light absorption is recorded as a function of the wavelength of the incident light in the ultraviolet or visible regions of the spectrum. The electron affinity of rr-P3HT is calculated to be 3.15 eV from the ionization energy and the band gap of the polymer [57]. The ionization energy is obtained from photoemission spectroscopy, in which the material is irradiated with UV light and the kinetic energies of electrons emitted from the material are measured. The energy difference between the source photon energy and the released electrons is used to find the ionization energy. Subtraction of the ionization energy from the band gap gives the electron affinity [57]. Since rr-P3HT is a p-type material the simulation is done on holes as carriers and the effect of electrons is ignored. Therefore, only the density of localized states close to the valence band is

considered. To mimic the density of states in rr-P3HT we have applied 19 discrete levels of trap states close to the valence band edge based on the density of states measured by Tanase et al. [58]. They have estimated the density of states in rr-P3HT by measuring the mobility in a field-effect transistor (FET). The applied levels are listed in table 3-1 where E_i represents the energy level in the *i*th trap level. By using their estimated densities the model will reproduce the relative changes in mobility and conductance as a function of field that are observed in Tanase's work. This response is highly dependent on the purity, synthesis and processing steps employed in depositing the polymer. The models are thus used to determine what is possible rather than to match quantitatively with experimental results.

Table 3.1. Discrete levels of trap density relative to the edge of valence band in rr-P3HT

E_k	E_k-E_V (eV)	Density of localized states ($cm^3.eV)^{-1}$
E_1	0	$1.00x10^{21}$
E_2	0.03	$4.15\ x10^{20}$
E_3	0.06	$1.72\ x10^{20}$
E_4	0.09	$7.15\ x10^{19}$
E_5	0.12	$2.97\ x10^{19}$
E_6	0.15	$1.23\ x10^{19}$
E_7	0.18	$5.12\ x10^{18}$
E_8	0.21	$2.12\ x10^{18}$
E_9	0.24	$8.82\ x10^{17}$
E_{10}	0.27	$3.66\ x10^{17}$
E_{11}	0.30	$1.52\ x10^{17}$
E_{12}	0.33	$6.31\ x10^{16}$
E_{13}	0.36	$2.62\ x10^{16}$
E_{14}	0.39	$1.09\ x10^{16}$
E_{15}	0.42	$4.51\ x10^{15}$
E_{16}	0.45	$1.87\ x10^{15}$
E_{17}	0.48	$7.78\ x10^{14}$
E_{18}	0.51	$3.23\ x10^{14}$
E_{19}	0.54	$1.34\ x10^{14}$

Since Medici uses the MTR model for the charge transport in amorphous semiconductors, the mobility of carriers in the energy band is necessary for the simulation. Since the energy band might not exist in rr-P3HT or if it does it is a very narrow band [35], the mobility in the band

has not been determined. However, it has been shown that the highest mobility that can be achieved from rr-P3HT is about 0.1 cm^2/Vs [12, 31]. In this work this value has been taken as the mobility at the mobility edge of rr-P3HT, thereby providing an upper bound on performance in this respect. The relative permittivity of rr-P3HT is assumed to be 3, as is typical of most organic semiconductors [59]. The background dopant density in rr-P3HT is set at 1×10^{16} cm^{-3} as Meijer et al. have measured it in an organic thin-film transistor [60]. They used conventional semiconductor equations for the depletion width in a transistor to obtain the doping density. Although it is not very accurate it provides a reasonable estimate of the actual dopant density.

In general there are two sources of carriers in organic semiconductors: dopants and defects. Since the typical density of carriers generated from defects ($\sim10^{13}$ cm^{-3}) [44] is much smaller than the dopant density, the effective carrier density is taken to be equal to the dopant density in a doped organic semiconductor.

In the simulations gold and aluminium are assumed as the metal contacts for all devices. In order to describe metals in Medici the work function are set (5.1 eV and 4.3 eV for gold and aluminium, respectively) [61]. In some of the devices silicon dioxide is employed as a common insulating layer. Silicon dioxide is already defined in the library of Medici. Therefore, there is no parameter to set for SiO_2 in Medici. The list of parameters set for rr-P3HT in Medici is provided in table 3-2.

The output file in Medici is either a graph type in postscript format or a data file in text format. In order to have the flexibility to use the plots in a different code has been written in Matlab (M-file) which converts the text file to an spreadsheet format. After the conversion data are analyzed and redrawn in Matlab. The Matlab code is presented in appendix A of this document.

Table 3.2. The list of set up parameters used for materials in the simulation of organic devices.

Material	**Parameter**	**Symbol**	**Value**	**Unit**	**Ref.**
rr-P3HT	Band gap	E_g	1.7	eV	[4]
	Electron affinity	χ_e	3.15	eV	[5]
	Permittivity	ε_r	3		[10]
	Dopant Density	N_S	$1x10^{16}$	cm^{-3}	[11]
	Mobility	μ	0.1	cm^2/Vs	[8,9]
Metals	Au work function	φ_{Au}	5.1	eV	[12]
	Al work function	φ_{Al}	4.3	eV	[12]

3.2 Micro fabrication

In order to build organic electronic devices conventional patterning processes were applied to create electrical connections. For the initial proof of concept stage performed in this thesis conventional processing is preferred to the novel methods such as printing because of the reliability and the yield in the fabrication. The principal part of the fabrication is building electrodes. The electrodes are utilized as terminals for the organic devices. Once electrodes are fabricated on a substrate the organic semiconductor is deposited on the electrodes to build a device. Depending on the type of device another electrode might be deposited over the semiconductor layer. In this section the focus is on the fabrication of the base electrodes. The details of each device geometry and operation are explained in later chapters.

Silicon wafers are chosen as the substrates on which to build the electrodes. In prototype organic transistors it is very common to use highly doped silicon as the gate as well as the substrate of the device. A thermally grown silicon dioxide layer acts as the insulator for the transistor. The SiO_2 layer can also be used as an insulating base to build conductive electrodes. Si/SiO_2 4" wafers from Silicon Quest International (SQI) are employed as substrates for the devices presented in this thesis [62]. The silicon is highly doped n-type (Arsenic) with a resistivity of 0.005 Ω.cm. The silicon grade is "prime" and has a chemically polished surface. A 350 nm thick layer of SiO_2 is grown at the factory on both sides of the wafer using a thermal growth process. The product is used as the substrate on which metallic electrodes are deposited.

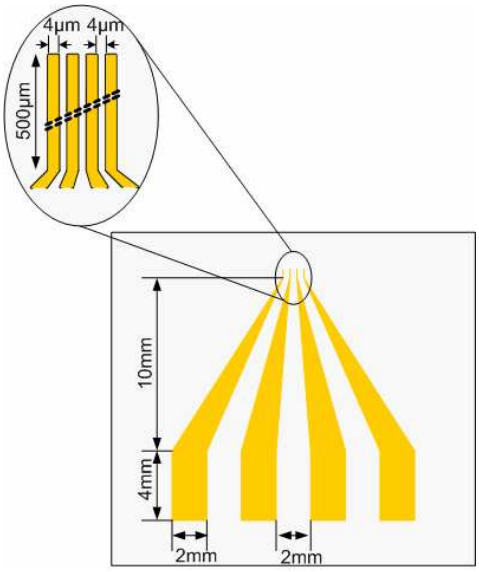


Figure 3.1. The micro-electrode designed for organic electronic devices.

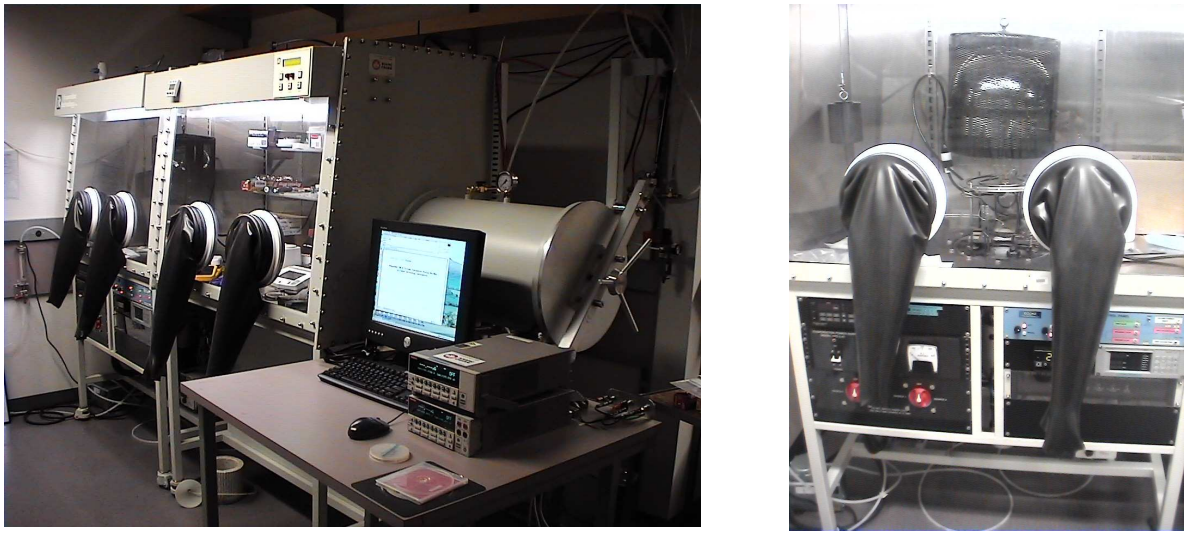
In the design of the electrodes the versatility of use with a range of organic devices is considered, as the ease of electrical connection. Four electrodes, each with a length of 500 μm, a width of 4 μm and a 4 μm spacing are designed. Each electrode is connected to a large pad which is located about 1 cm from the electrodes. Since the feature size in the electrode area is on a micro meter scale these are called micro-electrodes. Figure 3.1 is a sketch of a micro-electrode. Since a resolution of 4 μm is required a photolithography method is applied to pattern a photoresist layer on the Si/SiO2 substrate. A metal layer is then deposited all over the surface. Removing the photoresist leaves the metal electrodes on the substrate. This process is known as the lift-off process.

Although the fabrication process is a standard process which may be found in any microfabrication textbook, the details of process which are necessary for reproducing it are dependent on the equipments and materials that have been used. The process is explained in appendix C with sufficient details for future students, and with instructions specific to the available equipment in the AMPEL cleanroom [63].

3.3 Glove box, device fabrication and electrical connections

Since many organic semiconductors show a change in their electrical characteristics when they are exposed to air, a glove box system is used to fabricate organic devices and to test them. A glove box is an enclosed box filled with an inert gas (in this case it is filled with nitrogen) with a transparent side. Users have an access to the internal space of the box with sets of gloves attached to the transparent side of the box. The gas inside the glove box is circulating constantly through a filter which absorbs chemicals and purifies the gas. To transfer in (out) chemicals or samples an airlock system is devised for the glove box.

The glove box is equipped with a digital balance to weigh chemicals and an ultrasonic bath to dissolve particles of solute when a solution of organic semiconductor is prepared for spin or dip coating onto the electrode arrays. To fabricate an organic device a micro-electrode is transferred into the glove box. A spinner, located inside the glove box, or a manual dipping process is used to deposit a layer of the organic semiconductor from the solution on top of the micro-electrode. Depending upon to the type of device a layer of metal might be deposited over the semiconductor by means of a thermal evaporator embedded in the glove box. The device is then



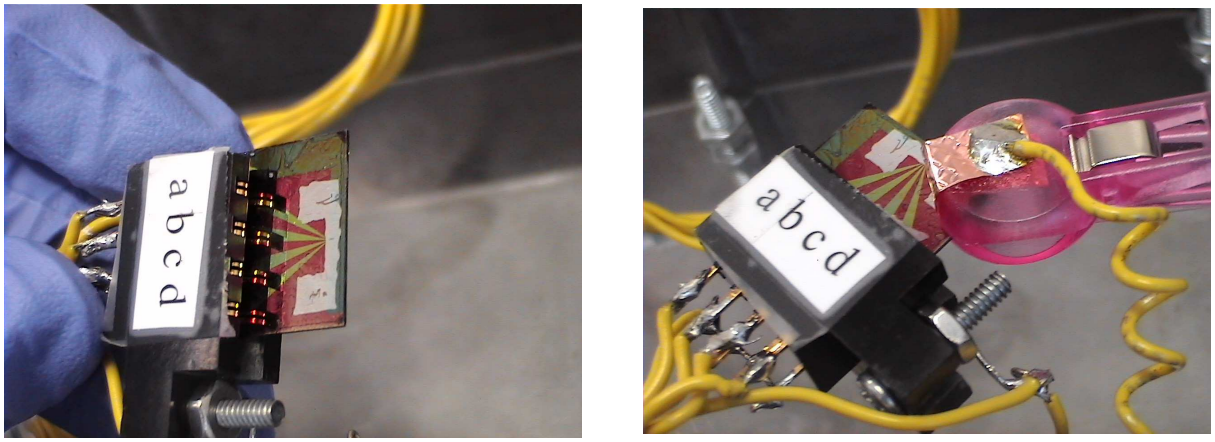
(a) (b)

Figure 3.2. (a) The glove box system (b) the embedded evaporator.

ready to be electrically tested. The details of the fabrication of each device are provided in the relevant chapters.

The thermal evaporator located inside the glove box allows the fabrication a device without exposing the semiconductor to air. The system is custom made to my specifications and was fabricated by Cooke Vacuum Inc. [64]. It consists of a 47” wide glove box with an embedded thermal evaporator. The glove box has 4 glove ports of which two are dedicated to the evaporator. The evaporator has three thermal sources with 2 kW power and is useful for small volume deposition. The vacuum system is a diffusion pump with a liquid nitrogen trap which can provide a vacuum as low as 1×10^{-6} torr. Figure 3.2 shows the system.

To test the electrical characteristics of a device a metal box is used as the Faraday cage to shield the device from electromagnetic interferences. The box is connected to the ground of the instruments. Inside the box a slot connector is embedded to make electrical connection to the pads of the micro-electrode by sliding it into the connector. For the top layer connection a plastic clip covered in copper tape is used, as shown in Figure 3.3b. Such a convenient connection is designed to be easy enough for manipulation with the gloves inside the glove box. Figure 3.3 shows how a sample is connected. The connector is wired to a set of female banana plugs on the side of the metal box. A set of coaxial cables are used to connect the box to instruments located out of the glove box. The cables are passed through a cable gland sealed by



(a) (b)

Figure 3.3. (a) The slot connector with an electrode array inserted and (b) top electrode connection using a clip.

cork seal. The shield of the cables is grounded on the instrument side to protect signals from noise.

For electrical measurements I used either an impedance analyzer (Solartron SI1287 + SI1260) or Source Measure Units (Keithley 2400 and 6430).

3.4 Summary

Medici 4.0 is used as a CAD tool for DC analyses of organic devices with arbitrary geometries. The MTR model is implicitly applied in Medici, a model which is appropriate for describing the charge transport in amorphous semiconductors. All simulations are done assuming rr-P3HT is the organic semiconductor. Rr-P3HT is specified for Medici by its band gap, electron affinity, density of states, carrier mobility, permittivity, and dopant density. All parameters used are based on experimental values extracted from the literature. The density of localized states in particular is dependent on the synthesis, purification and processing steps used. The models employing these properties are used to establish the feasibility of device designs rather than precise quantitative fits.

Micro-electrodes are fabricated using standard photolithography methods. The electrodes form platforms on which the transistors and diodes described in this thesis are built. Each micro-electrode consists of 4 gold electrodes with a length of 500 μm and width of 4 μm with spacing

between electrodes of 4 μm. These electrodes are connected to large pads for easy connection. Also, the substrate is highly conductive silicon with a silicon dioxide coating.

A glove box system with an embedded evaporator is used for the fabrication and testing of organic devices in an inert environment.

Chapter 4

Organic Schottky Diode

A substantial drawback of current organic transistor technology is the relatively large voltage at which devices operate. The large voltage is the consequence of the thick insulating layer used between the gate and the semiconductor. This thick layer is used because low cost methods of producing thinner insulating layers are still under development [65]. Schottky contacts have long been known to enable depletion regions to be modulated at low voltages. The fabrication of such a contact is demonstrated, showing that diode characteristics can be obtained. In Chapter 5 the Schottky contact is then used in a transistor, enabling low voltage operation. In Chapter 6 the Schottky contact is used in combination with a standard organic field effect transistor to show that the transistor performance can be greatly improved. The Schottky diode performance is thus central to all the work that follows. In this chapter the Schottky contact between rr-P3HT and aluminium is studied by fabricating and testing organic Schottky diodes in air and inert environments. The demonstration of such a metal-semiconductor is not new [40, 44], but establishing the characteristics of the junctions under the processing conditions employed is important for subsequent demonstrations of transistors.

The first few sections in this chapter are dedicated to the theory of a Schottky contact both in crystalline semiconductors and organics. Since the energy bands model is inappropriate for most of the polymer and small-molecule semiconductors employed in devices, the thermionic model is not applicable in organic Schottky contacts. A diffusion model is instead chosen for describing transport across the junction. This provides a justification for modeling current in the forward bias via an exponential function in certain situations where localized states dominate transport.

Then, the fabrication of the Schottky diode is described. The electrical characteristics of organic Schottky diodes fabricated in ambient conditions are then presented, which show poor reverse current (~4 nA) and breakdown voltage (~2.5V). The aging effect is also studied in the device, as previously reported [66]. Fabricating the diode in an inert environment shows an enhancement in the diode performance. A breakdown voltage larger than 10 V is obtained for

the diode with a reverse current less than 1 nA, which are sufficient for the operation of the MESFET design. Also, the frequency and time responses of the diode are studied. Finally, a steady and reproducible increase in current at constant voltage is observed in air-fabricated diodes, which the effect is interpreted as an apparent inductance described in Ref [67].

4.1 Introduction

In general any Metal-Semiconductor (MS) contact in electronic devices is a Schottky junction [68] and its DC electrical characteristic is determined by a function describing the current (I) at the junction versus the applied voltage (V). In the specific case that the current is a linear function of the voltage, the junction is called an ohmic contact. In most textbooks and scientific papers the term “Schottky contact” is used when the MS contact is not ohmic. In this thesis I have used the same terminology to distinguish a linear I-V function from a non-linear one by using the terms ohmic and Schottky contact.

Schottky contacts in organic semiconductors have been studied for more than two decades and have been used to build the first generation of organic light emitting diodes (OLEDs) [44]. A key aim of this thesis is to build an organic MESFET, as studying, optimizing and reproducing organic Schottky contacts are useful for understanding and influencing transistor characteristics.

4.2 Structure and energy diagram

A popular way to make an organic Schottky diode is a stacked structure in which a thin layer of an organic semiconductor is sandwiched between two metal contacts: an ohmic and a Schottky contact. The focus in the devices demonstrated here is on the Schottky junction as it determines the device characteristic. For a crystalline semiconductor the energy band diagram is usually used to explain the junction behaviour. The metal and the semiconductor each have a Fermi energy level (E_F), as shown in figure 4.1. At thermal equilibrium when the metal makes contact with the semiconductor, the bands bend in the semiconductor to align the Fermi level all along the junction (figure 4.1.b). The band bending is the result of a space charge region in the semiconductor adjacent to the metal contact. A potential barrier (φ_B) appears at the metal-semiconductor interface. According to the diagram in figure 4.1 the height of the barrier in a p-type semiconductor is:

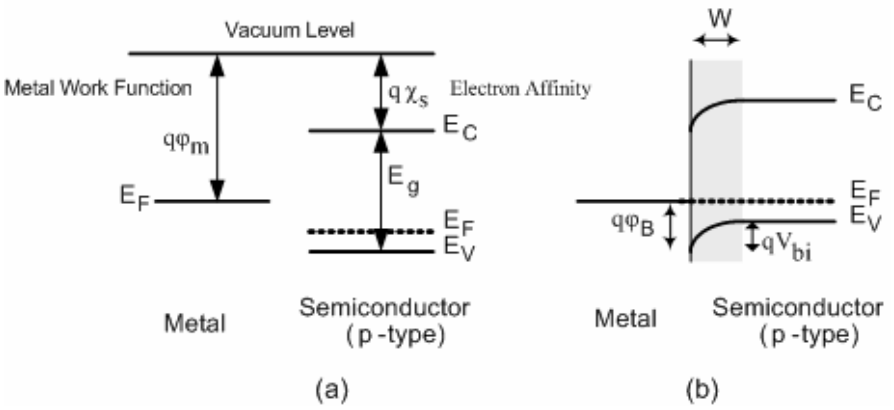


Figure 4.1. The energy diagram of a metal and a semiconductor (a) before and (b) after the junction.

$$q\varphi_B = q\chi_S + E_g - q\varphi_M \tag{4.1}$$

where q is the unit charge, $q\varphi_M$ is the work function of the metal, E_g is the band gap in the semiconductor, and $q\chi_S$ is the electron affinity in the semiconductor.

If the carrier density in the space charge region is much less than that in the bulk semiconductor, similar to the case shown in figure 4.1.b, the region is called depletion region. In order to determine the width of the depletion region (W), first the electric field is calculated by integrating Poisson's equation across the junction:

$$\mathcal{E} = -\frac{dV(x)}{dx} = \frac{1}{\varepsilon_S}\int \rho(x)dx \tag{4.2}$$

where ε_S is the permittivity of the semiconductor, x, is the distance from the junction, $\mathcal{E}$ is the electric field, ρ is the charge density and $V(x)$ is the electrical potential at x.

For a uniformly doped crystalline semiconductor, a reasonable approximation [49] is that the carriers are completely depleted over the width, W, such that the charge density in the depletion region is equal to the dopant density (N_A) times the unit charge (q) (the sign of the charge has to be considered as well). To balance the charge in the semiconductor electrons are removed from the surface of the metal to generate a zero net charge across the junction.

Therefore, in the depletion region ($0 < x < W$) the electric field and the potential are linear and quadratic functions of the distance, respectively. In a static state (biased) the electrostatic

potential difference across the junction is V_{bi} - V_A where V_A is the applied voltage in the forward bias and V_{bi} is the built-in voltage in the junction (figure 4.1 (b)). Application of the quadratic function, then, gives the depth of the depletion region as:

$$W = \sqrt{\frac{2\varepsilon_s}{qN_A}(V_{bi} - V_A)} \tag{4.3}$$

Equation 4.3 shows that the depletion width extends in the reverse bias (V_A<0).

In the above discussion the effect of image force, interfacial layer and the pinning phenomenon are ignored, whereas they have significant effects on the barrier height and the band bending. However, for the depletion width calculation, all these effects can be included by adjusting the built in potential as they mostly affect the barrier height. Equation 4.3 is found to provide a good description of the depletion width in uniformly doped crystalline semiconductors [69].

The differential capacitance associated with the depletion region (C_d) is inversely proportional to the depletion width. An impedance measurement can be applied to determine C_d and thereby to estimate *W*. Also, the measured capacitance at different biases allows the determination of the doping density and the built in voltage from the slope and the voltage intercept of the (C^{-2}-V_A) plot [70], if the semiconductor is uniformly doped:

$$\frac{1}{C^2} = \frac{2}{q\varepsilon_s N_A}(V_{bi} - V_A) \tag{4.4}$$

However, the situation in organic semiconductors is very different because of the difference in the energy structure between organic and crystalline semiconductors. As a result (explained in the next section) equations 4.3 and 4.4 are not appropriate to describe an organic Schottky contact and capacitance measurement is not an appropriate way to measure the carrier density and the built-in voltage.

4.3 Depletion region in an organic Schottky contact

The band description is not strictly applicable in organic semiconductors as most of the time there are no bands in organics. As explained in the following paragraphs, a bias dependent depletion region exists in an organic MS contact.

Regardless of the semiconductor energy structure, when a semiconductor material makes a junction with a metal with a different Fermi level, the electrons move from the material with higher Fermi level to the lower one until the Fermi levels align across the junction at the thermal equilibrium. The displaced charges change the balance of charge in the semiconductor and produce a space charge region in the semiconductor. As a result an electric field is established at the junction with which a built-in voltage is associated. The lack of a distinct band structure in the organic semiconductors results in no Schottky barrier ($q\varphi_B$) in organic Schottky contacts. However, the electric field controls the carrier injection from the metal, leading to a built-in potential, which has been represented as a barrier ($V_{bi} = \varphi_{bi}$) [71].

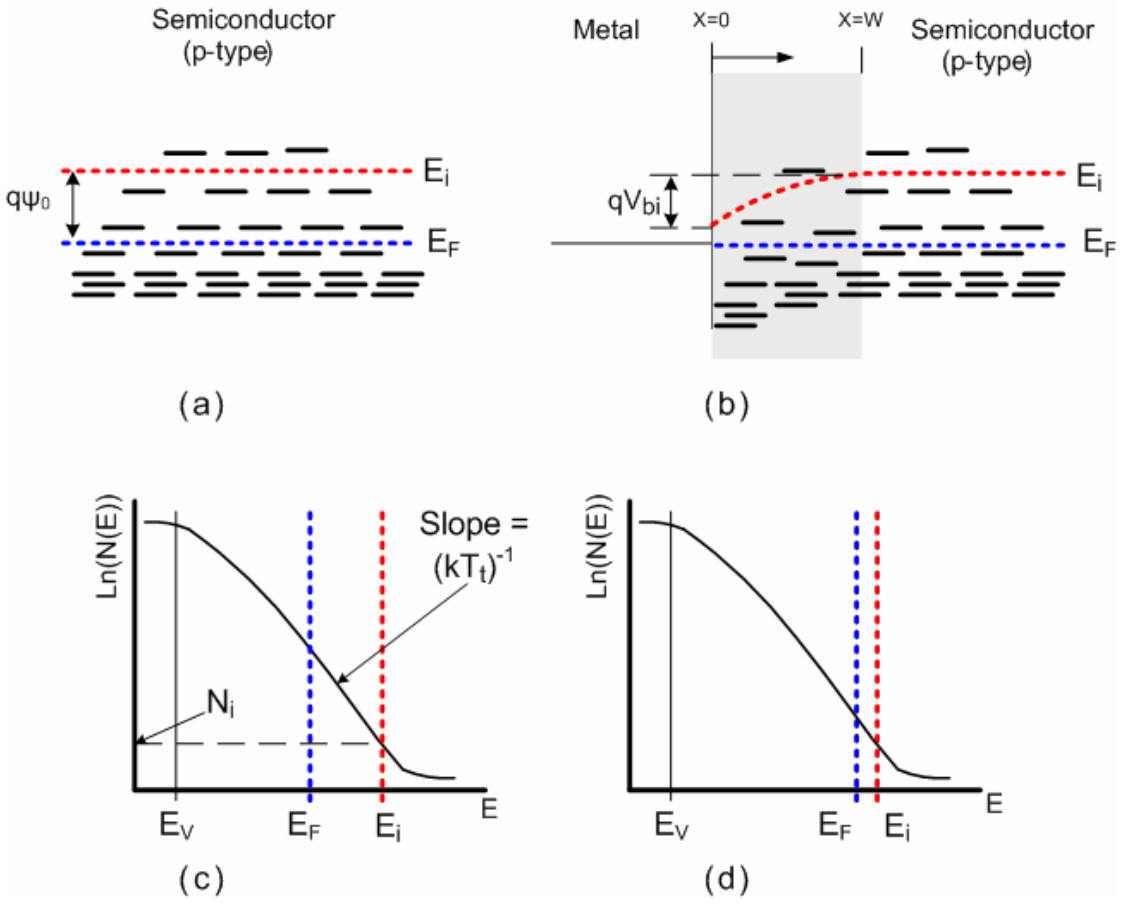


Figure 4.2. The Fermi level in the organic semiconductor (a) before and (b) after a metal junction is formed. The density of states in the organic semiconductor with an exponential tail states and the position of the Fermi level at the surface of the semiconductor (c) before and (d) after the junction.

In figure 4.2 the energy diagram and the density of states in a hypothetical p-type organic semiconductor before and after it makes a junction with a metal are illustrated. The localized states in the semiconductor are shown with dashes and the Fermi level for an intrinsic semiconductor is represented by E_i. In this semiconductor it is assumed that the density of states drops exponentially with the slope of $(kT_t)^{-1}$ in the tail states. When the semiconductor makes a junction with the metal, E_i bends in the depletion region.

The density of carriers in amorphous semiconductors involved in conduction is proportional to the density of states at the Fermi level ($N(E_F)$) [45]. As shown in figures 4.2.c and d, if the density of states at the Fermi level drops when the semiconductor makes contact with the metal, the carrier concentration in the space charge region also drops. The reduced carrier density near the interface effectively forms a depletion region. In other words, if in an organic MS junction the Fermi level moves toward the band tail, a depletion region is produced. Therefore a metal with an appropriate work function creates a depletion region on contact with an organic semiconductor. In non-equilibrium conditions when an external voltage is applied to the junction, the overall voltage (summation of the applied potential and the built-in voltage) determines the charge concentration in the depletion region. Hence, at steady state, the width of the depletion region is dependent on the applied voltage, but it is no longer a square root dependency because the charge density is not constant in the depletion region. Instead the charge density is determined by a combination of the concentrations of ionized dopants and trapped charges in the localized states [44]. In such a case, solving Poisson equation analytically is very complicated. Therefore, it is easier to find the depletion depth using numerical methods.

In practice, junction capacitance measurements at different biases are utilized to measure the depletion width, but the technique is not useful to find the built-in potential and/or the doping density as C^{-2}-V_A is not a linear curve any more, as has been shown experimentally [72].

In order to have an estimate of the depletion depth, Medici 4.0 [54] is utilized as a CAD tool to simulate an organic Schottky diode. The capability of Medici 4.0 to simulate organic semiconductor devices is discussed in chapter 3. The structure of the device is shown in figure 4.3.a. A 400 nm thick organic semiconductor is sandwiched between the anode and the cathode electrodes. The thickness and width of the electrodes are chosen to be 20 nm and 12 µm, respectively. For the semiconductor layer, regioregular poly (3-hexylthiophene) (rr-P3HT) is selected which is a relatively stable p-type semiconductor [73]. Rr-P3HT is widely used to make

various organic devices because it has very high carrier mobility for a soluble (readily processible) organic semiconductor [31]. The semiconductor is defined for Medici as an amorphous semiconductor by applying the density of states close to the valence conductivity edge (E_V). The semiconductor characteristics, which are applied for the simulation, are explained in chapter 3. Since the semiconductor is p-type, gold as a high work function metal ($q\varphi_{Au}$= 5.1eV) [61] is chosen for the anode electrode and aluminium with a low work function ($q\varphi_{Al}$ = 4.28eV) [61] is considered for the cathode. An organic Schottky diode with the similar structure and materials has been already experimentally demonstrated by others [40]. The Medici input code is presented in appendix B.

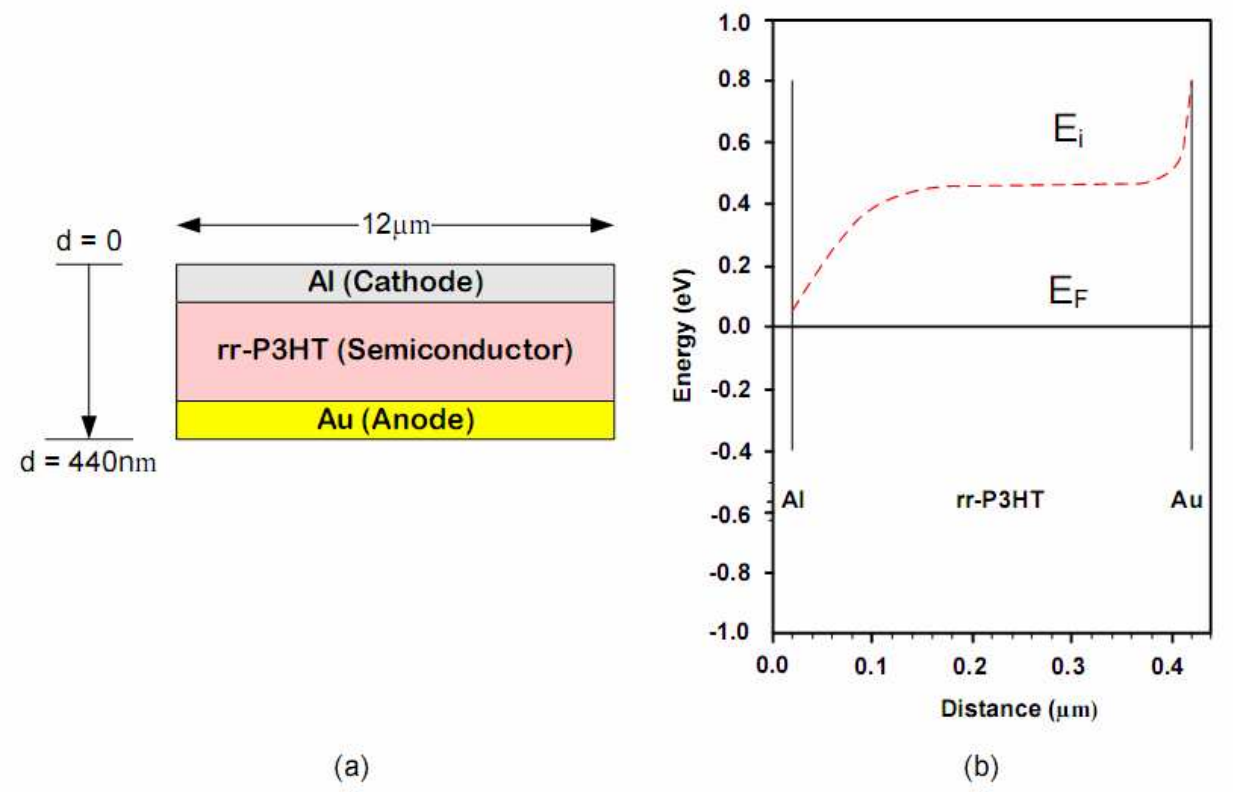


Figure 4.3. (a) The schematic of the simulated organic Schottky diode and (b) the energy diagram at equilibrium.

The downward energy bending of E_i in the semiconductor adjacent to the aluminium contact shows a Schottky contact between the aluminium and rr-P3HT (figure 4.3). The diagram shows that the depletion width is about 120 nm under equilibrium conditions. Upward bending of energy at the gold contact shows that the Fermi level is moved toward the mobility edge (E_V) as a result of the high work function in gold, thereby increasing density of states and conductivity.

If the semiconductor layer is thinner than 120 nm the entire semiconductor between the two electrodes is depleted. In such a case the semiconductor acts like an insulator and the built-in voltage is equal to the difference of the two work functions of metal electrodes [71].

4.4 Current transport mechanisms in Schottky diodes

The current transport in MS contacts is mainly due to the majority carriers [70]. According to the Schottky model for crystalline semiconductors a thermionic mechanism is governing the junction current in the forward bias, in which the current is produced from the carriers that have enough energy to pass over the barrier. The thermionic mechanism is not applicable in organic semiconductors because of the lack of barrier, but nevertheless the model has been used to describe organic devices in many scientific papers [59, 72, 74, 75]. If this model does not hold, then why is an exponential rise in current observed in these devices under forward bias over some of the voltage range? A diffusion based model is proposed here that, when combined with an exponentially changing density of states as a function of energy, predicts an exponential rise in current in the forward bias. This suggestion is new, but has not been proven experimentally. Following the description of the diffusion model other current limiting mechanisms including space charge limited current and ohmic contact are described. These are well accepted models used to describe current in organic MS junctions, and are presented because they are employed later in analyzing experimental results.

The thermionic model is more appropriate for high mobility semiconductors, whereas the mobility is very low in organics. Sze has suggested the diffusion model for low mobility semiconductors [70]. In this model the current in a Schottky contact is determined by the concentration gradient of the carriers in the depletion region [70]. The diffusion model does not rely on energy bands in the semiconductor, making it more promising for describing organic Schottky contacts.

The diffusion model starts with the basic drift-diffusion equation in a semiconductor[1] [70]:

$$J = p\mu \frac{dE_F}{dx} \tag{4.5}$$

[1] The semiconductor is assumed to be p-type for the purposes of the derivation.

where J is the current density, p is the hole density, and the x direction is indicated by the arrow in figure 4.2. b. Often in the tail states, the density of states in an organic semiconductor, $N(E)$, decreases exponentially with energy (see figure 4.2) [46]:

$$N(E) = N_i \exp\left(\frac{E_i - E}{kT_t}\right) \tag{4.6}$$

where N_i is the density of states at E_i and T_t describes the width of the band tail (i.e. it is not strictly a temperature). According to equation 2.6 the hole density can be written as:

$$p = N(E_F)kT = N_i \exp\left(\frac{E_i - E_F}{kT_t}\right)kT \tag{4.7}$$

Substituting equation 4.7 into 4.5 gives:

$$J \exp\left(-\frac{E_i}{kT_t}\right)dx = -k^2 T T_t N_i \mu \cdot d \exp\left(\frac{-E_F}{kT_t}\right) \tag{4.8}$$

Integrating both sides across the depletion region, and assuming that the mobility is not dependent on the Fermi level (MTR model), results in the relationship:

$$J\int_0^W \exp\left(-\frac{E_i}{kT_t}\right)dx = -k^2 T T_t N_i \mu \int_0^W d \exp\left(\frac{-E_F}{kT_t}\right) = -k^2 T T_t N_i \mu\left(\exp\left(\frac{qV_A}{kT_t}\right) - 1\right) \tag{4.9}$$

where V_A is the applied voltage across the junction in the forward bias. To solve the integral on the left side the energy bending in the depletion region has to be formulized. Since the energy bending in organic Schottky contacts is dependent on the doping density and the trapped charges in the localized states, it is difficult to formulize the energy bending. Although the band bending is analytically characterized in crystalline semiconductors, an integral similar to the left integral is simplified by assuming a constant electric field across the depletion region [69]. Generally this assumption is valid when the doping level is so low in the semiconductor that it behaves as an insulator. Applying the same approach for organics, E_i is expressed by (see figure 4.2):

$$E_i = q\psi_0 - qV_{bi} + \frac{qV_{bi}}{W}x \tag{4.10}$$

Substituting equation 4.10 into 4.9 and solving the integral gives:

$$J = \frac{qkTN_i V_{bi}\mu}{W} \exp\left(\frac{q\psi_0 - qV_{bi}}{kT_t}\right)\left(\exp\left(\frac{qV_A}{kT_t}\right)-1\right)/\left(1-\exp\left(-\frac{qV_{bi}}{kT_t}\right)\right) \tag{4.11}$$

In order to compare the characteristics of an organic Schottky diode with a crystalline one equation 4.11 can be written in the following form:

$$J = J_S\left(\exp\left(\frac{qV_A}{nkT}\right)-1\right) \tag{4.12}$$

where J_S is called saturation current density and n is the ideally factor ($n=T_t/T$). Since both W and μ are changing with V_A, J_S is not a constant except for a limited range of the voltage.

The ideality factor is strongly dependent on the slope of the tail in the density of localized states. In many organic semiconductors including rr-P3HT T_t is larger than 300 K [46] which results an ideality factor larger than 1 at room temperature. However, for a highly ordered semiconductor with sharp tail states n might approach to 1.

In addition to the diffusion process, other mechanisms are involved in charge transport in a Schottky contact including tunneling through the interfacial layer and recombination of carriers in the depletion region [69, 70]. The effect of those is usually considered in crystalline semiconductors by increasing the value of the ideality factor in equation 4.12 [70]. In forward bias when $V_A >> kT/q$ the current in an organic Schottky contact is expressed as:

$$J = J_S \exp\left(\frac{qV_A}{nkT}\right) \tag{4.13}$$

In crystalline semiconductors the ideality factor is usually between 1 to 1.6, whereas in organics the range is wider (1.2 to 8) [72].

According to equation 4.12 the current density in the reverse bias is J_S. However, the current does not saturate as J_S changes with the applied voltage.

Similar to a crystalline Schottky diode, breakdown happens in an organic Schottky junction at high reverse bias voltages [59]. Of course, the Zener effect is meaningless in organics because of the absence of bands, but an avalanche process is likely the reason for the breakdown [47].

Equation 4.11 is introduced for the first time and has not been proven experimentally. Further study especially on the current variation with temperature is required to prove or reject the diffusion model, which is beyond the scope of this thesis. Also equation 4.10 is a very poor estimation of the energy bending in the depletion region, which reduces the accuracy of equation 4.11. Nevertheless, equation 4.12 indicates why even in the absence of energy bands in organic semiconductors the current in a Schottky junction might exponentially change with voltage.

4.4.1 Ohmic contact

A metal with a Fermi level close to the mobility edge in the semiconductor can form an ohmic contact by accumulating carriers in the space charge region rather than depleting carriers. Such a case is often used to form ohmic contacts in organic semiconductors [44] as shown in figure 4.3 between gold and rr-P3HT. Also, at very high doping levels the organics have nearly metallic properties [44] and the junction is effectively a metal-metal contact.

4.4.2 Space charge limited current (SCLC) in an organic Schottky diode

Equation 4.6 describes the current at a Schottky junction in the forward bias, but the current might be limited at high values by other mechanisms. Considering the bulk resistance and the contact resistances in a Schottky diode, the applied voltage across the Schottky contact is $V_A=V_{ter}-IR$, where V_{ter} is the terminal voltage, I is the device current, and R is the overall resistance [59]. For a very high current in the forward bias the resistive effect can sometimes dominate and the device then shows a linear I-V curve instead of the exponential one.

Often, in an organic Schottky diode the current at large forward bias is limited by the space charge limited current (SCLC) effect [76]. This limitation occurs when the concentration of the injected carrier in a semiconductor is high compared to the carrier concentration at equilibrium, especially when the mobility of the carriers is low in the semiconductor [77]. In the SCLC regime the current density is expressed by [77]:

$$J = \frac{9\varepsilon_S \mu_b V_A^2}{8d^3} \tag{4.14}$$

where μ_b and d are the bulk mobility and the thickness of the semiconductor, respectively. In the space charge limited regime the mobility can be determined if the thickness of the device is known [44].

In summary, organic Schottky diodes are expected to have a non-linear *I-V* curve. Under forward bias the current is found to follow equation 4.13, with an ideality factor that is relatively large compared to a Schottky diode made of a crystalline semiconductor. At high currents the *I-V* curve deviates from the exponential trend as the current has been found to be limited by either the space charge limited current or the series resistance effects. The reverse current is rarely saturated and the breakdown happens by the avalanche effect in Schottky contacts.

4.5 Fabrication of Organic Schottky diodes

The most convenient way to build an organic Schottky diode is the stack structure shown in figure 4.3.a. The fabrication is done layer by layer. The bottom electrode is deposited and patterned on a substrate, and the semiconductor is deposited over it. The top electrode is then laid down and patterned. As has been explained, rr-P3HT is chosen as the organic semiconductor because of its solubility and high carrier mobility [73]. The anode electrode can be made of any high work function conductor such as gold ($q\varphi_{Au}$= 5.1 eV) [61], platinum ($q\varphi_{Pt}$ =5.65 eV) [61] or indium-tin-oxide (ITO) ($q\varphi_{ITO}$ =4.5 eV) [78]. ITO is widely used for OLED applications because it is a transparent conductor, but it is difficult to pattern it with manual methods because there is no visual feedback in the process. Gold is chosen over platinum based on availability and price. There are several choices for the cathode. Calcium ($q\varphi_{Ca}$ =2.87eV) [61], magnesium ($q\varphi_{Mg}$ =3.66eV) [61] and aluminium ($q\varphi_{Al}$ = 4.28eV) [61] are common metals used to make a Schottky contact with p-type organics. Among them calcium is best because it has the lowest work function, but its junction with organics degrades quickly due to the diffusion of the calcium ions into the semiconductor layer [79]. Also, application of magnesium is challenging due to the reactivity of the metal [79]. Therefore aluminium is used which produces an air stable Schottky contact with rr-P3HT. The simulation result in figure 4.3 suggests that the aluminium work function is low enough to make a Schottky contact with rr-P3HT. Formation of a Schottky contact in Al/rr-P3HT junctions has previously been demonstrated [40].

Generally, in the stack structure the aluminium electrode could be either the top or the bottom electrode, but in the particular way that we are making the device, it is preferred to have the aluminium at the top. The concern is the quick formation of alumina (Al_2O_3) at the surface of the aluminium which behaves as an interfacial layer in the Schottky junction. Deposition of the aluminium in vacuum as the last step of the fabrication reduces the opportunity to form alumina between the electrode and the semiconductor.

To fabricate diodes, gold micro-electrodes, made as explained in chapter 3, are used as the substrate and the anode contacts. On each of micro-electrodes there are four parallel electrodes with lengths of 500 μm, widths of 4 μm and with 4 μm spacing (figure 3.1). Having four electrodes on each sample allowed us to make four diodes in every run which was useful to test the consistency of the measured characteristics.

The cleaning process is a crucial step in making organic devices. Most of the time the organics used during the fabrication process of micro-electrodes (photoresist, acetone and so on) stay on the electrodes as a residue and later they contaminate the organic semiconductor. Different methods including standard cleaning-1 (SC1), washing with acetone and methanol, boiling in acetone and methanol and cleaning in piranha are tested. The piranha recipe, in which the micro-electrode is dipped in a solution (piranha) containing H_2SO_4 (50%) and H_2O_2 (50%) for 5 minutes at the room temperature and washed with plenty of deionized water (DI water), is found more effective than the other methods. Dry nitrogen is then blown over the sample to dry it. Since piranha is a highly reactive solution, the cleaning process has to be done in a fume hood. After cleaning, the sample has to be stored in a clean box and it is found to be best to perform the cleaning immediately before using it for device fabrication.

A solution of the organic semiconductor is prepared by dissolving the polymer into chloroform and sonicating the solution in an ultrasound bath for about 30 min. The polymer concentration is usually between 0.5% and 2% by weight. Generally, a solution with very low concentration results in pinholes in the deposited film and a very high concentration makes the solution viscous, making it difficult to obtain a thin film. The selected concentration range is appropriate for various methods of deposition as is suggested in several articles [12, 40, 80, 81]. Given that the density of chloroform is 1.48 g/cm^3, 7.4 mg to 29.6 mg of rr-P3HT in one millilitre of chloroform gives the desired concentration range.

Either spin coating or dip casting are used to coat the micro-electrode with the organic semiconductor. In the spin coating method, the micro-electrode is loaded in a spinner and a few drops of the solution are dropped over the micro-electrode. Running the spinner for 40 s at a speed of 1000 rpm gives a thin uniform layer of rr-P3HT over the electrode with the thickness of about 120 nm. In the dip casting method, the micro-electrode is dipped into the polymer solution and slowly pulled out at an oblique angle. While the electrode is being pulled out the chloroform evaporates rapidly and the polymer is deposited over the electrodes. Since the method is manual, there is no control over the thickness of the film. Thickness is measured with an atomic force microscope (AFM) after the device is electrically tested. The dip casting method is convenient when a thick layer of the organic semiconductor is required, whereas spin coating produces a relatively thin layer.

After the semiconductor deposition, the sample is heated on a hot plate at 100 °C for 20 minutes to anneal the semiconductor and remove the residual chloroform [82]. A mechanical mask is then put over the sample to apply the required pattern for the aluminium electrode. The sample and the mask are loaded in an evaporator to deposit an aluminium layer with a thickness of between 100 nm and 500 nm. Figure 4.4 is a schematic of the device after aluminium deposition.

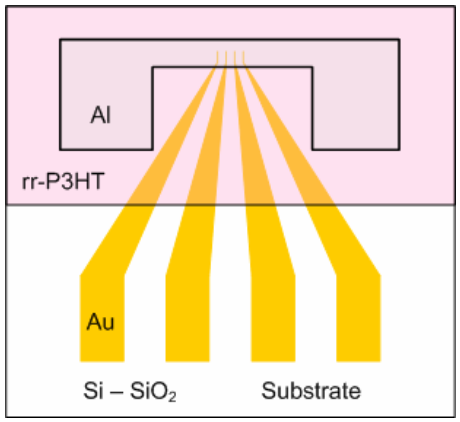


Figure 4.4. A schematic of the top view of the sample after the aluminium deposition.

The aluminium deposition rate is a very important factor in building a diode. To achieve a rectifying junction it is found that the rate has to be less than 1 Å/s. When the rate is higher than 3 Å/s there is often a short circuit between the top and the bottom electrodes, especially when the semiconductor layer is thin. The shorting is probably due to deep penetration of aluminium

into the soft organic layer when aluminium atoms have high kinetic energy in a high rate deposition. For a rate between 1 and 3 Å/s the diode usually shows a resistive characteristic in parallel with the Schottky diode. Such a characteristic is analyzed in section 4.6.1.

Most of the organic semiconductors, including rr-P3HT, are very sensitive to oxygen and moisture [83]. Although, the chemical structure of rr-P3HT is stable in air, oxygen and water molecules behave as dopants in the polymer if they penetrate into the semiconductor layer [60]. Since a Schottky junction behaves as an ohmic contact if the doping density is very high at the surface of the semiconductor [70], minimizing oxygen and water content is important. After the polymer deposition on the micro-electrode, the sample is kept in a vacuum of 10^{-7} torr for more than 8 hours in order to remove oxygen and moisture prior to the aluminium deposition [32]. Although this method does produce Schottky diodes, the device characteristics change after a few days when they are tested in air. In order to reduce exposure to air and moisture many of the devices are fabricated and tested in a glove box filled with dry nitrogen, described in chapter 3. In this case all the steps that involve the organic semiconductor, including opening of chemicals, preparation of the semiconductor solutions, deposition, and the testing of devices, are done in the glove box. An evaporator embedded inside the glove box is used for the aluminium deposition.

Diodes made in air and in the glove box are electrically tested to compare their performances.

4.6 Electrical characteristics

Since a non-ohmic junction in the anode electrode (Au/rr-P3HT contact) would reduce the diode performance, our first concern is ensuring the proper contact between the gold electrode and the semiconductor. To check the junction at the Au/rr-P3HT contact, the current between two adjacent gold electrodes is measured before the aluminium deposition when the voltage is scanned from -3V to 3V. Figure 4.5 shows the ohmic behaviour of the contact with a linear *I-V* curve. The sample used in this test made by dip casting 200 nm of the polymer on the micro-electrode and heating it to 100 °C for 20 min in the glove box. The resistance of 55 MΩ and the conductivity of the semiconductor (σ) is calculated to be 7.2×10^{-6} S/cm.

Since the conductivity measurement between two electrodes may not be accurate because of the contact resistance, a four-point technique is applied by using all four electrodes in the sample. A

very negligible difference is observed between the conductivity measurement with two-point and four-point techniques as the high resistance of the organic semiconductor dominates.

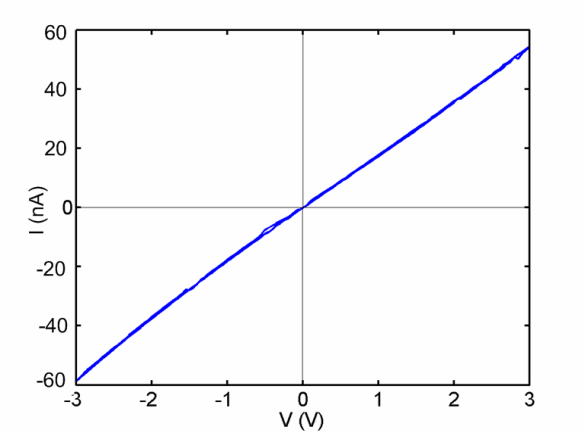


Figure 4.5. The *I-V* curve between two adjacent gold electrodes in a sample with 200 nm thick rr-P3HT and no aluminium layer.

Scanning the voltage back and forth several times gives a consistent *I-V* curve for this sample which is made and tested in the glove box. Testing a sample in air shows a rise in conductivity with time which becomes noticeable after a few minutes. The drift in the conductivity suggests oxygen doping. The measured conductivity for rr-P3HT from the sample in the glove box is taken as the 'intrinsic' conductivity of the polymer. This intrinsic conductivity is relatively high and likely results from undesired dopant (ions) in the polymer primarily left over from the polymer synthesis process [71].

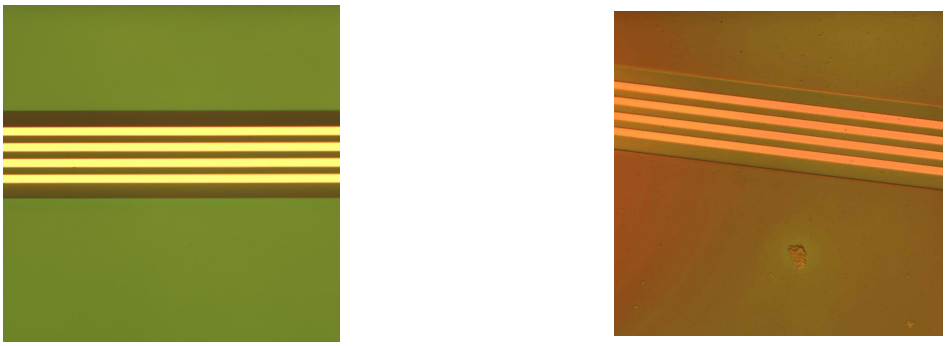
4.6.1 **Air-made organic Schottky diode**

In this section the feasibility of making diodes in air and operating them in air is investigated. It turns out to be a non-trivial challenge because organic semiconductors are known to be air and moisture sensitive, and encapsulating coatings tend to be somewhat permeable to oxygen and water. Much research is focussed on creating new organic semiconductors that are stable in air [84]. The advantage if it works is that manufacturing costs are reduced. The hope was that coverage of the diode (and later the transistor) with the top electrode would provide a barrier to air penetration, with the dense metal providing better protection than a polymer coating. It is discovered that diode characteristics are obtained in air, but the response is time dependent. The

overall conclusion is that the characteristics of the air-made diodes presented in this work are not sufficiently stable for practical application. They do have some interesting characteristics however, as presented at the end of this chapter.

Although the conductivity measurement in air indicates a time dependent *I-V* curve, more stable electrical characteristics are expected in an air-made Schottky diode because of the encapsulation provided by the covering aluminium layer. The idea is to put the air-made polymer coated micro-electrode into a vacuum chamber for a few hours to remove oxygen and moisture and then to deposit the aluminium over the polymer. The polymer should partially undope in vacuum [32]. Then it is encapsulated with the aluminium layer, which works as the cathode as well.

A 1.6% (wt.) rr-P3HT solution is used to make a Schottky diode on a micro-electrode. The solution is spin coated at a speed of 1000 rpm for 40 sec to produce a 120 nm thick polymer layer on the electrode. The thickness is measured with a profilometer. Figures 4.6.a and 4.6.b show the optical images of the tips of the micro-electrode before and after the polymer deposition. The electrode area is coated relatively uniformly and it appears to be defect free.



(a) (b)

Figure 4.6. Optical microscope image of the micro electrode (a) before and (b) after the polymer deposition (the width of each electrode is 4 μm).

The sample is left in a vacuum of 3×10^{-7} torr for more than 8 hours before the aluminium deposition. A 500 nm thick aluminium layer is then deposited with the e-beam evaporation method at an average rate of 5 Å/s. This rate of deposition was ultimately found to be higher than is desirable, as discussed above, but there is a remedy, as will be discussed shortly. The aluminium pattern is applied by use of a shadow mask during the deposition. The DC

characteristic between one of the gold electrodes and the aluminium is tested by a potentiostat (Solartron SI1287 + SI1260) with the sample exposed to air and electrically shielded in a metal box.

The high rate aluminium deposition in the device led to a very resistive characteristic (figure 4.7) when the voltage is scanned from 0 to 0.9 V. Such a low resistance may be due to pin holes in the semiconductor layer produced by the collision of highly energized aluminium atoms during the aluminium deposition. The aluminium filled pin-holes provide very conductive paths between the aluminium and the gold electrodes which results a “short circuit” characteristic. Increasing the applied voltage up to about 1 V leads to a sudden drop in current. Joule heating resulting from the high current densities at 1 V may evaporate the metal and disconnect the paths, similar to the burning of a fuse [85]. As a result the current drops to a very low value and a diode characteristic is detectable with a fresh scan.

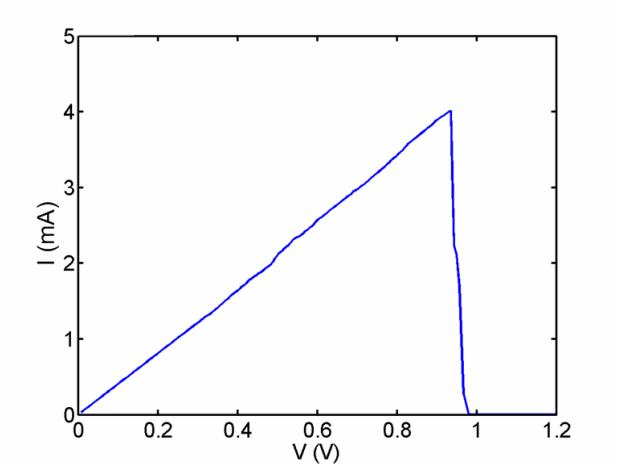


Figure 4.7. The *I-V* curve of a diode with a high rate deposition of aluminium showing the short circuit and burning the shorted paths at high voltages.

Figure 4.8. The optical image of a damaged micro electrode after the burning of the conductive paths in a Schottky diode.

Although, the burning method is useful to recover a short circuited diode, it is not always practical as the burning voltage likely depends on the size and the number of pin holes and sometimes such a large voltage is needed that the diode is damaged. Also, the surface area of the electrode, which is important to know in order to calculate the current density from the measured current, is changed after the burn. Figure 4.8 shows a picture of a damaged gold electrode after the polymer and the aluminium layer are washed off from the sample, suggesting that the area is changed significantly.

After burning the conductive paths the DC characteristic of the diode is tested by scanning the voltage between -3 V and 3 V. Figure 4.9 indicates the rectification property of the diode as the forward current at 3 V is almost sixty times larger than the reverse current at -3 V (rectification ratio ≈ 60 @ 3 V).

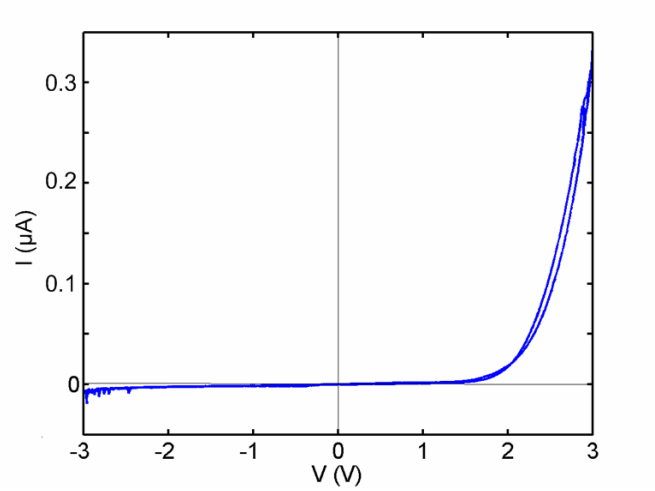


Figure 4.9. The I-V characteristics of an Al/rr-P3HT/Au Schottky diode made and tested in air.

The semi-log plot of the *I-V* curve, figure 4.10, indicates an exponential increase of the current with voltage from 1.5 V to 2.5 V. Least square error estimation is used to fit an exponential function to the measured current in that range (shown as the red line in figure 4.10). An ideality factor of 4.9 and saturation current of 2×10^{-11} A are obtained.

The measured current shows a decline from the exponential growth for voltages above 2.5 V, indicating a limiting mechanism such as the SCLC or bulk resistance. The deviation of the current from the exponential behaviour for voltages less than 1.5 V is studied by looking at the reverse current on a linear scale (figure 4.11). A fairly resistive characteristic is observed down

to -2 V indicating that there may be a resistive path parallel to the Schottky contact with a value of 810 MΩ.

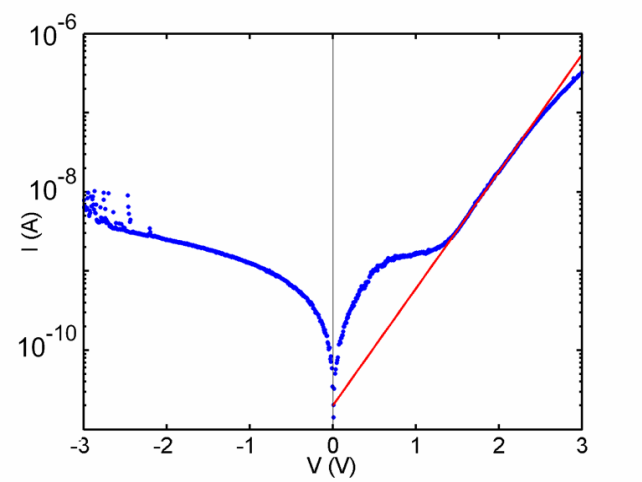


Figure 4.10. The *I-V* curve in a semi-log plot. The red (straight) line is a fit curve to the exponential part of the current.

To explain the DC characteristic of the device a simple model, shown in figure 4.12, is proposed which includes a diode (*D*) and a parallel resistor (R_P). The resistive characteristic is dominant when the diode current is very low in the reverse bias and at voltages lower than 1.5 V in the forward bias, but above 1.5 V the diode current is so large that it dominates the device current.

The time dependence of the parallel resistance is studied by recording the diode characteristic over a two-week interval. These results are presented next.

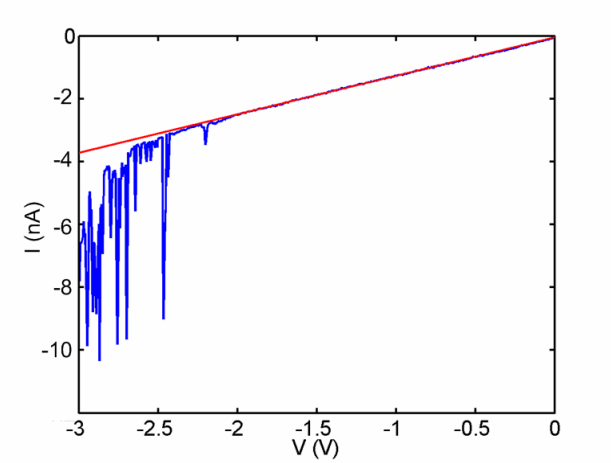


Figure 4.11. The reverse bias characteristic of the diode. The red (straight) line is a fit curve to the current.

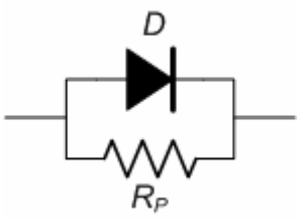


Figure 4.12. The proposed model for the organic Schottky diode.

4.6.1.1 Aging effect in an organic Schottky diode stored in air

Although aging effect has been already studied in organic Schottky diodes, particularly in OLEDs [85-87], the focus has been on the forward bias characteristic which emits the light. For the transistor application, however, the reverse bias characteristic is more important. Therefore the drift in the device parameters is studied over the course of two weeks when the sample is stored in air.

The estimated values of the parallel resistor (R_P), ideality factor (n) and the saturation current (I_S) for the diode are plotted in figure 4.13 at three different times: the day that the device was built (fresh sample), and then 7 and 14 days after fabrication.

The parallel resistance shows a drop with time from 810 MΩ to 17 MΩ, while the ideality factor and the saturation current are increased. The increase in ideality factor, n, suggests a reduction of the diffusion current in the Schottky contact. This might be due to the growth of the interfacial layer between the semiconductor and the aluminium [69]. Formation of an aluminium oxide layer between the aluminium and the semiconductor is very likely if oxygen can penetrate into the device. The burnt conductive paths or pin-holes on the aluminium layer are likely locations for the oxygen penetration.

Although the parallel resistance could be produced from small aluminium particles diffused into the polymer layer (the same particles that may have led to a short circuit), the variation of the resistance with time is not explained with this theory. Instead, the introduction of oxygen may explain both the degradation process in the diode and the drop in the resistance. If oxygen diffuses into the Al/rr-P3HT interface it can react with aluminium and make Al_2O_3 and/or dope the polymer. The former possibility causes the degradation of the diode characteristic and the second possibility can convert a Schottky junction to an ohmic one.

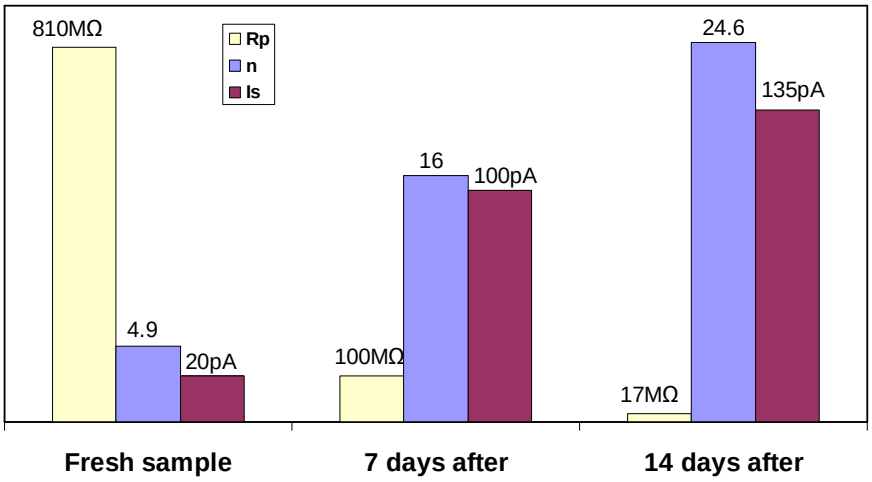


Figure 4.13. The drift of the diode parameters with time in two weeks.

A polymer semiconductor is quite likely to have a non-uniform junction between the metal and the semiconductor. The cartoon in figure 4.14 depicts a highly doped region in the semiconductor which makes an ohmic contact with the aluminium (right), while at left one the lightly doped side a Schottky contact with the interfacial layer is shown. An expansion of the highly doped domains with time is expected as more oxygen diffuses in. As a result the ohmic contact expands and the parallel resistance drops.

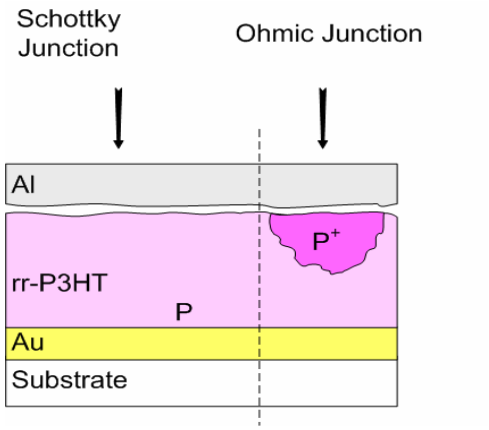


Figure 4.14. Non-uniform junction between the organic semiconductor and aluminium.

The hypothesis of the oxygen effect on the diode characteristic is tested with two experiments. In the first experiment the aluminium is deposited on a polymer film without dedoping the polymer in vacuum. In such a case the polymer which was exposed to air has thus already been doped before making contact with the aluminium. The device showed an almost completely resistive characteristic, indicating that the oxygen doped polymer forms an ohmic contact with

aluminium. In the second experiment, explained in the next section, the diode is built and tested in a glove box filled with an inert gas. The diode showed very slow degradation in its characteristics. Hence, the observed drift of characteristics in the diode is likely due to the exposure to air.

4.6.2 Organic Schottky diode made in an inert environment

4.6.2.1 DC characteristic

In a MESFET transistor the gate contact is a Schottky junction with the semiconductor. Since a very low gate current is desired for a transistor, the gate junction operates either in a reverse bias or at voltages lower than the built-in voltage [70]. Therefore, a Schottky contact with a very low reverse current is required for the gate junction. Also, the Schottky diode breakdown voltage should be high enough not to limit the operational range of the transistor.

The Organic MESFET consists of a pair of the gold micro-electrodes that are used as the drain and source terminals and an aluminium electrode deposited over the semiconductor layer that is used as the gate contact. Considering such a structure, the channel current in the transistor is the current between two adjacent gold electrodes (figure 4.5) which is in the range of 10^{-8} A. Generally the gate current has to be much smaller than the channel current in a transistor. A current smaller than 1 nA is required for the Schottky diode in the reverse bias to build an effective transistor of this design.

The diodes that are made in air have shown poor reverse bias characteristics both in the current range and in the breakdown voltage. However, their forward bias characteristic is reasonably good providing they can be effectively encapsulated. The non-uniform doping at the surface of the semiconductor due to air contamination is a possible reason for the relatively high reverse current. Hence, a nitrogen-filled glove box was used to build and test an organic Schottky diode. A thick polymer layer (250 nm) is deposited (using dip casting) to avoid the short circuit problem in the diode. Also the aluminium deposition rate is controlled to be less than 1 Å/s throughout the deposition. The result is a diode without any parallel conductive path as shown in figures 4.15 and 4.16. A breakdown voltage of higher than 10 V is a significant achievement as most of the organic Schottky diodes have been characterized up to only 5 V in the reverse bias [44].

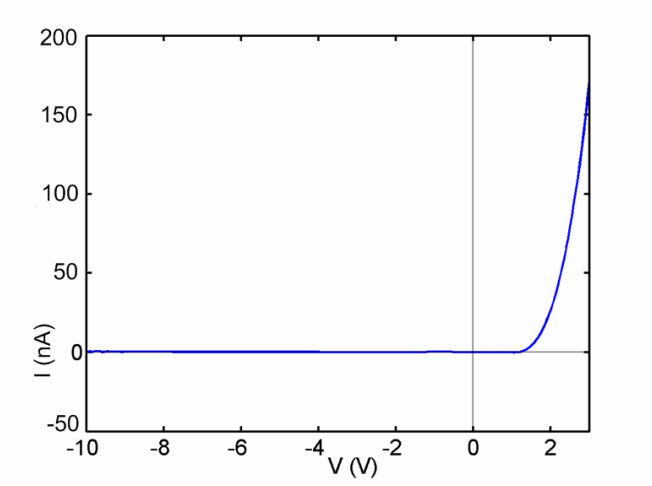


Figure 4.15. The *I-V* characteristic of an organic Schottky diode made in the glove box.

In the forward bias the current increases rapidly with voltage. A rectification ratio of about 250 is obtained at 3 V for the diode, but the current is barely exponential with the voltage. In a very small region, 1.1 V < *V* < 1.8 V, the following exponential function (the red line in figure 4.16) is fit to the experimental data by least squares error estimation:

$$I = 10^{-13} \exp(6.84 \times V) \qquad (1.1V < V < 1.8V) \tag{4.15}$$

where *I* has a unit of A.

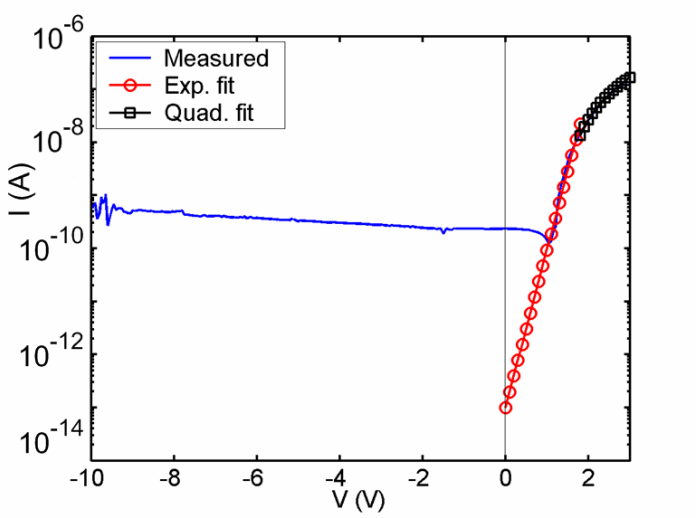


Figure 4.16. The *I-V* characteristic of the diode in a semi-log plot. The red line (○) is an exponential fit in the forward bias and the black (□) line indicates the quadratic function describing the SCLC. The red and black lines form good fits, hiding the experimental data above 1.1 V.

Using equation 4.13 the ideality factor and the saturation current are calculated to be 2.44 and 10^{-13} A, respectively. Both parameters are enhanced in the diode made in the glove box relative to the device made in air.

Above 1.8 V the current is not longer growing exponentially and it mostly follows a quadratic function suggesting space charge limited current. Fitting a second order polynomial equation to the data (black **(□)** line in figure 4.16), gives (*I* has a unit of A):

$$I = (0.6071 \times V^2 - 1.6362 \times V + 1.1113) \times 10^{-7} \qquad (1.8V < V < 3V) \qquad (4.16)$$

Using equation 4.14 the coefficient of V^2 is used to estimate the bulk mobility of the polymer. To convert the device current to the current density used in the equation, the surface area of the gold electrode (4 μm ×500 μm = 2000 μm^2) is used as the junction area. Knowing the polymer thickness (d = 250 nm) and the relative permittivity of the polymer (ε_r= 3) [59] the carrier mobility for rr-P3HT is found to be 1.6×10^{-4} $cm^2/V \cdot s$. The mobility is in good agreement with other experimental data for bulk mobility [53].

4.6.2.2 AC characteristics

Schottky diodes are known as high-speed diodes in crystalline semiconductors because they are majority-carrier devices [70]. The AC properties of the diodes have been studied by measuring their frequency and time responses. Potentially organic Schottky diode can operate up to tens of MHz, as it has been shown before [88]. In this case it is found that parasitic capacitance in the substrate limits the ability to probe the ultimate bandwidth of the device.

4.6.2.2.1 Frequency response

The frequency response of the diode is tested using a Solartron impedance analyzer (SI 1260A) in which one can set a DC bias voltage and apply a small AC voltage. The current is then measured and the real and imaginary parts of the impedance are recorded. To achieve a Bode plot of the impedance for the organic diode, the frequency is swept from 0.1 Hz to 10 kHz. The impedance measurement is done both in the forward bias (V= 2 V) and the reverse bias (V= -2 V) with an amplitude of the AC signal of 20 mV. The results of the measurements are shown in figure 4.17. The plot shows a first-order RC impedance with cut-off frequencies of 20 Hz and 500 Hz for the reverse and forward biases, respectively. A standard parallel RC model for a diode in the AC mode [70] is applicable to calculate the resistance and the capacitance values.

In the model, the resistance (R_d) is representing the slope of the I-V curve at the bias voltage, and the capacitance (C_d) is the junction capacitance due to the depletion region in the Schottky contact.

The results indicate a resistance change from 5 MΩ in the reverse bias to 200 kΩ in the forward bias, while the capacitance is fairly constant at 1.59 nF both in the forward and the reverse biases. The variation of the resistance from high to low values from the reverse bias to the forward bias is consistent with the DC characteristic of the device, but the capacitance is expected to change as the depletion width changes with the bias. Also the cut-off frequencies are suspiciously low, and make the devices useless for many applications. Knowing the electrode area, (4 μm ×500 μm) A = 2000 μm^2, we have calculated the depletion width (W) from the parallel-plate capacitor equation:

$$C = \varepsilon_S \frac{A}{W} \tag{4.17}$$

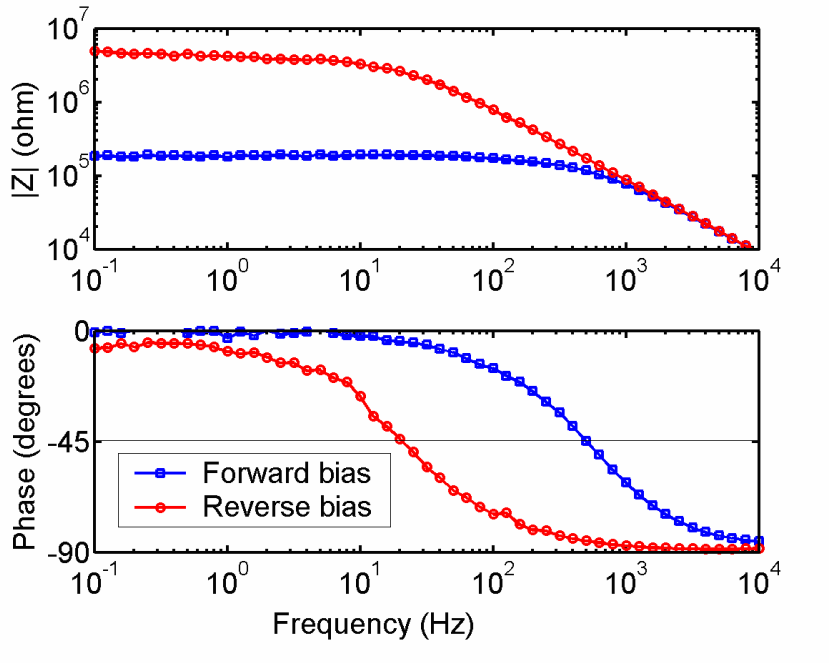


Figure 4.17. The Bode plot of the impedance in an organic Schottky diode. The blue and red curves are the impedances in the forward bias (2V) and the reverse bias (-2V), respectively.

The resulting depletion width is 0.3 Å. Such a depth is even shorter than the bond length between two carbon atoms in the polymer [89], which does not make sense. Therefore, it is likely that a large parasitic capacitor in the device acts as the dominant capacitance.

Although the diode is built on a silicon dioxide layer, underneath of the SiO_2 layer is highly doped silicon which couples to the large gold and aluminium pads. These parasitic capacitors are depicted in figure 4.18. The capacitances between the gold or aluminium pads and the silicon are measured individually by a Fluke multimeter (Fluke 187 DMM) to be: $C_{Au\text{-}Si}$ =2.35 nF and $C_{Al\text{-}Si}$ =5 nF. Since these two capacitors are in series, the total capacitance between the gold and the aluminium electrodes is 1.6 nF which is the same as achieved in the impedance measurement. Such a capacitance is much larger than the capacitance in the capacitance in the diode with a very small area. Therefore, the parasitic capacitance is dominant and the bandwidth is limited by it. To eliminate the effect of the parasitic capacitance the device has to be built either with much smaller pads or using an insulating substrate. The first solution is a change in the photolithography mask and the electrical connection setup that is made for convenient connection in the glove box. The second solution is suggested in chapter 7 for future experiments. Si/SiO_2 substrates were chosen because they can also be used for fabricating OFETs, and device performance can then be compared with organic MESFETs. The details of the OFET and organic MESFET geometry are presented in the next chapter. The frequency response of the diode indicates that the transistors are not expected to work at high frequencies without reducing the parasitic capacitance.

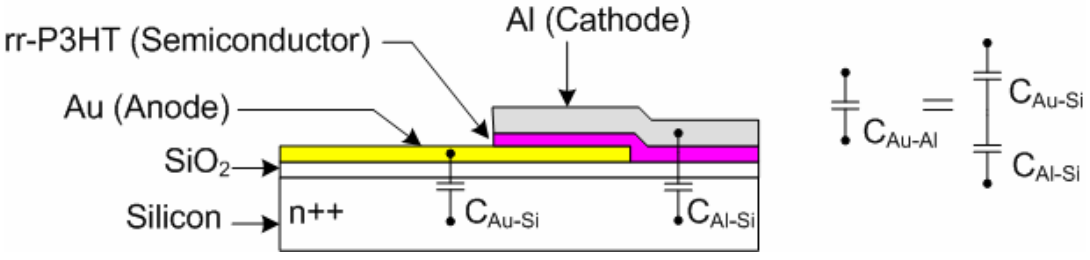


Figure 4.18. The parasitic capacitance between the gold and the aluminium electrodes. The gold/silicon capacitance ($C_{Au\text{-}Si}$) is in series with the capacitance between the aluminium layer and the silicon ($C_{Al\text{-}Si}$).

4.6.2.2.2 Time response

The frequency analyses showed that the device can not operate at high frequencies using the substrate that has been chosen, so the focus of the remaining characterization is on the relatively low frequency characteristics. To study the low frequency response of the diode and the current stability, a pulse sequence is applied to the diode and the current is recorded. A Keithley 6430 is used as a controlled Source-Measure Unit (SMU) to both apply the voltage and measure the current. Because of the sampling rate limitation of the instrument the data can only reliably be recorded approximately every tenth of second. The applied voltage range is chosen such that the diode is tested for transition from the zero bias to both the forward (V=3 V) and the reverse (V=-5 V) biases as well as switching directly from the forward to the reverse biases and vice versa. Two cycles of the applied and measured signals are shown in figure 4.19.

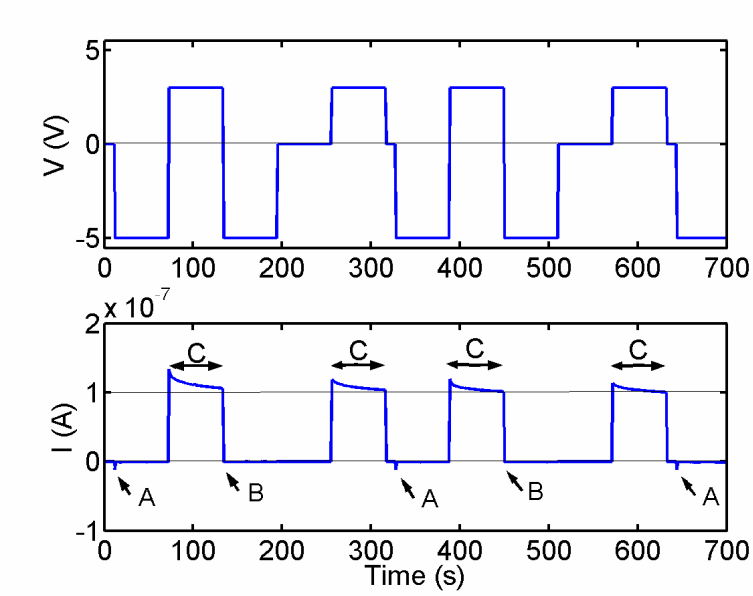


Figure 4.19. The applied voltage to the organic Schottky diode and its current response.

Transition from zero bias to the reverse bias shows a small peak in the current (marked as points A in figure 4.19) that dies off quickly which can be interpreted as the effect of the observed pole at 20 Hz in the frequency response. The transition from the forward to the reverse bias has no peak as points B indicate. The reason is the higher cut off frequency in the forward bias (500 Hz) which results in a much faster response than is detected by low sampling rate of the instrument. In other words, the large parasitic capacitance is charged with a very small reverse current when the voltage is switched from 0 to -5 V showing a small peak and relatively slow

charging. Instead, the large current in the forward bias can charge the capacitance more quickly when the voltage is changed from 3 V to -5 V resulting in no recorded peak at the slow sampling rate.

The most significant change in the current happens when the voltage is switched to 3 V from either 0 V or -5 V. The current shows a slow exponential drop with time to reach an equilibrium value at about 1×10^{-7} A. The time constant (τ), the time that the current value reaches to 63% below the peak, is approximately 17 seconds. It is a sign of a very slow phenomenon that is not accounted for by the parallel RC model used to explain the frequency response.

Although the source of such a low frequency response in organic devices is not clearly known, it is attributed to the effect of the deep traps in the semiconductor [90]. The average relaxation time associated with the traps is represented by τ. The trap time constant is known to reach tens of minutes for deep traps [90]. The effect of traps is usually considered as a series resistor-capacitor (R_tC_t) in the AC model of a diode.

Figure 4.20 depicts an AC model of an organic Schottky diode suggested in reference [91] in which the bulk of the semiconductor is modeled with another resistance and capacitance (R_bC_b). *Rs* represents the overall series resistance, called the contact resistance, due to the connection and electrodes. In this case it is negligible as the measured conductivity in the sample is the same from both the two-point and four-point methods. Usually the time constant of the bulk semiconductor (R_bC_b) is much shorter than the RC time constant associated with the depletion region (R_dC_d). However, the large parasitic capacitance in our device (not represented in the figure) overcomes the effects of C_b and C_d.

Since the relaxation time is dependent on the quasi-Fermi energy, the product value of R_t and C_t changes with the bias. As it is indicated in figure 4.19 the time constant is longer in the forward bias than that in the reverse bias (no trap effect in the reverse bias is observed). Since in a MESFET transistor the Schottky contact is reverse biased, the relaxation time has a minimal effect on the transistor performance, which is an advantage for the organic MESFET approach.

The effect of slow traps in an organic Schottky diode likely results in a secondary effect, that the author has named apparent inductance. This effect was discovered when the air-made diode was tested at a large forward bias. These previously published [67] experimental results and discussions are presented in the next section.

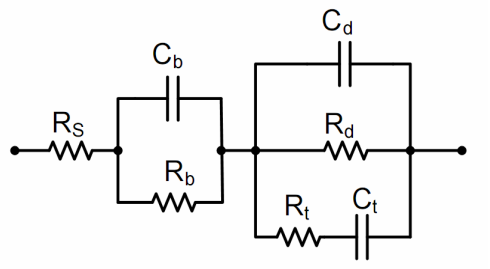


Figure 4.20. AC model of an organic Schottky diode.

4.7 Inductive-like behaviour in organic Schottky diodes at low frequency

In this section a curious and as yet unexplained effect discovered in the course of this work is presented. Current is found to increase in time when a fixed voltage larger than a threshold is applied to an air-made organic Schottky diode. The device is acting as an integrator – one that is not perfectly linear. In order for an inductor to produce a similar effect, it would need to be enormous (mega-Henry range).

The very low frequency behaviour of a diode is of interest in a DC circuit. According to the AC model (figure 4.20) the phase of the impedance is expected to be zero or negative at all frequencies because of the resistive and capacitive elements in the model. Although, the diode might show an inductive behaviour at very high frequencies (leads effect) [92], an inductive-like response is found in the organic Schottky diode at very low frequencies at potentials above a threshold voltage. This effect is observed in diodes made in air similar to the one described in section 4.6.1.

A triangular voltage starting from 0 V with a rate of 50 mV/s is applied using the SI 1287 unit to determine the DC characteristics of the device and the current is recorded with the same instrument. When the amplitude is limited to ±5 V, the forward current is only two times higher than the reverse current (figure 4.21). The very low rectification ratio is mostly due to the parallel resistance effect for the diodes made in air. Although, the rectification ratio can be enhanced by burning the resistive paths, no attempt is made to do that to avoid any process that might affect the device characteristic. The current loop in the forward bias in figure 4.21 indicates the capacitive behaviour. The absence of the loop in the reverse bias indicates the bias dependence of the relaxation time in the diode.

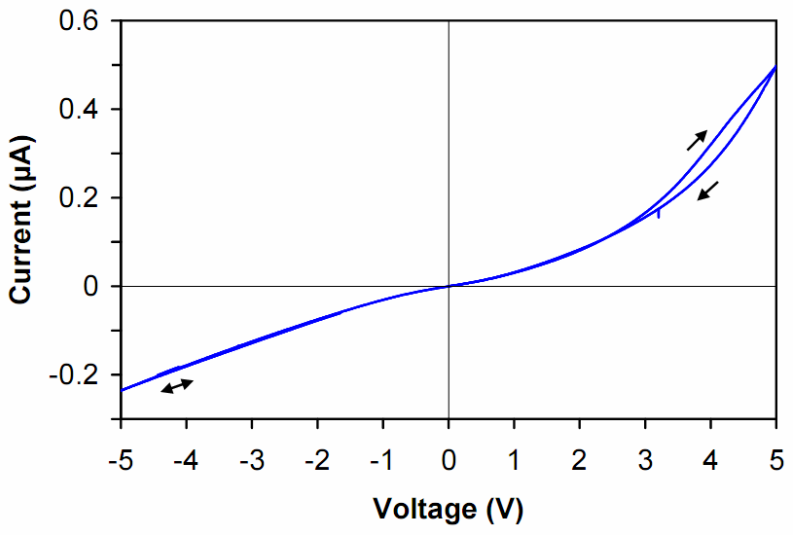


Figure 4.21. The *I-V* characteristic of the organic Schottky diode in the range of ±5V showing a capacitive hysteresis loop.

Increasing the amplitude of the scan voltage to 7 V shows a change in the *I-V* curve (figure 4.22). Although the reverse current maintains its resistive property, a sharp slope appears at voltages larger than a threshold (V_{th}=5.4 V) when the voltage is scanned from 0 V to 7 V. Also the current shows a seemingly inductive hysteresis loop that is not predicted by the AC model. Scanning voltage over different ranges has shown that the inductive loop appears when the voltage is more than the threshold and it is not necessary to scan voltage both in forward and reverse biases.

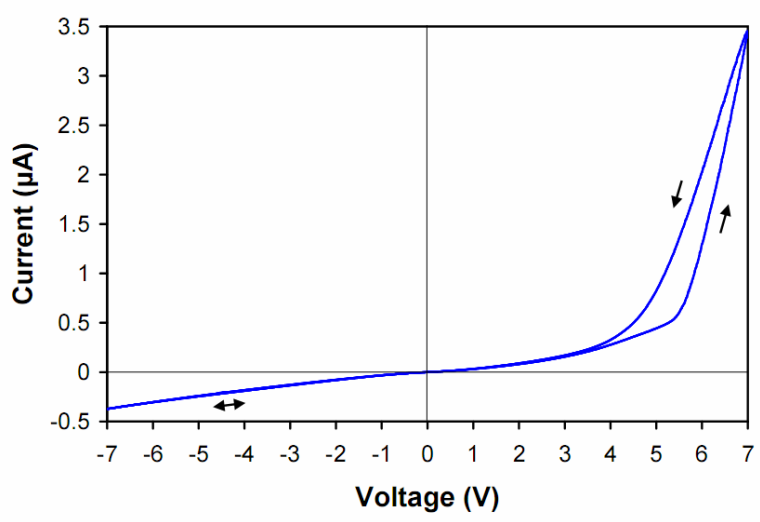


Figure 4.22. The *I-V* characteristic of the organic Schottky diode in the range of ±7V showing an inductive hysteresis loop.

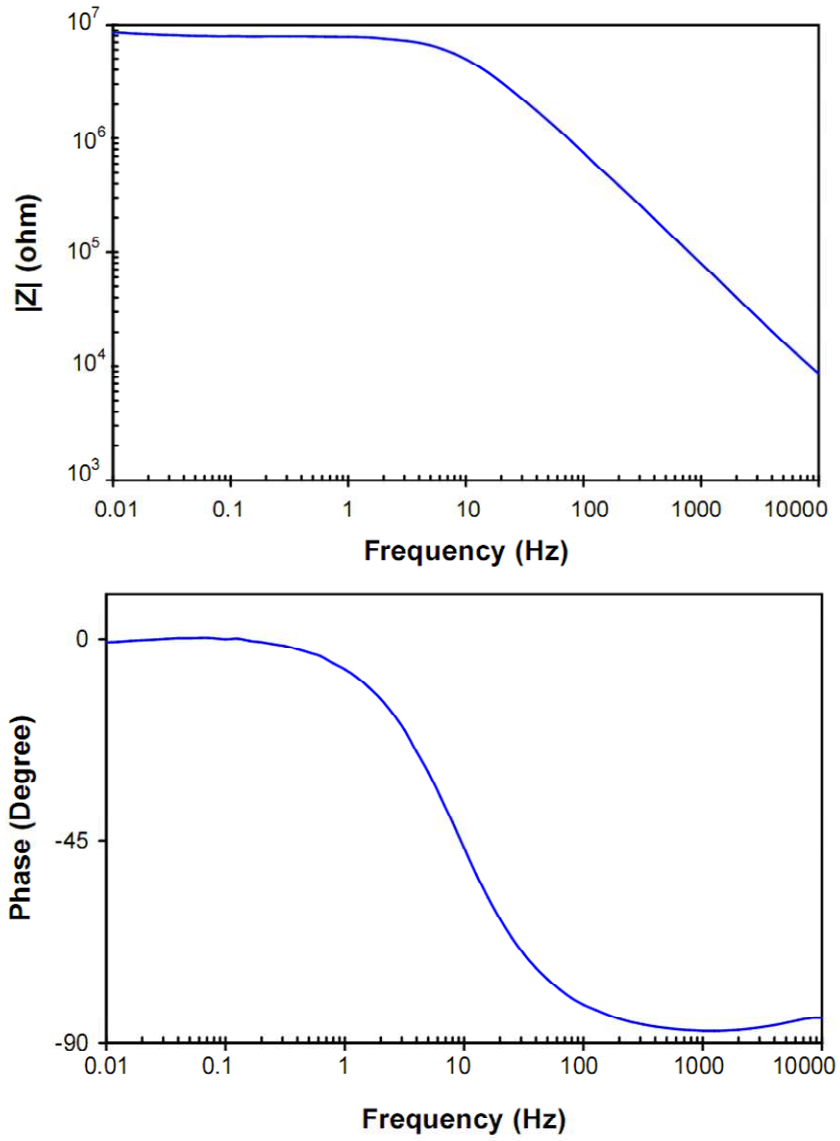


Figure 4.23. The magnitude and phase of small signal impedance of the organic Schottky diode at 4V DC bias.

To study the AC characteristic of the organic Schottky diode the impedance of the device is measured at a number of biases. Figure 4.23 shows the magnitude and phase of impedance at 4 V DC bias, with an AC amplitude of 200 mV. The device behaves as a single pole RC circuit with a bandwidth of 10 Hz. At very low frequency (0.01 Hz) the diode has a purely resistive behaviour.

The Bode plot of the impedance at 7 V bias is represented in Figure 4.24. The positive phase of the impedance at frequencies below 10 Hz is a sign of an inductive-like behaviour. An estimated value of 5 MH is obtained in a parallel RLC model by considering the 3 dB drop in

the magnitude at 0.02 Hz (see arrow) as a new pole with a zero at 0 Hz. However, the absence of the expected phase (45˚) at the proposed pole suggests a more complicated model, which is not considered in this study.

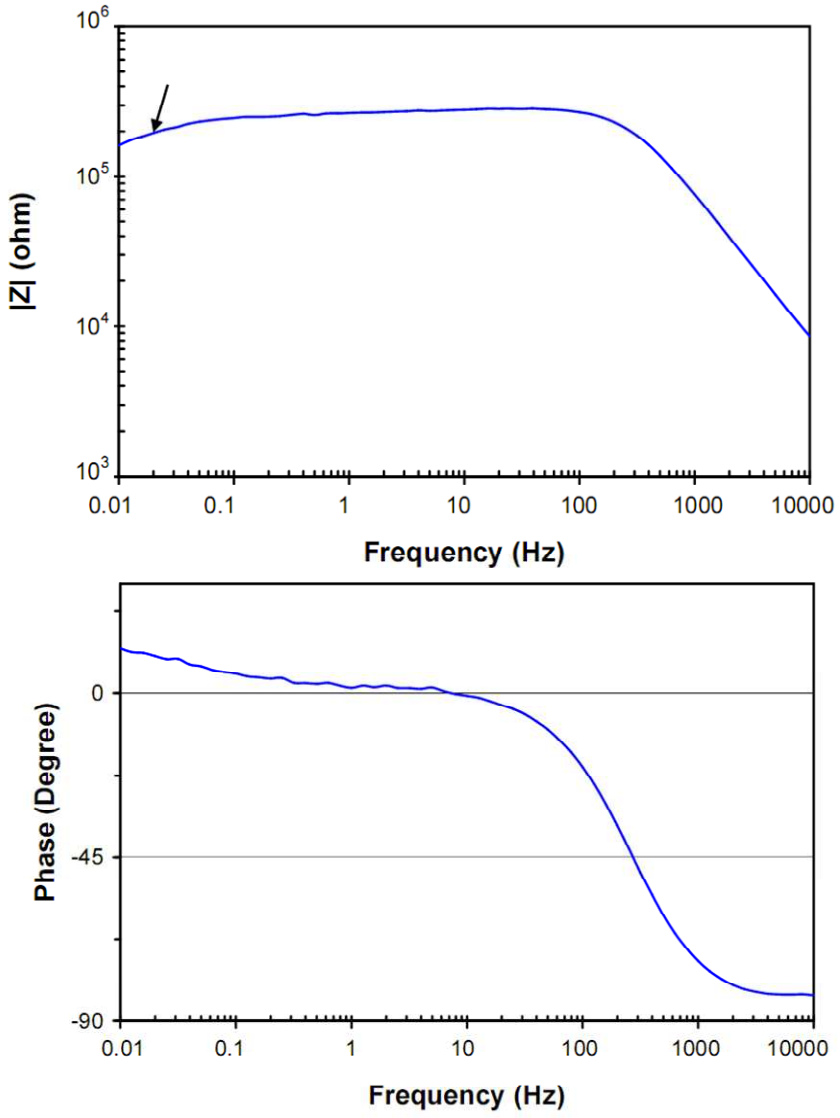


Figure 4.24. The magnitude and phase of small signal impedance of the organic Schottky diode at 7 V DC bias.

Since the effect appears at very low frequencies, the characteristic can be studied by the application of pulses to the diode. Figure 4.25 shows the measured current in response to the applied pulses. When a 5 V pulse is applied from 0 V bias the current settles very quickly to 4.25×10^{-7} A, while the application of 7 V shows a gradual increase in the current that confirms inductive-like behaviour of the junction at large bias. According to the basic inductor equation

(V=L×ΔI/Δt), the apparent inductance (L) is calculated as 860 MH from the slope of the current (ΔI/Δt). An attempt to keep the device at 7 V bias for long enough to observe saturation failed due to a sudden drop of the current, perhaps because of Joule heating induced damage to the device [85].

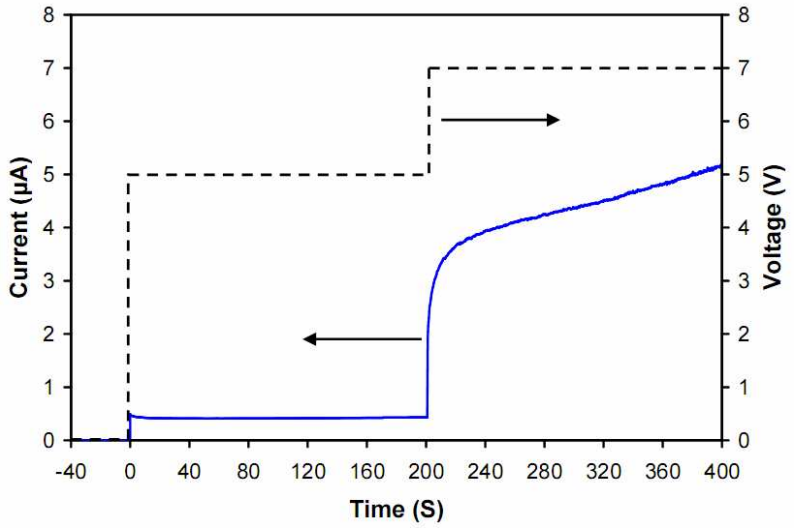


Figure 4.25. The organic Schottky diode current in response to a voltage pulse.

The inductive-like response of the organic Schottky diode is similar to the memory effect in Organic Bistable Devices (OBDs) [93, 94], in which the current shows a loop in the *I-V* plot when the scan range is larger than a threshold voltage. However, the loop in the OBDs is much broader than that in our device. The OBD structure is similar to an organic Schottky diode, except for a very thin (less than 5 nm) aluminium layer deposited in the middle of the semiconductor [93]. Although the mechanism that leads the memory effect in OBDs is not well understood, modeling suggests that it is due to an increase in the transmission probability when charges are stored close to the middle layer [95]. The thin middle layer is producing a potential barrier in the semiconductor. When the voltage is lower than the threshold, the tunneling current through the barrier determines the device current. If the voltage is higher than the threshold, some charges are trapped in the middle layer and form polarized states. As a result of these states the transmission probability and the current increase. A voltage much lower than the threshold has to be applied to release the charges. Such a process predicts a loop in the *I-V* curve of the device when the voltage is scanned back and forth.

Penetration of the aluminium particles into the organic layer during the aluminium deposition in the organic Schottky diode is very likely as discussed earlier. These particles can behave

like the middle layer in the OBDs. Also, the trapped charge in the localized states close to every aluminium particle might cause an enhancement of the current by increasing the transmission probability.

Although the gradual increase in the current in our device is very different from the sudden change in current in the OBDs, the large time constant associated with the deep traps could explain the difference in the time response. Charging of the deep, slow traps in the organic Schottky diode could lead to an increase in the transmission probability by reducing the middle layer barrier thereby increasing the current in the Schottky diode (Figure 4.26). The current increases with time in a positive feedback process as more charge is trapped. The effect is not observed at high frequencies perhaps because of the long relaxation times in the deep states which can not respond at high frequencies.

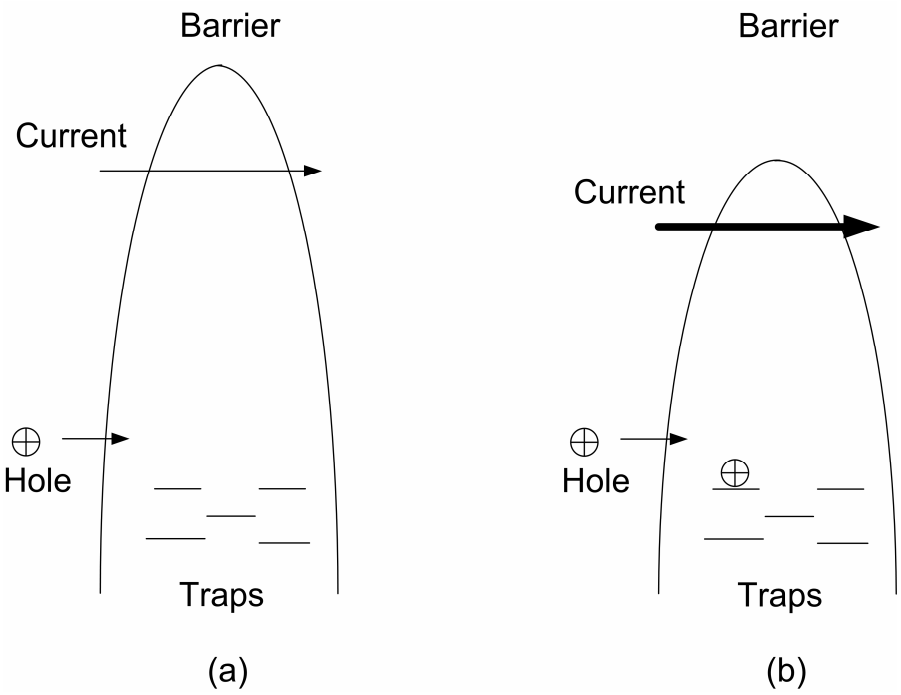


Figure 4.26. (a) The barrier of the middle layer limits the current in the Schottky diode. (b) Trapped charge reduces the barrier and increases the current.

Although the current is lagging the voltage in the diode at low frequencies and high voltages, it is not like a real inductance in the device which does not need any biasing. Producing inductive behaviours through a positive feedback is a common method to simulate inductors in electronic

circuits [96]. For example, a simple circuit shown in figure 4.27.a mimics an RL circuit. As shown in the equivalent circuit (figure 4.27.b) a very large inductance is obtained when the time constant (RC) is very long. Similar to the simulated inductance, the observed inductive behaviour in the organic Schottky diode likely results from a positive feedback mechanism.

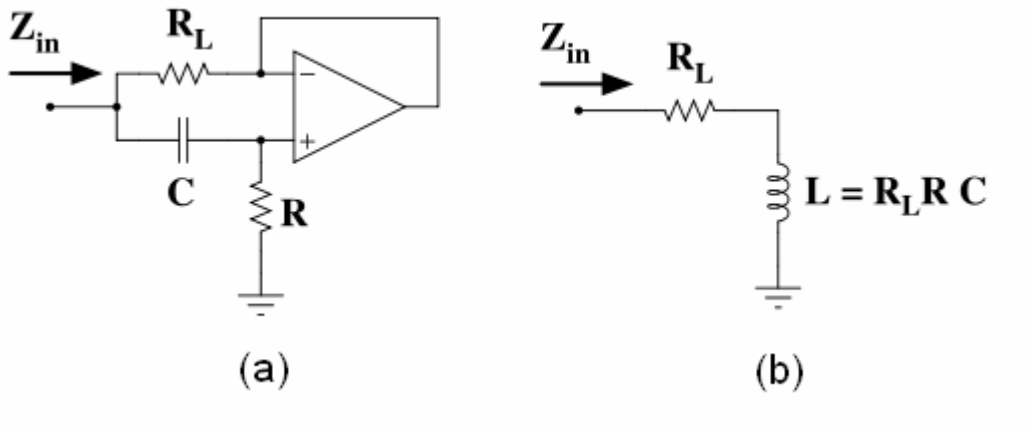


Figure 4.27. (a) Simulation of an RL circuit using positive feedback in the op-amp and (b) its equivalent circuit.

The appearance of the inductive-like behaviour only at very low frequencies and the necessity to bias the diode substantially are drawbacks in applying this inductive-like behaviour for real applications such as filters. Therefore the effect is unlikely to be useful in circuit applications, but it can be studied more to develop the knowledge of organic-metal junctions.

4.8 Summary

The formation of the depletion region in an organic Schottky contact is explained with the energy diagram and the density of states in the organic semiconductor. Also, the current in the organic Schottky diodes is explained by the diffusion mechanism which leads an exponential current-voltage dependence in the device over a certain voltage range.

The DC characteristics of two diodes, one made in air and the other made in a glove box, are presented. The air-made diode showed a resistive behaviour in the reverse bias which is modeled as a resistor parallel to the diode. Degradation of the diode is, then, studied by the drift in the ideality factor, the saturation current, and the parallel resistance over two weeks. The rise in the ideality factor and in the saturation current suggest the growth of an interfacial

layer. The drop in the resistance indicates an increase in the doping level in some regions in the semiconductor. Both effects are likely due to the penetration of the oxygen into the device. The air-made diode does not perform sufficiently well to be used in a transistor since the reverse current is high and drifts with time. The hope of cancelling this drift by applying an encapsulating aluminium gate did not succeed.

A glove box is used to fabricate and test organic Schottky diodes in an oxygen-free environment. The resulting devices achieve a current ratio of 250 with an ideality factor of 2.44. The bulk mobility of the semiconductor is 1.6×10^{-4} $cm^2/V\cdot s$ from the current-voltage characteristic in SCLC regime. The reverse current is less than a nanoampere down to -10 V, which is low enough to build an organic MESFET. The AC characteristics of the diode are investigated through both the frequency and the time responses. The large parasitic capacitance between the anode and the cathode electrodes of the diode has limited the bandwidth to about 500 Hz in the forward bias. The time response showed a very slow drift in the current with a time constant of 17 s at the forward bias, which is likely due to the effect of traps in the semiconductor. The poor frequency response should readily be rectified by changing substrate or using smaller area devices.

Slow charging and discharging of deep traps may be the cause of a secondary effect in the diode current at large biases. In this regime, the device acts somewhat like a voltage integrator with an apparent inductance in the mega-Henry range. An increase in the transmission probability due to the trapped charges is a possible reason for the inductive behaviour.

The low reverse current and the high breakdown voltage of the diodes made in the glove box are sufficient to build MESFET transistors operating at DC. However, the parasitic capacitance is expected to limit the frequency response of the transistor using the substrate geometry chosen for this work. The next chapter describes the theory, fabrication and testing of organic transistors.

Chapter 5

Organic Transistors

Although the application of printing methods is promising for the production of low-cost organic electronics, the performance of the printed organic transistors is usually poor due to the thickness of the deposited layer and the poor molecular order that results from this type of deposition. Also, the voltage range in most organic transistors exceeds 20 V, which is a drawback for widespread application. Solutions have been proposed to reduce this large voltage range, but so far these are not compatible with printing methods. In this chapter the Organic Metal-Semiconductor Field Effect Transistor (OMESFET) is successfully demonstrated as a low-voltage transistor compatible with printing methods. Before discussing the OMESFET, the structure and operation of conventional organic transistors, known as OFETs, are explained, including the challenges of achieving low-voltage operation and reasonable performance using printing techniques. Then, the OMESFET structure is described. To motivate the work, both types of transistor are simulated and their DC characteristics are compared. For a thick semiconductor layer, compatible with printing methods, the MESFET approach shows advantages over the OFET in terms of the voltage range, subthreshold swing and the current on/off ratio [97]. Both types of devices have been fabricated, and again the organic MESFET shows better voltage range than the OFET with a thick layer of the semiconductor [98]. In the devised approach the depletion width in an organic Schottky contact is estimated from the current in the organic MESFET [99]. At the end of this chapter the simulation and experimental results of organic transistors are compared, indicating the circumstances in which organic MESFETs have advantages over conventional OFETs.

5.1 Introduction

Research in organic transistors started seriously in the early 1980s when a group in Japan introduced a polyacetylene based transistor [100]. Although initially the transistor characteristics were very poor, the development of organic semiconductors has brought performance to a reasonable level compared to transistors made from other non-crystalline materials e.g. hydrogenated amorphous silicon (a-Si:H) [18].

The thin-film transistor (TFT) is a well known type of field-effect transistor (FET) utilized in the amorphous semiconductor based electronics. The similarities in the semiconductor properties between amorphous silicon and organics have led to the wide application of the TFT structure in organic transistors. Although a few attempts are reported in which different types of organic transistors are built [19, 20, 101-103], the preponderance of work is devoted to the organic TFT transistors, known as organic field-effect transistors (OFETs).

5.2 Organic Field Effect Transistors (OFETs)

This section provides the background information needed to understand the operation of OFETs and to inform readers of the current state of the art. The description is at a fairly basic level in order that those not intimately familiar with transistor operation may follow the discussion.

5.2.1 Structure and modes of operation

An OFET is basically an Isolated Gate FET transistor (IGFET) in which the gate is isolated from the semiconductor by a layer of an insulating material. Figure 5.1 shows a schematic of an OFET. The drain and source usually make ohmic contacts with the semiconductor. The structure shown in figure 5.1 is known as a bottom-contact OFET, in which the drain and the source electrodes are located between the semiconductor and the insulating layers. When the drain and the source electrodes are on top of the semiconductor, the structure is called top-contact. Depending on the fabrication method, either the top-contact or the bottom-contact is applied, but the operation modes in both are the same.

As in any Metal Oxide Semiconductor (MOS) device potentially there are three modes of operation in an OFET: inversion, accumulation, and depletion. Inversion happens when the applied voltage to the metal is high enough that at the surface of the semiconductor the minority carrier density is higher than the majority carrier density in the bulk (strong inversion). The inversion mode is applied in MOS Field Effect Transistors (MOSFETs) to turn on the transistor. Such an effect is rarely employed in the organics because they mostly behave as a single carrier semiconductor [44]. Instead an OFET is put in the accumulation mode to turn the transistor on. In this mode the gate voltage accumulates the (majority) carriers at the semiconductor-insulator interface, resulting in a high conductance at the surface of the semiconductor. The accumulated layer is referred to as the channel of the transistor. In the channel not only is the carrier concentration higher than the bulk semiconductor, but also the mobility is higher. This is

because of the field effect (see section 2.9). In the depletion mode, the gate voltage repels the carriers not only from the surface but also from the bulk semiconductor, reducing the conductivity of the semiconductor. The depletion mode is applied to turn off an OFET.

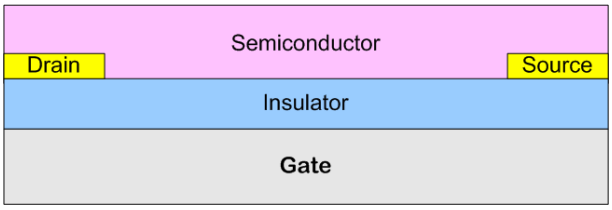


Figure 5.1. A schematic of a bottom-contact OFET.

Similar to any other FET, the OFET shows linear and saturation regimes in its output characteristic when the transistor is on. The current in the linear regime is expressed by [21]:

$$I_D = (\frac{Z\mu_f C_i}{L})[(V_{GS} - V_T)V_{DS}] \qquad (V_{GS} > V_T) \& (V_{GS} - V_T > V_{DS}) \tag{5.1}$$

where I_D is the drain current, Z is the channel width, L is the channel length, μ_f is the field-effect mobility, and C_i is the capacitance per area between the semiconductor and the gate. V_T is the threshold voltage and V_{GS} and V_{DS} are the gate-source and the drain-source voltages, respectively.

In the saturation regime the drain current follows a quadratic function of the gate voltage [21]:

$$I_D = (\frac{Z\mu_f C_i}{2L})[(V_{GS} - V_T)^2] \qquad (V_{DS} > V_{GS} - V_T) \tag{5.2}$$

The equations are very similar to those in a MOSFET transistor [104], but the mobility and the threshold voltage in an OFET are different from those in a MOSFET in some aspects. μ_f increases significantly with an increase in V_{GS} in OFETs [44] whereas the mobility in a crystalline MOSFET has shown a small reduction (by factor of ~0.5) with the gate voltage [55]. More precisely, μ_f is a function of the density of carriers at the surface of the semiconductor [35]. Since, in the on mode the Fermi level at the semiconductor surface is moved toward the mobility edge, the carrier density and the mobility increase. The closer the Fermi level is to the mobility edge, the higher the mobility is [105]. How fast the mobility changes with the gate

voltage depends on the distribution of the density of states in the semiconductor. In a steep band tail the change in the mobility is faster than in a broad band tail.

The threshold voltage in OFETs is also different from that in MOSFETs. Although most of the time the threshold voltage in an OFET is introduced as the gate voltage at which the carrier density at the surface of the semiconductor is doubled [21], in practice the measured threshold voltage does not always match this definition. The reason is that an OFET turns on when the field-effect mobility at the threshold voltage is much higher than the bulk mobility [106], and this does not necessarily happen when the surface carrier density is doubled. Therefore, the threshold voltage is determined in practice by the voltage intercept of an asymptote to the I_D-V_{GS} curve in the linear mode [21]. Sometimes the $\sqrt{I_D}$-V_{GS} curve in saturation is used to obtain V_T [21], but it will be shown in the next chapter that using the linear regime is more accurate because of the parasitic effects.

Although equations 5.1 and 5.2 are widely used to characterize OFETs in the accumulation mode, OFET behaviour is seldom analyzed in the depletion mode [21]. Similar to the depletion mode in a MOS device, a depletion region is produced in the semiconductor when the gate voltage is less than the threshold voltage in an OFET. Such a region reduces the effective cross section of the semiconductor between the drain and the source contacts in the OFET. The drain current drops as the width of the depletion region increases. Application of a small, or in some cases a reverse, voltage to the gate can extend the depletion region through the semiconductor thickness, which turns off the transistor. Sometimes the polarity of the turn-off voltage (V_0) might be different from the threshold voltage (V_T) [12]. For example, using a p-type organic semiconductor to build an OFET, a negative voltage has to be applied to the gate in the accumulation mode to form the channel in the transistor ($V_T < 0$ V), while a positive gate voltage repels holes from the semiconductor to deplete the region between the drain and the source contacts ($V_0 > 0$ V). If the gate electrode is chosen from low-work function materials, the flat band voltage helps to produce a depletion region at zero gate voltage. In the case that the semiconductor layer is thin enough to be fully depleted at zero gate voltage, there is no need to change the polarity of the gate voltage to switch between the on and off modes in an OFET.

Understanding the depletion mode is of great assistance in characterizing OFETs both in the off mode and the subthreshold regime. The only model available for OFETs in the depletion mode is proposed by Horowitz [50], in which it is suggested that the OFET behaviour resembles a

MESFET characteristic. This model is proposed despite the fact that the structure of a MESFET is different from that in an OFET due to the absence of an insulating layer in the former. (The structure and the operation of a MESFET are explained in section 5.3.)

In the Horowitz model the depletion region of the OFET is considered to be a capacitor with the capacitance of $C_d=\varepsilon_S/W_d$ (figure 5.2), where ε_S is the permittivity of the semiconductor and W_d is the depletion width. Since this capacitor is in series with insulator capacitance, C_i, the gate voltage is divided between the two capacitors, as depicted in figure 5.2, with a ratio of the inverse of their capacitances. The voltage which drops across the depletion region is considered as the voltage in a Schottky contact. Using equation 4.3, that describes the depletion width versus the voltage across the metal-semiconductor junction in a uniformly doped crystalline semiconductor, Horowitz has obtained an equation to calculate the depletion width in an OFET at any given gate voltage [44]. Furthermore, he has characterized the current in the depletion mode by using a MESFET current and he has introduced an equation for the turn-off voltage (or pinch-off voltage) [44].

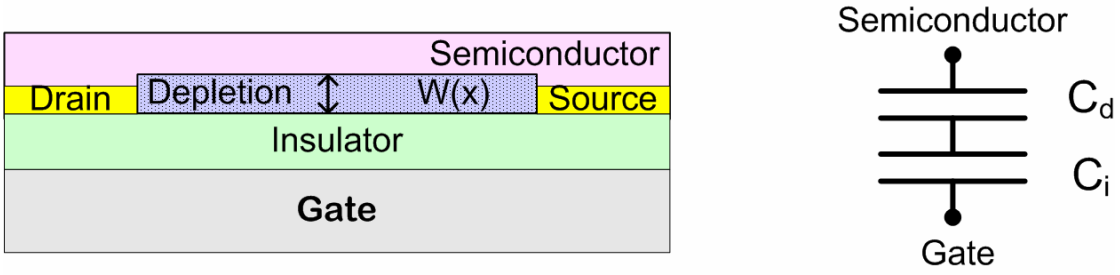


Figure 5.2. A schematic of the depletion layer in the OFET when V_{DS}=0 V and the capacitive model of the transistor in the depletion mode.

Although the voltage division between the two capacitors and modeling the depletion mode as a MESFET device are very valuable in analyzing OFET behaviour [21], Horowitz's analytical models are seldom used to explain the subthreshold current and the turn-off voltage in an OFET. The reason is that the equations are not applicable in an organic semiconductor because they are derived from equation 4.3 which is used in crystalline semiconductors. As is explained in chapter 4, the width of the depletion region in an organic Schottky contact strongly depends on the density of states in the semiconductor [44] and a numerical simulation is usually the best way to calculate the width for a given density of states.

5.2.2 **Challenges in the OFETs**

Increasing the mobility and reducing the operational voltage range are two major challenges in the OFETs. Some other aspects of the transistor performance such as the switching speed and the on/off current ratio are of concern as well. These properties improve as the mobility is increased. Although enhancing the mobility is not the concern of this research, in this thesis the effect of mobility on the transistors performance is frequently mentioned. The reason is that the field-effect mobility employed in OFETs is different from the bulk mobility in the OMESFETs and some of the parameters in the transistors including on current and conductance are strongly dependent on the value of the mobility in the device. Understanding the difference between the mobilities and the methods, which can increase each of them, are keys to enhance the performance of each transistor. Therefore, first the effect of mobility on the transistor performance and the challenges involved in increasing the mobility are explained. The required voltage for driving an OFET is then discussed along with the solutions that are proposed for reducing the voltage range – in particular the use of a direct metal semiconductor contact at the gate.

5.2.2.1 Field-effect mobility in OFETs

The early OFETs had very poor field-effect mobility (~ 10^{-6} $cm^2/V{\cdot}s$) due to the disordered molecular structure of the organics [18]. The low mobility limits the performance of OFETs as the on current, the on/off current ratio and the speed are dependent on the mobility.

a) The effect of mobility on the transistor current

Equations 5.1 and 5.2 indicate the effect of the mobility on the drain current of an OFET. The mobility appears as an amplification factor in the drain current. The higher the mobility, the higher the current is in the transistor. As a comparison the mobility of holes in a p-type silicon is about 400 $cm^2/V{\cdot}s$ at a doping level of 10^{16} cm^{-3} [107], whereas the best field-effect mobility achieved in small molecule organics is about 35 $cm^2/V{\cdot}s$ [30] and in soluble organics it reaches 0.12 $cm^2/V{\cdot}s$ [31]. Although the field-effect mobility in organics is at least one order of magnitude lower than that in crystalline semiconductors, it is in the same range as that in the hydrogenated amorphous silicon (a-Si:H) [21], and thus similar device applications are being considered for these technologies.

Also, the transconductance and the output conductance are linearly dependent on the mobility. By definition the transconductance (g_m) is the slope of the I_D-V_{GS} curve at a constant drain voltage [21]:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{5.3}$$

The output conductance (g_o) is expressed as [49]:

$$g_o = \frac{\partial I_D}{\partial V_{DS}} \tag{5.4}$$

Since the transconductance describes the gain of the transistor, a high field-effect mobility in the organic semiconductor increases the gain in the OFET. Also, when the transistor is used as a switch a high output conductance is expected from the OFET, and again availability of high mobility materials improves response.

b) The effect of mobility on the speed

To achieve high switching speeds the mobility is a limit as it determines the drift velocity of carriers in the semiconductor. According to the Drude model [108], the drift velocity in a conductor (v_d) is proportional to the applied electric field ($\mathcal{E}$), where the constant of proportionality is defined as the mobility (μ). Application of V_{DS} across the drain-source contacts in an OFET with a channel length of L, gives:

$$v_d = \mu\, \mathcal{E} = \mu \frac{V_{DS}}{L} \tag{5.5}$$

In order to form an accumulation layer in response to the switching of the gate to a voltage above the threshold, the carriers injected from the source terminal move all along the channel to reach the drain contact. Therefore, the minimum time needed for switching of the transistor is $t_m = L/v_d$ or [109]:

$$t_m = \frac{L^2}{\mu \cdot V_{DS}} \tag{5.6}$$

Equation 5.6 suggests increasing the mobility to increase the switching speed in an OFET. The effect of the channel length is also important in high-speed applications. However, organic

transistors are much slower than silicon MOSFETs (of the same channel length) because of the lower mobility in the organics. Therefore, organics are not suitable for high-speed applications such as advanced microprocessors.

c) The effect of mobility on the current ratio

To use OFETs in logic circuits the transistors should work like switches. In an ideal switch no current passes through when the switch is off. However the off current is not zero in a transistor. In such a case, the current ratio between the on and off states is used to evaluate its performance. In the next chapter an equation (equation 6.10) is introduced in which the parasitic resistance in the OFETs is used to calculate the current ratio. Also, other expressions are available for specific cases such as very lightly doped semiconductors or very small C_i [44]. In all of them the current ratio increases with increases in the field-effect mobility.

In summary, the mobility is a very important parameter in the transistor performance. Since OFETs conduct the carriers through the channel the mobility in the channel (not the bulk) has to be enhanced to affect the transistor characteristic. The channel in OFETs forms at the surface of the semiconductor adjacent to the insulator within a depth of a few molecules [110]. Therefore, the molecular order of the first few mono-layers of the organics (on top of the insulator) has a significant effect on the field-effect mobility. To produce a well ordered layer of an organic material on an insulator the molecular structure of both the semiconductor and the insulator are important, as is the fabrication method and the roughness of their surface [18].

Pentacene molecules are found to form a highly ordered structure when deposited on a SiO_2 layer, and using this procedure a few groups have built OFETs with high field-effect mobilities (above 1 $cm^2/V{\cdot}s$) [11]. The challenge in the application of pentacene or other small molecules is the expensive fabrication method. To deposit a layer of pentacene a high vacuum chamber with a precisely controlled thermal source is necessary to evaporate the organic semiconductor and deposit it on the substrate. Also, the use of thermal evaporation limits the area of the deposited film to the size of the chamber. Furthermore, pentacene forms a well ordered layer only if the insulator is a crystalline material [11]. Since, the molecular order at the semiconductor-insulator interface is important, a very clean and smooth insulator has to be used. Such expensive methods with limited choice of insulator material provide no cost advantage over amorphous silicon based TFTs [21]. Soluble organics, which can be deposited with low-cost methods over large areas, offer the opportunity to make electronic truly low in cost.

As has been mentioned in previous chapters, among solution processible organics rr-P3HT has shown the highest field-effect mobility. The best quality rr-P3HT has a field-effect mobility of 0.12 $cm^2/V{\cdot}s$ [31] obtained from spin coating of the polymer over a SiO_2 substrate. The rr-P3HT mobility is close to that in the amorphous silicon (~ $1cm^2/V{\cdot}s$) [21]. In this thesis all work presented employs rr-P3HT as the organic semiconductor. It is a relatively well characterized material, and suits the focus of the work presented here, which is the investigation of device structures suitable for low-cost fabrication methods. Substantial research efforts are focussed on designing new processible organic semiconductors with higher mobilities, and on improving the processing of existing ones, in order to improve performance. As these materials emerge they may be used in place of rr-P3HT in order to improve device characteristics.

5.2.2.2 Operational voltage in OFETs

The voltage range in most of the prototype OFETs reported is more than 40 V, and sometimes to reach optimal performance the voltage is 100 V [18]. High voltage limits the application of organic electronics because of both the power supply challenges and safety issues. Also, such a high voltage increases the power consumptions in the electronics. Although the a-Si:H TFTs, used to drive LCDs, also operate at high voltages [21] (typically 20V), most of the applications for organic electronics, such as RFID tags, active matrix displays (AMDs) and OLED displays, are best implemented using low voltage operated transistors. This section describes why high voltage is needed and how others have attempted to reduce it.

The wide voltage range used in OFETs results mainly from the large subthreshold swing. Since in digital applications a transistor with a high on/off current ratio is preferred, the gate voltage has to be sufficiently below the threshold voltage to turn off the transistor effectively. For a transistor in which the subthreshold swing is large, the turn-off voltage, V_0, is far below the threshold voltage, V_T, and can even have different polarity than the threshold voltage [12]. The subthreshold swing in the crystalline FET transistors is usually less than 80 mV/decade [92], whereas it is typically about 7 V/decade in OFETs [52]. The large subthreshold swing in OFETs results from the fact that the drain and source electrodes are making ohmic contacts with the semiconductor. The drain current in the subthreshold regime is dependent on the bulk resistance. In order to achieve a low subthreshold swing a thin semiconductor layer with low bulk conductivity is ideal, along with the maximum possible capacitance across the insulator.

How thin should the semiconductor layer be? In reference [12] an OFET with a 50 nm thick low doped rr-P3HT layer required a voltage range of 80 V to achieve an on-off ratio of 10^6. This example uses a solution-processible polymer, but despite using a layer thickness that is too thin for current printing applications, the voltage is still too high. Simply making the semiconductor layer thinner in order to improve performance is not an option if printing methods are to be employed.

This leaves two ways to increase the control of W with V_{GS}: increasing C_i and/or reducing the density of localized states in the semiconductor layer. The former increases the fraction of V_{GS} which drops across the depletion region (two capacitors in figure 5.2) and modulates the depletion width more effectively. The second solution reduces the density of trapped charge in the depletion region and allows larger variation of W with the voltage across the depletion region. In order to reduce the density of trapped charge the molecular order has to be improved not only at the surface but also in the entire thickness of the semiconductor film, and/or the purity needs to be increased. Both of these approaches favour the use of highly controlled deposition methods rather than printing techniques. Due to these considerations the focus has been on increasing C_i to reduce the subthreshold swing.

To have an idea of how large the gate capacitance should be in order to produce good subthreshold swing, data from Sirringhaus [12] is used. He has reported the highest mobility and current ratio in an OFET made of a solution-processible conjugated polymer (rr-P3HT). In his experiment SiO_2 is used as the insulator in the OFET with the gate capacitance of 15 nF/cm^2. To obtain six orders of magnitude change in the current, the gate voltage is changed by about 80 V. To reduce the voltage range to about 5 V, the gate capacitance has to be increased by a factor of 16 to 240 nF/cm^2. Using silicon dioxide with a relative permittivity of 3.9, the thickness of the insulator has to be about 14 nm to obtain such a capacitance. Production of such a thin layer with a low-cost method is a major challenge, especially when a low-leakage current is demanded. Although in state of the art integrated circuit technology a defect-free layer of SiO_2 as thin as a few nanometers can be produced by a thermal growth method on a silicon substrate [111], the method is too expensive for low-price organic products. Also, the method is restricted to use on a silicon substrate (or gate), while a flexible substrate is preferred in the organic electronics.

Application of high dielectric materials is another means of increasing capacitance. The idea was tested by a group at IBM who applied barium zirconate titanate (BZT) as the gate insulator in an OFET [18]. They have demonstrated a pentacene based transistor working at 4 V with a 120 nm thick insulator. However, the mobility and the current ratio are much lower than when silicon dioxide is used as the dielectric. The mobility is reduced because the molecular order of pentacene on BZT is not as good as that on SiO_2. Also, the dielectric strength of BZT limits the gate voltage to 4 V for that thickness, which leads to a relatively low current ratio [18]. Finally, the sputtering method used to deposit BZT is not a low-cost production method. As a low cost alternative for creating high capacitance, scientists at Motorola have mixed high dielectric nanoparticles in a cross-linked polymer to make dielectrics with a permittivity of 35 [112]. However, the size of particles (1000 nm) limits the insulator layer to be relatively thick so the capacitance is not much higher. As a result, this approach has so far not reduced the voltage range in the transistor [113].

The most promising method to reduce the voltage range is to apply thin organic dielectric layers with low-cost deposition methods [65]. By developing crosslinked polymer-blends for use as insulators, scientists at Northwestern University have demonstrated OFETs with voltage ranges of less than 5 V [65]. The relative dielectric constant in the organic insulators is typically less than 8. A spin coating method is applied to produce a defect free 20 nm thick layer. Such a combination results in a 300 nF/cm^2 capacitance at the gate in an OFET, which is sufficient for low voltage operation. Similar to the application of BZT, the mobility and the current ratio in the OFET with the organic dielectric are lower than those in the OFET with SiO_2. In addition spin coating is not compatible with roll-to-roll production and neither is it readily applicable to very large area devices (e.g. large displays). Other methods such as printing and casting are not appropriate for depositing such a thin (20 nm) defect-free layer.

The solutions proposed for reducing the voltage range are not yet appropriate for cheap and large area production, particularly for a roll-to-roll process. In general, the material thicknesses and the molecular structure of the layers have to be precisely controlled to achieve a reasonable performance in OFETs, while the interest is to print electronics as easily as newspapers. In addition, OFET characteristics are very dependent on the roughness of the semiconductor surface. Since the depth of the accumulation layer is only 2-3 nm [110], a roughness more than 3 nm at the semiconductor-insulator interface causes discontinuity in the channel, which leads to

a poor mobility. Therefore, a very flat and clean substrate is required for effective OFET fabrication, which it makes the fabrication process more challenging for flexible electronics.

As a solution to reduce the voltage range in low-cost organic transistors I propose the MESFET structure. The metal-semiconductor junction used at the gate produces a low voltage junction. As will be seen, in this structure the performance depends on the bulk semiconductor properties. It is appropriate for use with methods that produce relatively thick layers of deposition and is less dependent on surface properties. Although the low bulk mobility limits the performance of an organic MESFET as compared to an OFET, the organic MESFETs are suitable for low-cost, low speed applications where high current density is not necessary – e.g., E-ink displays [114], and RFIDs.

To compare the performance of OMESFETs in later sections with printed OFETs, experimental results from Park et al., [81] and Knobloch et. al., [16] are frequently referred to. In the former, OFETs are made using a micro-stamping method which results a polymer thickness of 250 nm to 500 nm [81]. Knobloch has used a doctor blade to deposit the polymer with a thickness of a few hundred nanometers to fabricate OFETs [16]. In both experiments rr-P3HT is applied as the semiconductor and the transistors are tested over a voltage range of 40 V. Since, Park's transistor shows better performance (mobility of 0.02 $cm^2/V{\cdot}s$ and a current ratio of 1000), these experimental results are directly compared with the results from the experimental OMESFET in section 5.6.3.

5.3 Organic Metal-Semiconductor Field Effect Transistors (OMESFETs)

One way to make a low voltage OFET is to increase C_i, which it can be obtained by a reduction in the thickness of the insulator. In the limiting case that the insulator thickness is zero the lowest subthreshold swing is achieved. Obviously, when the insulator is removed from the OFET, the transistor can not operate in the accumulation mode. Also, the direct contact of the gate to the semiconductor affects the current in the semiconductor, unless a potential barrier between the gate and the semiconductor controls the gate current. Such a barrier can be formed by a Schottky contact between the gate metal and the semiconductor. The Schottky junction between a low work function metal and a p-type organic semiconductor is a well known phenomenon which has been used to make OLEDs and organic solar cells [44]. In semiconductor devices, a FET transistor whose gate is making a Schottky junction with the

semiconductor is known as MESFET. A key objective at the outset of this thesis was to create an organic MESFET, thereby demonstating low voltage operation and its overall characteristics.

Organic MESFETs have been reported previously in two papers. However very little information was provided in these two reports [19, 20]. In one case a MESFET structure is applied as a phototransistor in which the transistor itself is not characterized. The experiments show low voltage operation of the device [20]. In the other case, reported in 1991, the transistor is fabricated from a free standing poly(3-alkylthiophene) [19]. Although, the device has a poor current ratio (<5), again low voltage operation of the device is demonstrated. Organic MESFETs can operate at low voltage, but otherwise the possibilities arising from an organic MESFET structure are virtually unexplored. It is this exploration which is the focus of this chapter and one of the key objectives of this thesis.

5.3.1 **Structure and operation**

The structure of an OMESFET is shown in figure 5.3. The drain and the source make ohmic contacts with the semiconductor, while the junction of the gate is a Schottky junction. MESFETs work only in the depletion mode. The non-depleted region in the semiconductor provides a resistive path (channel) between the drain and the source. Since a change in the gate voltage changes the depletion width, the effective cross section of the path changes with the gate voltage. Consequently, the drain current is controlled with V_{GS}. Application of a high enough voltage in the reverse bias across the gate Schottky contact extends the depletion region to the entire thickness of the semiconductor and pinches off the channel. Forward biasing the Schottky contact broadens the channel. It is possible to design a MESFET such that at zero gate-source voltage the depletion width covers the entire thickness of the semiconductor. In this case the transistor is normally off and is called an enhancement MESFET, while when at zero gate-source voltage the transistor is on it is called a depletion MESFET. Similar to that when the Schottky contact in a MESFET is in the forward bias, it is called enhancement mode, and in the reverse bias it is in the depletion mode[2].

In order to implement the OMESFET, rr-P3HT is chosen as the semiconductor because it has the highest molecular order among soluble organics in a solid form [31] and can be easily deposited by the printing methods [81]. Also as demonstrated in the last chapter, gold and

[2] Bias mode is different from the operation mode. MESFETs operate only in the depletion mode and no inversion or accumulation occurs.

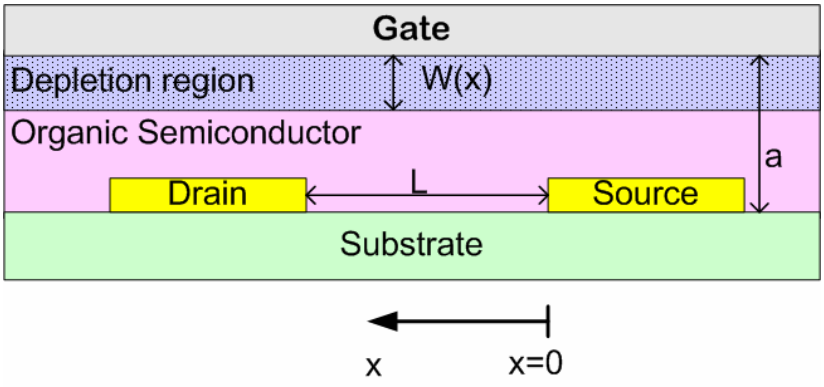


Figure 5.3. The structure of an organic MESFET at equilibrium.

aluminium can be used to make ohmic and Schottky-like contacts with rr-P3HT, respectively. Therefore, the drain and the source electrodes are made of gold, and aluminium is used as the gate metal.

In order to derive an analytical expression for the current in a MESFET one usually [55] starts with the current in an element of resistance, *dR*, at distance *x* from the edge of the source contact. Assuming that the channel has not pinched off and using the gradual channel approximation, the drain current I_D is expressed versus the voltage, *dV*, across *dR*, by:

$$I_D = \frac{dV(x)}{dR(x)} = \sigma[a - W(x)]Z\frac{dV(x)}{dx} \tag{5.7}$$

where σ is the bulk conductivity of the semiconductor, *a* is the semiconductor thickness, Z is the channel width, and *W(x)* is the width of the depletion region at position *x*. For a p-type semiconductor with a density of holes, *p*, the conductivity is equal to $q\mu p$, where μ is the bulk mobility. In a uniformly doped crystalline semiconductor *p* is usually the same as the acceptor density, N_A, and the depletion width, *W(x)*, is obtained from equation 4.3. Inserting these relationships into equation 5.7 and integrating over *x* and *V* after a variable separation results in an equation for the current at the drain terminal. Simplifying the equation gives:

$$I_D = G_o\left(1 - \sqrt{\frac{V_{bi} + V_{GS}}{V_P}}\right)V_{DS} \tag{5.8}$$

where

$$G_o = q\frac{Z}{L}aN_A\mu \tag{5.9}$$

and

$$V_P = \frac{a^2 qN_A}{2\varepsilon_S} \tag{5.10}$$

G_0 is the maximum channel conductance (when there is no depletion region), V_P is the pinch-off voltage, V_{bi} is the built-in voltage at the Schottky contact, and ε_S is the permittivity of the semiconductor.

Equation 5.8 indicates a linear relationship between the drain current and V_{DS} before the pinch-off. Beyond pinch-off the drain current saturates. Therefore, a resistive and a saturation region are expected in the output characteristic of a MESFET. The saturation current at pinch-off is usually obtained from the non-simplified current equation in the resistive regime (not shown in this document) by setting $V_{DS}=V_{GS}+V_P$ [104]. The simplified version of the saturation current is expressed by [104]:

$$I_{D,sat} = (\frac{G_o}{4V_P})[(V_{GS} - V_T)^2] \tag{5.11}$$

where V_T is the threshold voltage equal to the V_{bi}-V_P.

As in the OFETs, the transconductance and the output conductance in a MESFET are obtained from the derivatives of the drain current versus the gate voltage and the drain voltage, respectively.

5.3.2 **OMESFETs versus OFETs**

The application of OMESFETs has some advantages and disadvantages over OFETs. First, the voltage range in OMESFETs is expected to be much lower than that in OFETs because OMESFETs work only in the depletion mode. In fact, equation 5.10 shows that the voltage range is determined by the semiconductor thickness and the doping density. Second, the channel

is a part of the bulk semiconductor, whereas the channel in an OFET is a thin layer at the surface of the organic material. This property makes the OMESFET characteristics less sensitive to the roughness of the substrate, and thus suitable to apply to various substrates including fabrics. Third, there are fewer fabrication steps in OMESFETs than in OFETs because there is no insulator in OMESFETs. Fourth, the OFET performance drops rapidly with increasing semiconductor thickness due to increasing parasitic source-drain resistance [115]. This thickness dependence limits the fabrication methods to those that can deposit the organic with thicknesses of less than 50 nm. In OMESFETs the semiconductor thickness appears as a gain factor (equation 5.9). Therefore a thicker layer easily produced by printing methods is preferred in OMESFETs. The upper limit on the thickness will likely be determined by the desired operational voltage range since the thicker the layer the more voltage is needed to deplete it.

Despite the advantages of the OMESFET design, the performance in OMESFETs is limited by the low bulk mobility in the organic semiconductors. Equation 5.6 and 5.9 indicate that the speed and the drain current in a MESFET transistor are linearly dependent on the mobility in the channel (equation 5.6 is valid for the both transistors). However, G_0 can be boosted up by increasing the doping level in the semiconductor. Indeed, the bulk mobility in conducting polymers can, also, be increased by three orders of magnitude (from 10^{-6} to 10^{-3} $cm^2/V{\cdot}s$) [44] by doping the semiconductor. Nevertheless, such mobilities are still about 100 times lower than the field effect mobility. As a further challenge in OMESFETs the gate current has to be substantially lower than the channel current to apply them in a circuit. The gate current in OFETs is not a critical issue as it is low because of the insulating layer between the gate and the semiconductor.

In the crystalline semiconductors the depletion width is simply related to the voltage across the Schottky junction by equation 4.3, whereas because of the localized states in organics there is no analytical equation for the depletion width. Therefore, equations 5.8 and 5.11 which are obtained with the assumption of uniform doping in a crystalline semiconductor are not applicable for OMESFETs. However, the above discussions about the effect of the mobility, the semiconductor thickness, and the doping density on the OMESFET performance are qualitatively true as all are deduced from equation 5.7 which is valid for the OMESFET as well as crystalline MESFET. Given the distributed density of states in the semiconductor, numerical methods are preferred to obtain the OMESFET characteristics. Therefore, a simulated OMESFET is studied in the next section to predict the transistor characteristics and motivate the

experiments. Before that an OFET is simulated to compare the performance of both types of transistor. Both in the simulation and in the experiments a relatively thick layer of the semiconductor (200 nm to 400 nm) is applied for the devices to mimic the printing method of deposition [81].

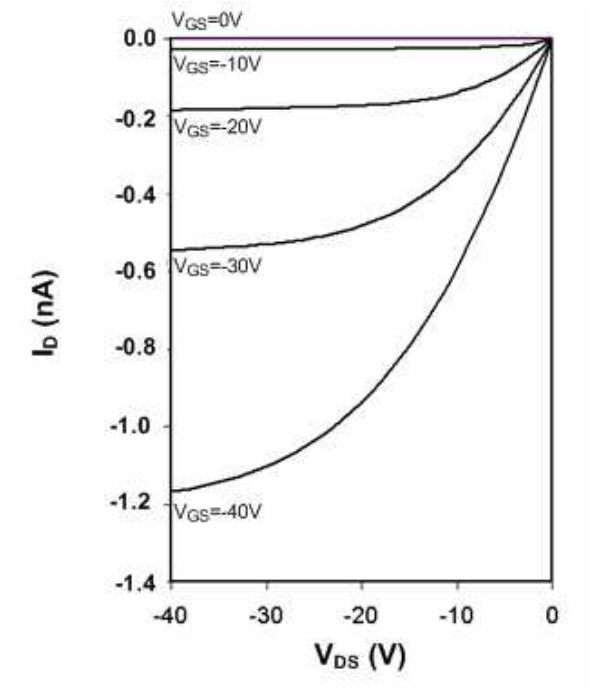
5.4 Simulation

Medici 4.0 is the CAD tool used to simulate an OFET and an OMESFET. The input codes are presented in appendix B and the parameters for the organic semiconductor are set as explained in chapter 3. Although there is no energy band in rr-P3HT, the charge transport is modeled assuming the Multiple Trapping and Release (MTR) mechanism described in chapter 2 [50] and the drift-diffusion equations can be applied to obtain the current in the devices.

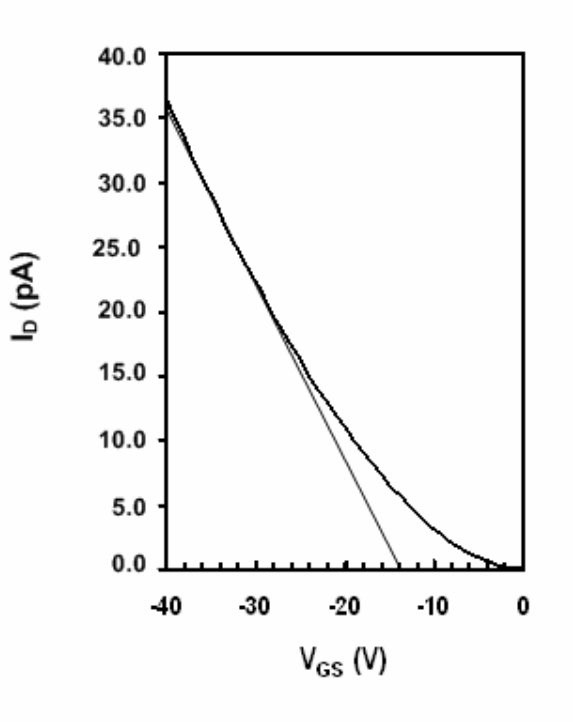
5.4.1 OFET simulation

The structure shown in figure 5.1 is used in the simulated OFET. A 400 nm thick layer of the organic polymer (rr-P3HT) is applied as the semiconductor, which is a typical thickness obtained using current printing technology [81]. The gate electrode, located at the bottom, is assumed to be made of aluminium, and the insulating layer is SiO_2 with a thickness of 100 nm. The drain and source electrodes are gold and are 4 µm wide and 20 nm thick. The gap between the drain and the source is assumed to be 4 µm which is actually the channel length of the transistor. In order to compare the simulation results with the experimental results in section 5.6 the parameters dependent on the width and the length, including conductance, transconductance and on current are normalized to Z/L =1.

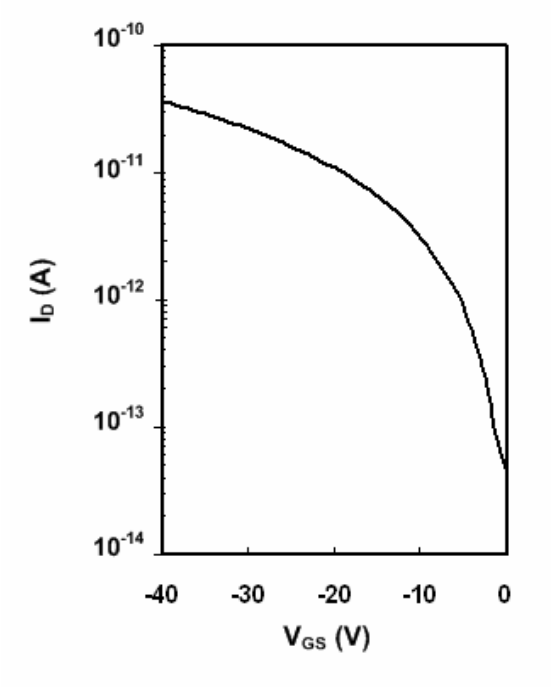
The output characteristic of the OFET is shown in figure 5.4.a for five different values of the gate voltage between 0 and -40 V. V_{DS} is, also, scanned from 0 to -40 V in steps of -1 V. The output conductance, g_o, of the OFET in the linear regime is found to be 2×10^{-10} S, from the slope of the plot when V_{GS}=-40 V at V_{DS}=0 V.



(a)



(b)



(c)

Figure 5.4. (a) The output and (b,c) transfer characteristics (V_{DS}=-0.5 V) of the simulated OFET with a channel width of 1 µm and a length of 4 µm. (b) is in a linear scale and (c) is in a semi-log scale.

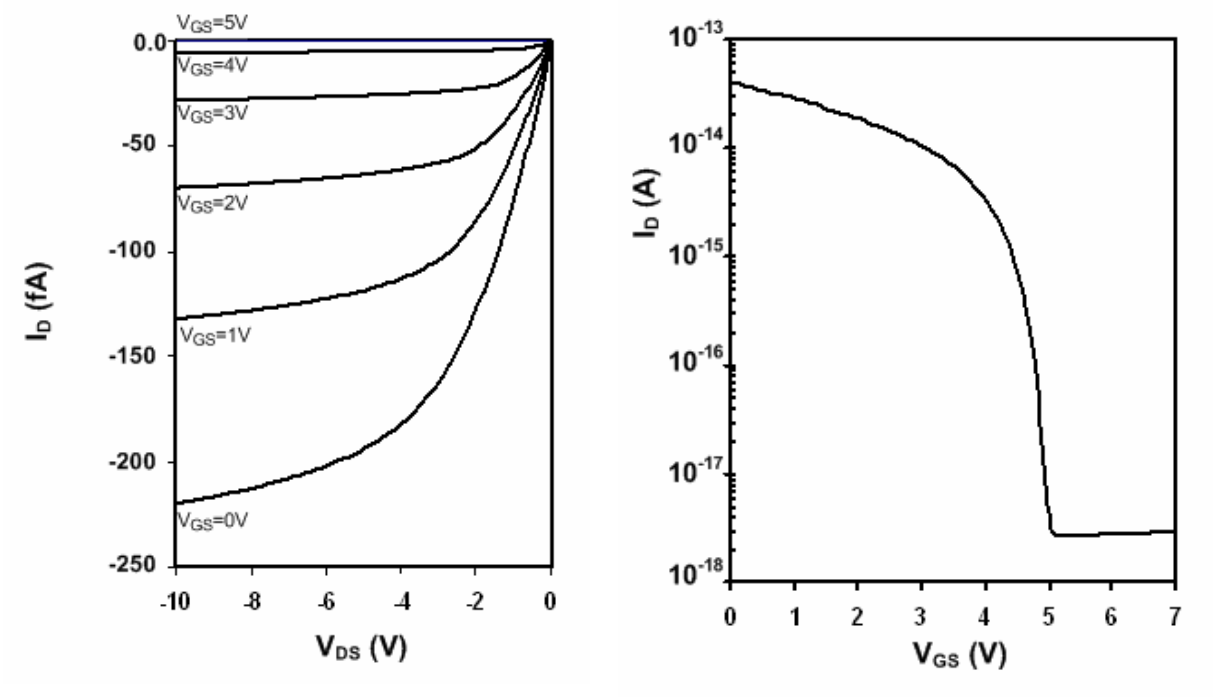
To study the transfer characteristics of the transistor the drain current is plotted versus the gate voltage in the linear regime (V_{DS}=-0.5 V), as shown in figure 5.4.b. A threshold voltage of -14 V is found for the transistor from the intercept of the asymptote to the voltage axis. Also, from the slope a mobility of 3.1×10^{-4} $cm^2/V\cdot s$ is obtained. Redrawing the curve in a semi-log scale (figure 5.4.c) shows a poor current on/off ratio (I_{on}/I_{off}) of 700, which is due to the thickness of the semiconductor. To be more like a switch, a transistor is required to have a high current ratio ($>10^4$), which also reduces the static power dissipation in a logic circuit. The inverse slope of the plot at V_{GS}=0 V, known as the subthreshold swing, is 4 V/decade, which is relatively large for a FET transistor [104]. The transconductance (g_m) in the linear regime is found from the slope of the plot at V_{GS}=-40 V to be $g_m = 6\times10^{-12}$ S.

The simulated transistor characteristics are reasonably close to those measured in printed OFETs by Knobloch et al., in Ref. [16]. A mobility in the range of 10^{-3}-10^{-4} $cm^2/V\cdot s$ and a current ratio between 10 to 140 are obtained in the experiments in printed rr-P3HT OFETs [16, 81]. The similarity between the characteristics of the simulated OFET and the actual OFETs indicate the reasonability of simulation results for studying organic transistors.

5.4.2 **OMESFET simulation**

The cross section of the device is shown in figure 5.3. Gold is chosen for drain and source electrodes and aluminium is used for the gate electrode. The same dimensions and materials that are applied in the OFET are used for the OMESFET in order to compare the performance of the two transistors. The thickness of each electrode is 20 nm and the channel length is 4 µm. The gate electrode is assumed to be long enough not only to cover the channel area but also to extend over the drain and source electrodes.

The output and transfer characteristics of the OMESFET are plotted in figure 5.5. The curves in figure 5.5.a show both the resistive and saturation regimes, which indicate the occurrence of the pinch off in the transistor. The output conductance, g_o, of 4×10^{-13} S (normalized to Z/L=1) is found from the plot at V_{GS}=0. Since the transistor works in the depletion mode, it is on at V_{GS}=0 and application of a positive voltage to the gate switches the transistor to the off mode. In figure 5.5.b the variation of the drain current versus the gate voltage at V_{DS}=-0.5 V is shown. The plot shows a subthreshold swing of 0.18 V/decade, and a threshold voltage of 5 V. Also, the normalized transconductance is $g_m=8\times10^{-14}$ S from the slope of the plot at V_{GS}=0. The on/off



(a) (b)

Figure 5.5. (a) The output and (b) transfer characteristics (V_{DS}=-0.5V) of the simulated OMESFET with a channel width of 1µm and a length of 4µm.

current ratio of the order of 10^4 is achieved using a gate voltage range of only 5V.

In order to obtain the bulk mobility in the OMESFET the device is simulated in the absence of the aluminum layer. Then, the I-V curve at the drain terminal is plotted (figure 5.6). The slope of the curve indicates that G_0=1.24×10^{-13} S. Knowing the doping density (N=1×10^{16}cm^{-3}) the bulk mobility is found to be 8×10^{-6} cm^2/V·s which is in good agreement with experimental results [116]. The bulk mobility is about 40 times lower than the field effect mobility.

In OFETs the gate current is not a crucial parameter in DC characteristics. The gate current in OMESFETs limits the performance of the devices. In figure 5.7, the gate current is plotted versus the gate voltage at V_{DS}=-10 V. The leakage current of the reverse biased Schottky junction between the gate and the semiconductor shows a current value in the order of 10^{-18} A. This current is small enough compared to the drain current to be ignored when the transistor is on. However, the off current for the transistor is in the range of the gate current which likely indicates that the off current is limited by the gate current. Therefore, the off current is expected to be reduced if the gate current is reduced.

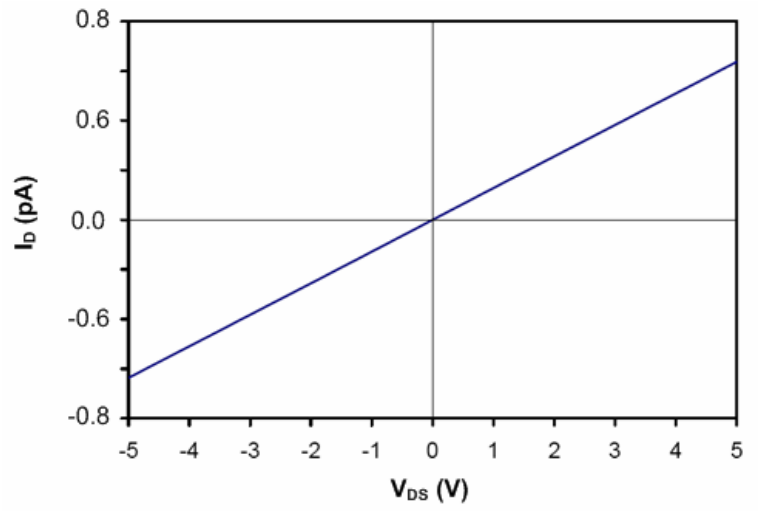


Figure 5.6. The simulated I-V curve between the drain and source terminals of the OMESFET in the absence of the gate contact. The slope indicates G_0 in the OMESFET.

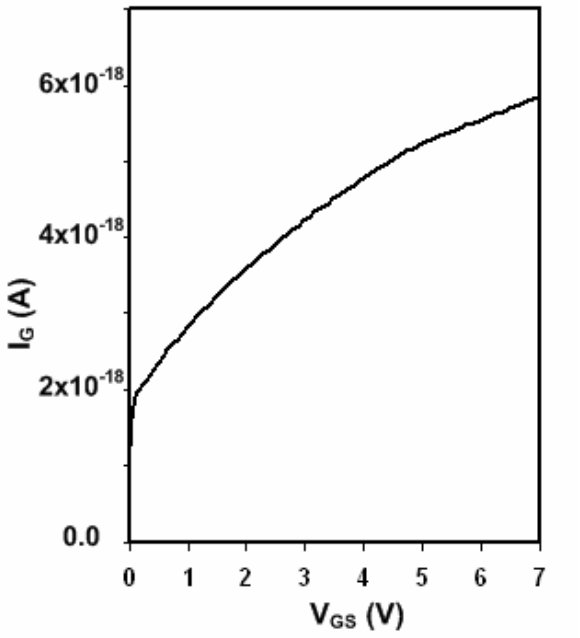


Figure 5.7. The input characteristic of the simulated OMESFET.

The different parameters obtained from the simulation of the OFET and the OMESFET are listed in table 5-1. As the main advantage the voltage range is significantly lower in the OMESFET (5 V) than that in the OFET. In addition, the OMESFET has a very small subthreshold swing, making it well-suited to logic circuits. g_0, g_m, and I_{on} in the OMESFET are much smaller than in the OFET mainly due to the lower mobility in the OMESFET.

Table 5.1. Electrical characteristics of the simulated OFET and OMESFET.

Parameter	OFET	OMESFET
I_{on}/I_{off}	700	10^4
Gate Voltage Range (V)	40	5
Threshold Voltage (V)	-14	5
Subthreshold Swing (V/decade)	4	0.18
Mobility ($cm^2/V{\cdot}s$)	$3.1x10^{-4}$	$8x10^{-6}$
g_o (S)†	$2x10^{-10}$	$4x10^{-13}$
g_m (S)†	$6x10^{-12}$	$8x10^{-14}$
I_{on} (A) @ V_{DS}=- 0.5 V†	$1.4x10^{-10}$	$1.6x10^{-13}$

†: normalized to Z/L=1.

The low conductance, transconductance and on current in the OMESFET does make it less desirable than the printable OFET in applications where voltage and on/off ratio are not critical, but obtaining high current is (e.g. organic LEDs). g_0, g_m, and I_{on} are however adjustable by increasing the doping density in the semiconductor (the doping density is assumed to be 10^{16} cm^{-3} in the simulation). An increase in the channel width to length ratio (Z/L) also improves these parameters [104], in which case the desired values of g_0, g_m, and I_{on} are achievable for the OMESFET at the expense of size.

The simulations thus suggest that OMESFETs will enable the voltage problem to be overcome, but this is achieved at a performance cost. It is now demonstrated experimentally that the use of relatively highly doped semiconductor can enhance the OMESFET performance.

5.5 Fabrication of Organic Transistors

The fabrication process of the organic transistors is very similar to that in the organic Schottky diode explained in chapter 4. As before, device dimensions and thicknesses are chosen to simulate what is possible in printing processes (e.g. thick layers and poor lateral resolution).

To build an OFET a layer of rr-P3HT is deposited on a micro-electrode (figure 3.1). Highly doped silicon with a 350 nm thick silicon dioxide layer are used as the gate and the insulator in the OFET and the gold electrodes are used as the drain and source contacts. The micro-electrode is cleaned with piranha solution and dried with nitrogen before polymer deposition. The

polymer solution is prepared by dissolving 16 mg of rr-P3HT (purchased from ADS [117]) in 2 ml of chloroform (0.54% in weight) and sonicating the solution for 30 minutes. Dip casting is used to deposit the polymer on the micro-electrode. In this method the sample is dipped in the polymer solution and pulled out slowly. The fast evaporation of the chloroform leads to the formation of a film of the polymer on the micro-electrode when it is pulling out. Although manually dip casting the polymer does not give a reproducible thickness, it is quite uniform over the electrode area. Using casting methods films with thicknesses of 200 nm to 400 nm were produced, as measured with an atomic force microscope. After deposition of the organic the sample is heated for 20 to 30 minutes at 100 °C to evaporate the residual chloroform and anneal the film [82].

After measuring the OFETs characteristics, the samples are used to build Schottky diodes and OMESFETs by deposition of an aluminium layer over the electrode areas (figure 4.4). The details of the aluminium deposition and its patterning are explained in section 4.5.

Since there are four electrodes in each micro-electrode, three transistors are made in each fabrication batch, which can then be individually tested. The length of electrodes (500 μm) is the channel width, *Z*, and the spacing between them (4 μm) is the channel length, *L*, in the transistor. Regarding the thickness of the silicon dioxide layer (350 nm) the gate capacitance in the OFETs is 9.8 nF/cm^2.

5.6 Electrical characteristics

The characteristics of a thick film OFET are presented which indicate a poor performance. Then the experimental results from an OMESFET with the same thickness as the OFET are presented. The DC parameters of the OMESFET are then compared with those from a relatively high-performance printed OFET reported by Park et al., [81]. Since the transistor's dimensions are different from those in the simulated transistors in section 5.4, the parameters which are dependent on the dimensions are normalized to $Z/L = 1$ – e.g. conductance, transconductance, and on current to aid comparison.

5.6.1 **OFET**

The attempt to build an OFET in air was unsuccessful because of the rapid air-induced change in the rr-P3HT conductivity. The bulk conductivity becomes so high that the drain current

achieved in accumulation mode shows a trivial increase relative to the off current. The long vacuum dedoping process applied for organic Schottky diodes (section 4.6.1) is, also, not working in the OFET, because the organic layer is exposed to air during the test and the oxygen redopes the polymer quickly. Therefore, the OFETs are fabricated and tested in a glove box filled with dry nitrogen.

The drain current is measured with a Keithley 2400, which is a Source-Measure Unit (SMU), when the drain voltage is scanned from 0 to -20 V with steps of -1 V. The current is measured in 10 samples at each step and the average of samples is recorded. In every scan the gate voltage is held constant by a Keithley 6430 unit while the gate current is recorded. The gate voltage is changed after each scan with a step of 5 V. A 10 sec delay is applied at the beginning of each scan to guarantee that the charge is settled after the gate voltage change. The measurement and data recording is managed by LabTracer 2.0 which controls the Keithley instruments through GPIB ports.

Using dip casting method a layer of rr-P3HT with a thickness of 200 nm is deposited on a micro-electrode to make an OFET. As it is shown in figure 5.8 (output characteristic) the performance of the OFET is very poor. Although, the current is modulated by the gate, the current ratio of only 2.4 is achieved in a 20 V change of the gate voltage. Also, no saturation occurs in the drain current. In such a case the device is more like a controllable resistor than a transistor. Using the transverse characteristics of the transistor (not shown) the field-effect mobility and threshold voltage are measured to be 4.9×10^{-4} $cm^2/V \cdot s$ and +21 V, respectively.

The OFET presented here has shown poor performance, mainly due to the trivial difference between the bulk mobility (1.6×10^{-4} $cm^2/V \cdot s$) and the field-effect mobility and a high positive threshold voltage. A similar performance (low current ratio, low mobility, and a high threshold voltage) has already been reported for a printed OFET [81]. High doping density, poor molecular order at the surface of the insulator, and a relatively thick film of semiconductor and insulator are the main reasons for such poor performance.

Park et al. have shown that the performance of a printed OFET is enhanced by dedoping the semiconductor with vacuum and O_2 plasma treatment of the insulator surface, which assists the formation of an ordered layer of semiconductor on the insulator. The former treatment reduces the bulk conductivity and the bulk mobility in the polymer and plasma treatment enhances the

field-effect mobility. As explained in the next chapter, reducing the bulk conductivity and the semiconductor thickness increase the current ratio and adjust the threshold voltage. However, the performance is still likely reduced due to the thick semiconductor layer printed by micro-stamping method (250 nm to 500 nm). A current ratio of 1000 with a mobility of 0.02 $cm^2/V{\cdot}s$ are reported for this printed OFET [81]. However, the voltage range (40 V) and the subthreshold swing (6.5 V/decade) are still high in the device. The extra treatments applied to enhance the OFET performance add to the capital cost of production. If a vacuum process is used, why not also vapour deposit the semiconductor to get a thin and ordered layer?

In the next section the OMESFET is demonstrated as a low voltage transistor fabricated in a few steps. The enhanced characteristics of the printed OFET from Ref. [81] are listed in table 5-2 to compare them with the fabricated OMESFET.

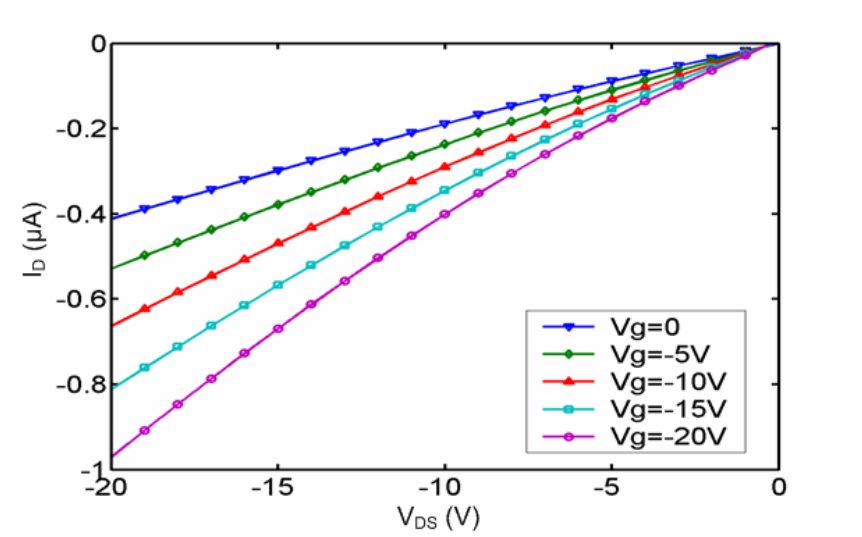


Figure 5.8. The output characteristic of the OFET with the polymer thickness of 200 nm.

5.6.2 **OMESFET**

Since a large gate current in a MESFET ruins the operation of the transistor, a low reverse bias current is essential in both the gate-source and the gate-drain Schottky diodes. As is explained in the last chapter, application of a thick layer of polymer and a low-rate deposition of aluminium result in low reverse bias Schottky diodes, providing that the polymer is isolated from oxygen and moisture. A dip casting method is applied for deposition of a thick layer of rr-P3HT on the micro-electrode array and the aluminium deposition rate is controlled at 0.5 Å/s. To avoid any contamination the organic deposition is done in the glove box and the evaporator embedded in

the glove box is utilized for the aluminium deposition. Indeed, the same sample which provided the OFET results in figure 5.8 is converted to an OMESFET by depositing of an aluminium layer on top of the 200 nm thick semiconductor (a = 200 nm). Since in the OMESFET approach doped semiconductors are preferred, no attempt is done to dedope the polymer before the aluminium deposition.

Figure 5.9 shows the output characteristics of the OMESFET. The transistor shows a low conductance when the gate voltage is less than 3V, which is interpreted as the threshold voltage. The conductance increases with a drop in the gate voltage. The plot indicates a current ratio of 24.6 at V_{DS}=-3.5 V when the gate voltage is changed from -1 V to +3.5 V. The transistor is operating in the enhancement mode when the gate voltage is negative, while it is driven into the depletion mode when V_{GS}>0.

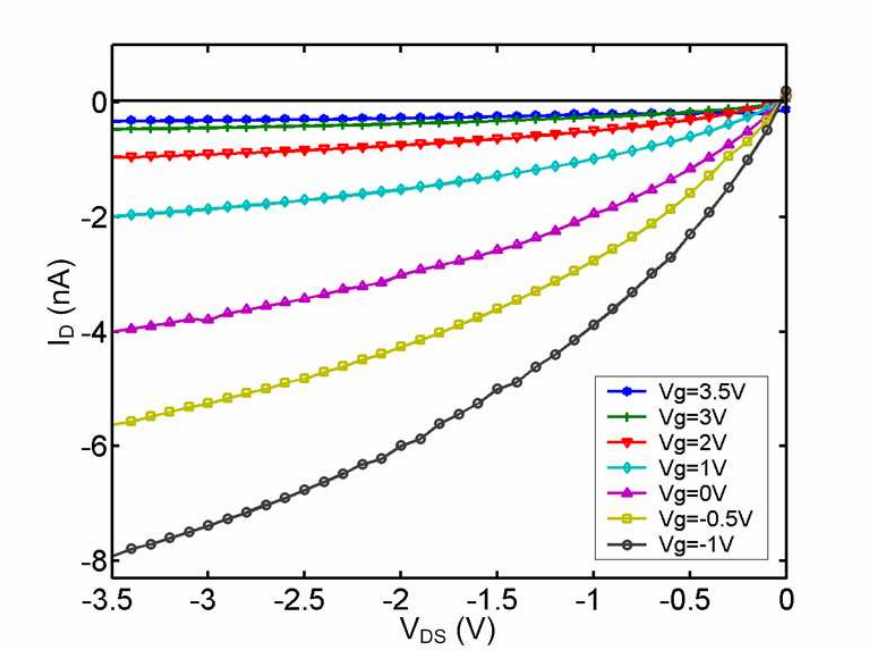


Figure 5.9. The measured output characteristic of the OMESFET.

The mobility in the OMESFET is expected to be the same as the bulk mobility (μ= 1.6×10^{-4} $cm^2/V\cdot s$) measured by the space-charge limited current (SCLC) in the Schottky diode. The conductivity of the polymer is determined from the source-drain resistance measurement to be σ = 7.2×10^{-6} S/cm (figure 4.5). From these measurements the carrier concentration of p=2.81×10^{17} cm^{-3} in the semiconductor is estimated from:

$$\sigma = q \cdot \mu \cdot p \tag{5.12}$$

In OFETs, the transverse characteristic is used for measuring the field effect mobility and the threshold voltage, but this is not applicable for OMESFETs because of the nonlinear dependence between I_D and V_{GS} (equation 5.8). However, the I_D-V_{GS} plot in the OMESFET leads to the determination of the dependence of the depletion width in the Schottky junction on the voltage across the junction. One can assume that the variation of the depletion width (W) along the channel is negligible at low V_{DS}. Under such a condition, the drain current (I_D) is expressed by:

$$I_D = \sigma \frac{Z(a-W)}{L} V_{DS} \tag{5.13}$$

Therefore the depletion width is:

$$W = -\frac{L}{\sigma \cdot Z \cdot V_{DS}} I_D + a \tag{5.14}$$

Figure 5.10 shows the I_D-V_{GS} at V_{DS} = -0.3 V. The magnitude of the current is decreasing when the voltage is changing from -1 V to 3 V. The slight increase in the magnitude of the current when V_{GS}>3 V is likely due to the effect of the gate current (I_G) which it is larger than the channel current at low V_{DS}. Equation 5.14 is applied to obtain W from I_D and W-V_{GS} is, then, plotted in figure 5.11 for -1 V <V_{GS}< 3 V. As the plot indicates the depletion width is very close to 200 nm (the polymer thickness) when V_{GS}=3 V, which confirms the pinch-off around this voltage. A depletion width of about 172 nm is estimated at the zero bias. Choosing to fabricate a transistor with a semiconductor thickness of less than 172 nm would give an enhancement OMESFET. The difference between slopes above and below V_{GS}=0 V indicates that the variation of the depletion width in enhancement mode is more than that in the depletion mode for the same voltage span.

To check whether the depletion width is proportional to the square root of the voltage, W^2 is plotted in the same chart (figure 5.11). The nonlinearity between the voltage and W^2 indicates that equation 4.3 is not applicable in organic Schottky contacts. Using the least square error a fit curve is obtained for W with less than 0.2% error at every measured point. The equation which describes the fit curve is found to be:

$$W = 200 \times \left(1 - 0.1363 \times \exp\left(-0.6471 \cdot V_{GS}\right)\right) \tag{5.15}$$

where W has a unit of nm. Therefore, the relationship between the depletion width and the voltage in the organics is more exponential than quadratic, as has been found by others [69].

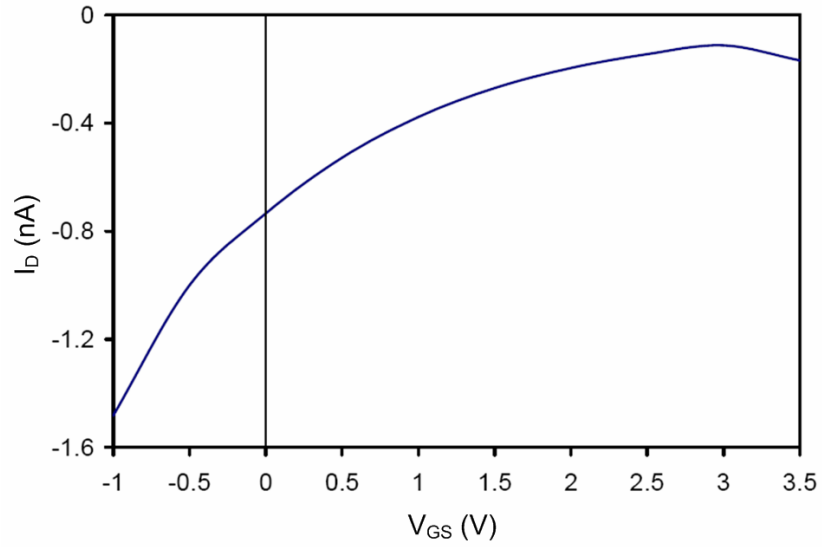


Figure 5.10. The measured I_D-V_{GS} characteristics of the OMESFET at V_{DS}=-0.3V.

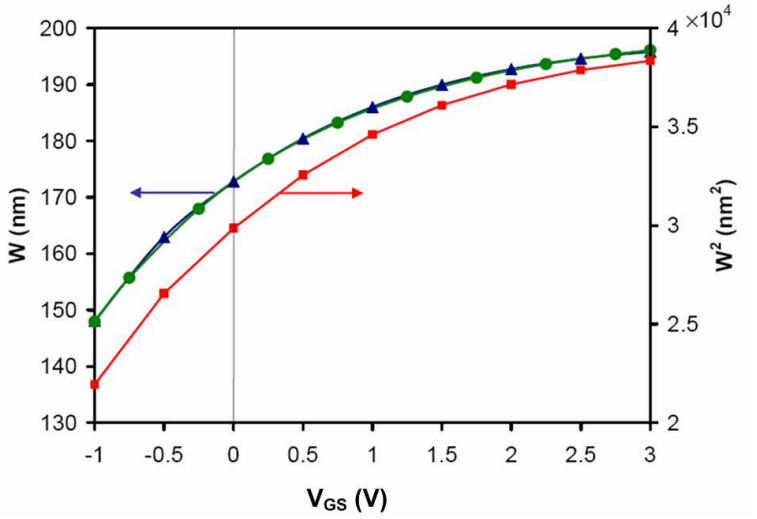


Figure 5.11. The depletion width versus the voltage. (▲) calculated W from the measured drain current (●) fit curve calculated from equation 5.15, (■) W^2 versus the voltage.

The magnitude of the gate current in a field effect transistor limits the number of transistors that a single transistor can drive. This is referred to as the fan-out of a logic gate made of these transistors. The highest gate current happens when the transistor is in the enhancement regime. Therefore the gate current is studied by plotting I_G-V_{DS} in figure 5.12 when V_{GS} = -1 V. The average gate current is about -0.48 nA which is about 16 times lower than the on current at V_{DS} = -3.5 V in figure 5.9.

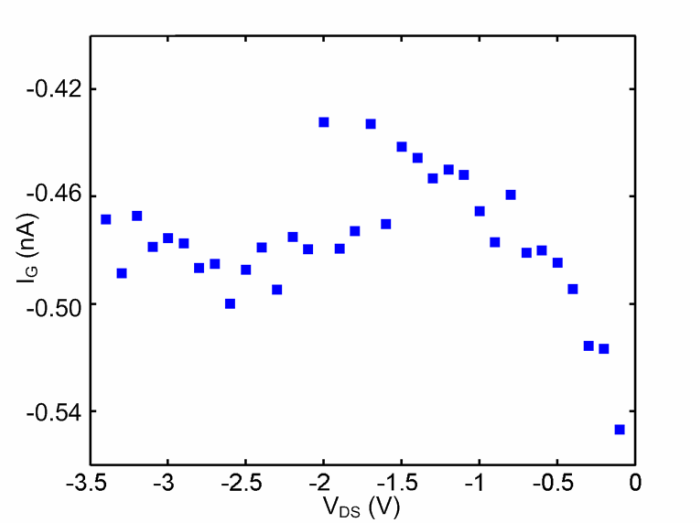


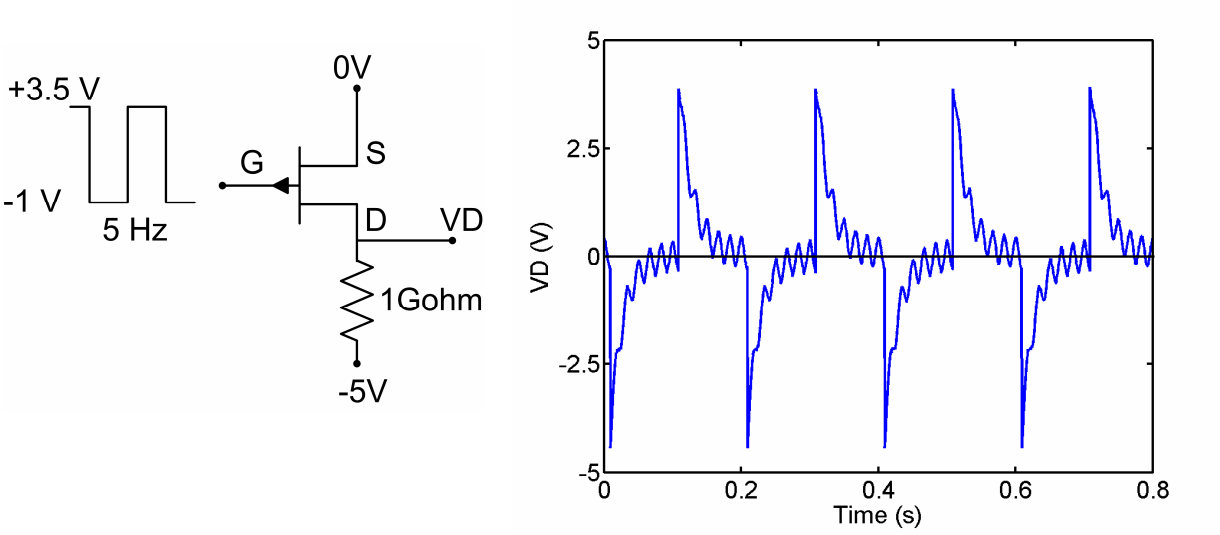
Figure 5.12. The gate current versus the drain source voltage in the OMESFET (V_{GS}=-1V).

The normalized (Z/L=1) output conductance and the transconductance are found to be 4×10^{-11} S and 3.7×10^{-11} S, respectively. The subthreshold swing of the device is measured to be 2.5 V/decade.

The switching speed of the transistor is studied with an application of a 5 Hz square wave to the gate which switches between -1 V and + 3.5 V. The drain voltage is, then, monitored by an oscilloscope in the AC mode while the drain was pulled down with a 1 GΩ resistor to -5 V. The result (figure 5.13) shows the operation of the device at 5 Hz. The peaks are almost lost when the input frequency is raised to 20 Hz. Such a limited range of frequency is expected because of the large parasitic capacitance between the gate and the source/drain. Indeed, 20 Hz is the cut-off frequency that has already been measured for the organic Schottky diode in the reverse bias (figure 4.17). To improve the switching speed the application of an insulating substrate instead of the conducting silicon is suggested to reduce the parasitic capacitances between the gate and

the drain/source electrodes. Here silicon is chosen intentionally to be able to test both the OFET and the OMESFET consistently for every sample.

In the absence of the parasitic capacitor, a switching speed of 3.1 kHz is expected for the OMESFET with a channel length of 4 μm, mobility of 10^{-4} $cm^2/V{\cdot}s$, and V_{DS}=5 V (see equation 5.6) Such a frequency is adequate for many low frequency applications, including small displays and even organic RFID tags. Although the carrier signal in RFID tags is either at 125 kHz or 13.56 MHz, in passive tags the logic circuit does not necessarily operate at high frequencies (usually only a few kHz).



(a) (b)

Figure 5.13. (a) The circuit diagram applied to monitor the switching properties of the OMESFETand (b) the AC pulse response of the OMESFET.

5.6.3 **OMESFETs versus OFETs**

The characteristics of the printed OFET reported by Park [81], and the 200 nm thick OMESFET are compared in table 5-2. The work by Park is chosen because it represents the best performance reported to date in a thick film OFET. In some aspects such as the voltage range and subthreshold swing, the OMESFET is better, whereas the mobility dependent parameters of the OFET, including g_o, g_m , I_{on}, and I_{on}/I_{off}, are better.

The voltage range and the subthreshold swing in the OMESFET are lower than those in the OFET because of the absence of the insulating layer in the OMESFET, which provides direct control of the gate voltage over the depletion region in the semiconductor.

Table 5.2. Electrical characteristics of the printed OFET from Ref. [81] and the OMESFET.

Parameter	**OFET [81]**	**OMESFET**
I_{on}/I_{off}	1000	24.6
Gate Voltage Range (V)	40	4.5
Threshold Voltage (V)	+2.5	+3
Subthreshold swing (V/decade)	6.5	2.5
Mobility ($cm^2/V{\cdot}s$)	$2x10^{-2}$	$1.6x10^{-4}$
g_o (S)†	2×10^{-8}	4×10^{-11}
g_m (S)†	3×10^{-8}	3.7×10^{-11}
$I_{on\text{-}max}$ (A)†	$5x10^{-7}$	$6.4x10^{-10}$

†: normalized to Z/L=1.

In the OFET g_o, g_m , and I_{on} are about 3 orders of magnitude higher than those in the OMESFET. Those parameters are proportional to the product of the mobility in the device and either V_{DS} or V_{GS} (see equations 5.2, 5.3, 5.4, 5.8, and 5.9). Since the field-effect mobility in the OFET is about 100 times larger than the bulk mobility in the OMESFET and the voltage range is about 10 times larger in the OFET than that in the OMESFET, the 3 orders of magnitude difference in those parameters is expected.

The weakest parameter in the OMESFET is the low current ratio (24.6). The low current ratio results from high off current in the OMESFET (the on current is in the expected range as discussed above). In the off mode that the current in the channel is very low the drain terminal current is determined by the leakage current from the gate. The gate current in OFETs is much lower than in OMESFETs, because of the insulating layer between the gate and the channel in OFETs. The current ratio in OFETs is instead limited by the semiconductor thickness and the bulk conductivity of the semiconductor (see section 6.2). A current ratio as high as 10^6 is achievable in OFETs [21] if a very thin intrinsic semiconductor is applied. However, soluble organic semiconductors employed for printing techniques usually have some background doping due to the impurities both in the polymer and in the solvent. Also, the printing

techniques have poor control over the thickness of the deposited layer. As a result the current ratio in this and other printed OFETs are much lower than 10^6.

As mentioned, the OFET reported by Park [81] takes advantage of an O_2 plasma treatment and vacuum dedoping that is not appropriate for use with low cost printing processes and in this sense represents potential performance using printing processes. In another example of a thick film device [16], that does not use vacuum purification or surface treatment the on/off ratio is much lower (~10). However the results from Park and the simulations offer some insight into what can potentially be achieved. By comparing Park's work to the OMESFET response, and by comparing simulation results, the OMESFET offers low voltage and possibly lower sub-threshold swing, while the OFET offers higher on current and transconductance. Simulations suggest that on/off current can be better in OMESFETs, but this remains to be demonstrated experimentally.

5.7 Discussion

Although both simulation and experimental results indicate the low voltage operation of OMESFETs, the characteristics predicted by the simulation are different from what have been obtained in the practice. To explain the differences and possible reasons, voltage ranges, mobilities, threshold voltages, current ratios and subthreshold swings in tables 5-1 and 5-2 are integrated in table 5-3, and each item is discussed in following subsections. As it is explained in section 5.6.3, conductance, transconductance and the on current in transistors are dependent on the mobility and the voltage range, so they are not discussed individually.

Table 5.3. Electrical characteristics of the simulated and real transistors.

Parameter	**Simulation**		**Experiments**	
	OFET	**OMESFET**	**OFET [81]**	**OMESFET**
Gate Voltage Range (V)	40	5	40	4.5
Mobility ($cm^2/V{\cdot}s$)	$3.1x10^{-4}$	$8x10^{-6}$	$2x10^{-2}$	$1.6x10^{-4}$
Threshold Voltage (V)	-14	5	+2.5	3
I_{on}/I_{off}	700	10^4	1000	24.6
Subthreshold swing (V/decade)	4	0.18	6.5	2.5

a) Mobility

In both simulations and experiments the field-effect mobilities are two orders of magnitude larger than the bulk mobilities, but the mobilities obtained from the simulation are much lower than the realistic ones. This is partially due to the high doping level in the experiment. The measured dopant density (2.81×10^{17} cm^{-3}) for the OMESFET is at least one order of magnitude larger than what has been set in the simulation (10^{16} cm^{-3}). Since the Fermi level in the bulk semiconductor moves toward the mobility edge with an increase in the doping level, a higher bulk mobility is obtained in the real OMESFET. Also the density of states in the simulation is possibly overestimated. A sharper tail drop in density of localized states away from the mobility edge leads to higher bulk and field-effect mobilities for a given doping level. The simulation and experimental results in organic Schottky junctions, also, confirm the overestimation of the density of states in the simulation. The simulation results in figure 4.3 suggest a depletion width of < 120 nm whereas the width calculated from measured drain current (as shown in figure 5.11) is 170 nm. This indicates that in the simulation the depletion width at equilibrium is under estimated, especially given that the doping density in the simulation (10^{16} cm^{-3}) is set lower than the measured value (2.81×10^{17} cm^{-3}). Therefore, the density of states chosen for rr-P3HT in the simulation is not accurate.

Although the experimental result from Tanase et al., [58] is applied to define the density of states in the simulation, in practice the density of states depends on many factors including deposition method, boiling point of the solvent, substrate material and surface treatment prior to the polymer deposition. Therefore it is very likely that the density of states of the rr-P3HT used in the experiments presented here is different from the values used in the simulation.

In fact, the simulation results mimic a very amorphous semiconductor with low doping density, whereas in practice the organic has higher molecular order and higher background doping.

b) Threshold voltage

The measured threshold voltage in the OMESFET is 3 V whereas the voltage predicted from the simulation is 5 V. Their difference is likely due to the difference between the thicknesses of the simulated OMESFET (400 nm) and the real OMESFET (200 nm). Although the high doping level in the real OMESFET can potentially increase the threshold voltage, the more compact density of states has probably compensated for this effect.

The difference between the threshold voltages of the simulated and real OFETs is significant. Such a large discrepancy is due to the doping level in the real OFET. In the next chapter the effect of the conductivity and the thickness of the semiconductor film on the threshold voltage of an OFET is explained (equation 6.11). Since the thickness of the simulated OFET (400 nm) is in the same range as that in the real OFET (250 to 500 nm) the difference is mainly due to the difference in bulk conductivity between the semiconductors in the experiments and in the simulation. Indeed, Park has shown that dedoping the polymer by vacuum treatment can shift the threshold voltage from +20 V to +2.5 V [81]. Such a large drift in the threshold voltage indicates the high sensitivity of the threshold voltage in OFETs to the doping level in the semiconductor, whereas in OMESFETs the variation of threshold voltage with the doping level is more controlled. Since the doping level in the organics increases with any contamination in the materials or the process, reproducing and maintaining a specific threshold voltage in mass production of OFETs may require extra steps and/or more complicated processes to purify the materials and provide a clean environment for the fabrication. The OMESFET is less affected by contamination, a factor that could be very important in making low cost production.

c) On/off Current ratio

The predicted current ratio in the simulation for the OFET is close to what has been reported in a real device. This ratio is strongly dependent on the ratio of field effect to bulk mobility, μ_f/μ (as is suggested in equation 6.10), which both in the simulation and experiment the field-effect mobility is about two orders of magnitude larger than the bulk mobility. The weakest parameter in the real OMESFET is the low current ratio. Although simulation has predicted a current ratio of 10^4, the experimental value is much lower (24.6). This is likely due to the gate leakage current. Reduction in the gate current reduces the off current and increases the current ratio. To reduce the leakage current the reverse current of the organic Schottky diode has to be reduced. A few solutions are suggested later in this section.

d) Subthreshold swing

The predicted subthreshold swing in the simulated OFET is reasonably close to what has been measured in the experiments. A small gate capacitance (~10 nF/cm^2) and a thick semiconductor film are main reasons for the large subthreshold swing in the OFETs. In OMESFETs the measured subthreshold swing is much larger than the prediction from the simulation. The difference is likely due to the gate leakage current in the real OMESFET. When the gate current

is comparable to the channel current, the drain terminal current is more influenced by the gate current. In the subthreshold regime where the channel current is low the gate current determines the subthreshold swing, unless the gate current is much lower than the channel current as it is indicated in the simulation. It should be possible to reduce gate leakage by changing transistor geometry, as is discussed later in this section. This will then improve OMESFET on/off ratio.

The simulations used in this thesis have been useful for qualitatively predicting aspects of transistor performance. However, in order to get close matching between experiment and simulation the properties of the organic semiconductor as processed need to be known. In particular the density of states in the polymer has to be accurately determined.

Nevertheless, the simulations have helped motivate the development of the OMESFET and suggest that properties such as on/off current ratio and the subthreshold swing can be substantially improved.

The performance of OFETs improves with a reduction in the semiconductor thickness and with reduction in doping density. In OMESFETs in contrast an increase in these parameters enhances the performance {equation 5.9). The reasons for these differences are that high current ratio and high on current are achieved in OMESFETs when the semiconductor layer is highly conductive, while in OFETs a poorly conducting semiconductor is preferred (in order to have a low off current). Therefore, one can say starting from very thin low-doped organic layer the OFETs performance is better than that in OMESFETs, but an increase in the thickness or doping make their performances comparable until above a certain level OMESFETs are preferred. This preference for operation at large thicknesses is an important advantage of the OMESFET over the OFET for use with printing and dipping processes, where layers are generally thick. Also, the doping level in the semiconductor significantly affects the threshold voltage in OFETs, whereas the threshold voltage is less sensitive to the doping level in OMESFETs. The tendency of organics to be doped by any contamination in the materials or the process is a weakness for mass production of OFETs, especially when a low-cost method, like printing, is employed.

Therefore increases in the semiconductor thickness and the doping level in the OMESFET are suggested to achieve higher conductance, transconductance and on current. Increasing both the semiconductor thickness and its doping density increase the voltage range in the transistor. If it is necessary to reduce the voltage range a metal with lower work function such as magnesium (Mg) might be applied. The main challenge to enhance the OMESFET performance is the

reduction of the gate current, which leads to improved current ratio and subthreshold swing. Fabrication of Schottky diodes with low reverse currents is a solution to reduce the gate current. Application of a metal with lower work function than aluminium is again a solution as it reduces the injection of carriers from metal to the semiconductor. Also a very large portion of the gate current likely results from the overlap of the gate and the drain/source electrodes, as depicted in figure 5.14.a. Covering the top surface of the drain and source electrodes with an insulator before polymer deposition is recommended (figure 5.14.b) to reduce the leakage current. In this case the electrodes are in contact with the semiconductor from the sides and the depletion region from the gate controls the channel. The patterning of the insulator layer is not necessary as the insulator can be deposited over the metal before the lift off step. A thicker layer of metal may be necessary to ensure a low contact resistance between the drain/source electrodes and the semiconductor.

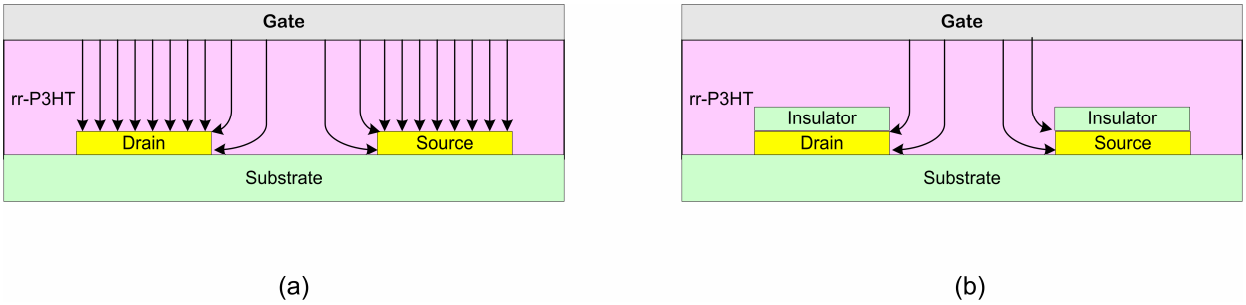


Figure 5.14. (a) The gate current paths in the experimental OMESFET (b) the solution to reduce the gate current. (V_{GS} >0 and V_{DS}=0)

In general OMESFETs are compatible with the printing methods in which a relatively thick layer of semiconductor can be deposited. The low voltage feature in OMESFETs has some benefits in battery operated applications. Also, OMESFETs are promising for driving Active Matrix Displays (AMDs). For current generation of active displays a current density of about 0.3 mA/cm^2 is adequate to turn on pixels [118]. The OMESFET presented in this work (table 5-2) is capable to provide 0.13 mA/cm^2, which should readily be increased by increasing doping level and/or thickness. However, much better current ratio has to be demonstrated in order to apply OMESFETs in AMDs. Similarly, Liquid Crystal Displays (LCDs) and “E-ink” displays, developed by Plastic Logic [114], require very small currents which make the OMESFET a

suitable choice for low-cost and flexible displays. Achieving better current ratio is, however, necessary to distinct the on and off states of each pixel in the display.

Another application for which the OMESFETs may be suitable is in cheap and low-voltage chemical and/or optical sensors. Since the conductivity of the polymer changes with exposure to some chemicals, including oxygen and moisture, the drain current can represent the chemical level. The depletion width in the OMESFET, also, changes in response to light [20]. Therefore, the drain current might be used to detect light in a certain range of wavelength.

A low voltage transistor is preferred for logic applications, especially for battery operated electronics and circuits which receive their power from electromagnetic coupling, such as RFIDs. Although the OMESFET has a bandwidth of only 20 Hz, it should be possible to extend this to a few kHz by fabricating the device on a pure insulating substrate. In that case OMESFETs might be suitable for RFID tags.

In conclusion, OMESFETs outperform OFETs by presenting low voltages and higher current ratio (figures 5.8 and 5.9) when a thick doped polymer is applied. For a printed semiconductor layer with thickness of a few hundred nanometers the voltage range is less than 5 V in the OMESFET, whereas the voltage range is typically larger than 20 V in OFETs. The current ratio is potentially higher in thick film OMESFETs than OFETs, providing that the gate leakage current is controlled. The high doping level and poor molecular order in a printed semiconductor film result a small difference between the field-effect mobility and the bulk mobility. Although the performance of the OFET can be enhanced by increasing the field-effect mobility through extra treatments on the substrate and the semiconductor, the process is expensive and increase the capital cost of the product.

Remaining challenges include devising a complete process (perhaps all polymer) suitable for constructing the OMESFETs, as well as investigating means of improving performance.

5.8 Summary

A key aim of this research is to determine the feasibility of building an OMESFET in order to offer a low voltage alternative to OFETs which is also preferably compatible with low cost fabrication methods. Low voltage operation was successfully achieved, and the transistors work well with the thick organic semiconductor layers typical of low cost processes.

The low mobility and the large voltage range in OFETs are two challenges constraining the widespread application of organic transistors. A low-doped semiconductor layer with high molecular order is required to obtain high field-effect mobility in an OFET. Also very thin insulator and semiconductor films have to be applied in an OFET to achieve low voltage operation. Application of printing methods to produce low-cost OFETs have shown poor transistor characteristics because of the high doping level, poor molecular order and thick deposited films [16, 81]. A mobility of 10^{-3} to 10^{-4} $cm^2/V{\cdot}s$ and a voltage range of 40 V and a current ratio less than 140 are typical in printed OFETs. To enhance the device performance Park et al. [81] have applied O_2 plasma and vacuum treatments to increase the mobility and the current ratio to 0.02 $cm^2/V{\cdot}s$ and 1000, respectively. These treatments, however, increase the capital cost of electronics. In addition, the voltage problem is still a challenge in OFETs.

To be compatible with the quality of a printed layer of a semiconductor OMESFET is suggested as a low voltage transistor. The effective mobility in an OMESFET is the bulk mobility in the semiconductor which can be increased to 10^{-3} $cm^2/V{\cdot}s$ by increasing the doping level [44]. Also, expensive treatments such as those used in printed OFETs are not required in the OMESFET fabrication.

The low voltage operation of OMESFETs (<5 V) are demonstrated in this thesis both in simulation and experiment. In simulation a threshold voltage of 5 V and a mobility of 8×10^{-6} $cm^2/V{\cdot}s$ are obtained when experimental data from Tanase et al. [58] are applied to define the density of states in a low doped rr-P3HT. Also, a current ratio of 10^4 is achieved for the simulated OMESFET. Compare to a simulated OFET with the same thickness, the on current, conductance and transconductance in the OMESFET are three orders of magnitude smaller than those in the OFET, because of lower mobility in the OMESFET. In experiment a mobility of 1.6×10^{-4} $cm^2/V{\cdot}s$ is obtained for unintentionally doped rr-P3HT in the OMESFET which is comparable to the mobility in an untreated OFET. The leakage current from the gate has limited the current ratio in the OMESFET to 24.6 which can be enhanced by covering the top surface of the drain and source electrodes (figure 5.14). In general OMESFETs are compatible with the printing methods in which a relatively thick layer of semiconductor can be deposited.

The transverse characteristic of the OMESFET is applied to find the relationship between the depletion width and the gate voltage. The data achieved from the experimental sample suggests some corrections for the applied parameters in the simulation. However, the density of states is

the most important data for the simulation which is dependent on the doping level and the fabrication method.

Focusing on the enhancement OMESFET is encouraged for future research as it is more compatible with low cost electronics. Integration of OMESFETs into circuits requires the design and development of fabrication processes compatible with particular applications, such as AMDs and sensors.

Chapter 6

Dual gate organic transistor

Although the key to achieving ultra low cost electronics is the application of printing methods, the high thickness and poor molecular order in an organic printed transistor lead to poor performance. In this chapter, the effect of the semiconductor thickness on OFET performance is analyzed by introducing a simple model for the device. Application of a Schottky contact as the secondary gate is then proposed to enhance OFET characteristics when a relatively thick semiconductor layer is utilized. The effect of thickness on the OFET characteristics is studied by simulation of the device. Also, the dual gate organic transistor is simulated to show its performance in comparison to an OFET. Then, the performance of a dual gate organic transistor is studied. The simulation results indicate that the performance of a 200 nm thick dual gate transistor is better than that in a 20 nm thick OFET [119]. The dual gate structure is implemented in a 250 nm thick OFET which resulted in a shift of 12 V in the threshold voltage and an increase in the current ratio [120]. The work presented in this chapter does not seek to improve performance by reducing voltage, but rather to show that existing OFET technology can be made more suitable for low cost fabrication methods by the use of a dual gate structure.

6.1 Introduction

The motivation for creating a transistor that works effectively despite having a thick semiconducting layer is strong, as mentioned in previous chapters. Among different techniques, printing methods are the most inexpensive patterning and deposition processes with the capability of roll-to-roll production of organic electronics. However the resulting device performance is relatively poor because the deposited film is too thick and has a poor molecular order [121]. Most of the simple printing techniques such as stamping have a thickness resolution around a few hundred of nanometers [81], whereas the optimum thickness for an OFET is about 30 nm [115]. Many research groups around the world are working on the development of printing techniques to meet the organic electronics requirements [21]. However, the price of advanced printing machines affects the cost of the product especially in low production quantities. Also, to build organic transistors on non smooth substrates such as fabrics for

wearable electronics the thickness of the semiconductor often has to be more than the surface roughness to produce an electrically continuous film. Therefore, a method of making organic transistors with reasonable performance from a few hundreds nanometer thick organic semiconductor layers will help enable low-cost production and widespread use of the organic electronics.

6.2 Modeling

The effect of the semiconductor thickness on a few parameters of an OFET has already been studied through modeling and experiments [122]. In this section an analytical model is presented which predicts most of the important DC characteristics of an OFET including the threshold voltage, output resistance, off current and the on/off current ratio.

As explained in chapter 5, an OFET (figure 6.1.a) is in the accumulation mode when the transistor is on. In this case, the applied gate voltage accumulates carriers at the insulator-semiconductor interface to increase the conductance between the drain and the source contacts. The depth of the accumulation layer is about 2 to 3 nm which is equal to a few monolayers of the organic semiconductor [110]. The remaining thickness in the semiconductor acts as a resistor between the drain and source. Excluding the effect of the resistor, similar to any Isolated Gate Field Effect Transistor (IGFET), the output characteristic of the transistor shows two distinct regimes: linear and saturation. When $|V_{GS}-V_T| > |V_{DS}|$ the transistor is in the linear regime, whereas for $|V_{GS}-V_T| < |V_{DS}|$ the transistor is in the saturation regime. Ideally, in the off mode, the transistor has a zero conductance between the drain and source when $|V_{GS}| < |V_T|$.

Figure 6.1 shows a schematic of a bottom contact OFET with an equivalent circuit for the device, in which the effect of the bulk resistance is represented by the parallel resistor. Assuming that the thickness of the semiconductor is much larger than the depth of the accumulation layer, this parallel resistance, $R_{P,}$ is expressed by:

$$R_P = \frac{L}{\sigma_{blk} Z t_s} \tag{6.1}$$

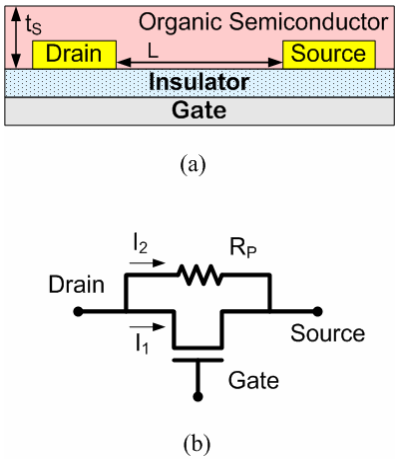


Figure. 6.1. (a) A schematic of a bottom contact OFET and (b) a simple model for the device consisted of an ideal IGFET and a parallel resistor.

where L is the distance between the drain and source, Z is the width of the drain/source electrodes. t_s is the thickness of the semiconductor in the channel and σ_{blk} is the bulk semiconductor conductivity.

The current in the transistor element (I_1) is a function of the gate voltage. In the linear regime, I_1 is [21]:

$$I_{1-Lin} = \left(\frac{Z\mu_f C_i}{L}\right)\left[(V_{GS} - V_T)V_{DS}\right] \tag{6.2}$$

where C_i is the gate capacitance per unit of area and μ_f is the field effect mobility of the carrier in the channel. For the saturation regime, the current is a quadratic function of the gate voltage [21]:

$$I_{1-sat} = \left(\frac{Z\mu_f C_i}{2L}\right)(V_{GS} - V_T)^2 \tag{6.3}$$

and in the off mode, ideally $I_{1\text{-}off} = 0$.

According to the model the drain terminal current for the device is the summation of the currents in the transistor and the resistor. Therefore, the current in the linear regime is:

$$I_{D-lin} = I_{1-Lin} + I_2 = \left(\frac{Z\mu_f C_i}{L}\right)\left[(V_{GS} - V_T)V_{DS}\right] + \frac{V_{DS}}{R_P} \tag{6.4}$$

Inserting R_P from equation 6.1 into equation 6.4 and rearranging after, gives:

$$I_{D-lin} = (\frac{Z\mu_f C_i}{L})[V_{GS} - V_{Tapp}]V_{DS} \quad (6.5)$$

where V_{Tapp} is the apparent threshold voltage described by:

$$V_{Tapp} = \left(V_T - \frac{\sigma_{blk} t_s}{\mu_f C_i} \right) \quad (6.6)$$

As equation 6.5 and 6.6 suggest, the effect of the parallel resistor appears only in the threshold voltage of the device in the linear mode. Therefore, the field effect mobility can be calculated from the slope of I_D-V_{GS} plot [21] in the linear regime regardless of the semiconductor thickness, but the apparent threshold voltage is a function of the thickness. Indeed, for a very thick semiconductor, especially when the bulk conductivity is relatively high, the sign of the apparent threshold voltage is different from V_T which means that the transistor can not be switched off even at V_{GS} =0. Such a case is very likely to happen in a printed device where it is common that both the semiconductor layer is thick and the background doping is relatively high. The OFETs presented in chapter 5 (figure 5.8) are suffering from the same effect.

An effect of the parallel resistor is that the saturation current is dependent of V_{DS}, and the slope of the I_D-V_{DS} curve is R_P^{-1}:

$$I_{D-sat} = (\frac{Z\mu_f C_i}{2L})(V_{GS} - V_T)^2 + \frac{V_{DS}}{R_P} \quad (6.7)$$

Since R_P is proportional to the inverse of the semiconductor thickness, the slope of the current in I_D-V_{DS} increases with the thickness (t_s). Indeed, R_P is the output resistance (R_{out}) of the device in the saturation regime, which drops with increasing semiconductor thickness. Also, equation 6.7 indicates that derivation of the field effect mobility from $\sqrt{I_D}$ - V_{GS} curve is not accurate in the saturation regime, except when R_P is very large.

Furthermore, the semiconductor thickness has a significant effect on the off mode of the device as the current is not zero when $|V_{GS}| < |V_T|$. Assuming that the transistor is off (ideal transistor) when V_{GS}=0, the device behaves as a resistor between the drain and source terminals. The value of the resistance in the off mode (R'_P) is actually different from the bulk resistance (R_P) because

of the depletion region produced from the energy bending at the V_{GS}=0. Figure 6.2 depicts the energy bending at zero gate voltage for a p-type Metal- Insulator-Semiconductor (MIS) device. Because of the depletion region, the effective thickness of the semiconductor is t_s-t_{dep}. Therefore R'_P is expressed as:

$$R_P^{'} = \frac{L}{\sigma_{blk} Z\left(t_s - t_{dep}\right)} \tag{6.8}$$

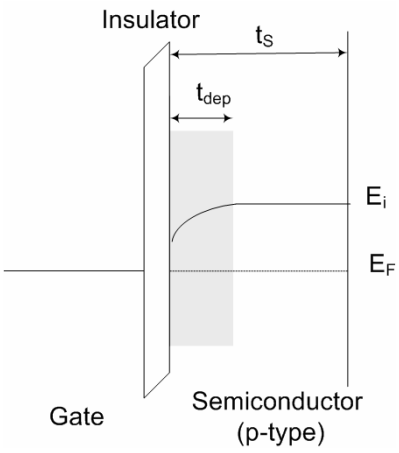


Figure. 6.2. The energy diagram for a MIS device at the equilibrium (V_{GS}=0).

and consequently the off current is:

$$I_{D-off} = \frac{\sigma_{blk} Z\left(t_s - t_{dep}\right)}{L} V_{DS} \tag{6.9}$$

To reduce the off current, one can apply a large enough voltage to the gate in the depletion mode to extend the depletion region close to t_s. For a thick layer of the semiconductor the required gate voltage is so high that insulator breakdown will likely occur before the semiconductor can be fully depleted. In a very thin semiconductor layer, t_s might be even smaller than t_{dep} which in this case, the depletion region is restricted to the semiconductor thickness and the semiconductor is fully depleted at V_{GS} = 0. When the entire thickness of the semiconductor is depleted the off current is determined by the conductivity of the depleted region rather than the bulk mobility and t_S is considered as the thickness.

Considering V_{GS} = 0 as the off state, the on/off current ratio is written in the linear mode by taking the ratio of equations 6.5 and 6.9:

$$\frac{I_{on}}{I_{off}} = \left(\frac{\mu_{field} C_i}{\sigma_{blk}(t_s - t_{dep})}\right)\left[V_{GS} - V_{Tapp}\right] \tag{6.10}$$

The current ratio drops with increasing semiconductor thickness, and there is also an influence due to a shift in the apparent threshold. Equation 6.10 also suggests that the current ratio is independent of the channel length (L) and width (Z). Increasing the value of R_P by changing L and/or Z does not improve the current ratio.

In summary, the modeling presented above suggests that the thickness of the semiconductor has negative effects on the apparent threshold voltage, output resistance, and the on/off current ratio. Hence, the performance of the device improves with a reduction in the semiconductor thickness. Theoretically, the peak performance is achieved when the semiconductor is just as thick as the depth of the accumulation layer, which is less than 3 nm. In practice, such a thin film is hard to make continuous and shows a poor current ratio due to the contact resistances and leakage current in the off mode [115]. Consequently, the optimum thickness is measured to be around 30 nm [115]. Most of the inexpensive deposition methods such as printing or dip casting create films that are much thicker than 30 nm. As a result the performance is very poor in the devices made with these simple methods relative to those made by evaporation techniques.

This simple model of the effects of thickness will be used below to help explain results from simulations and experiments.

6.3 Structure and operation of the dual gate organic transistors

To reduce the effect of the thickness on device performance a secondary gate is suggested on top of the semiconductor. The top gate (TG), shown in figure 6.3, makes a Schottky contact with the semiconductor, which produces a depletion region in the semiconductor with a depth of t_{Sch}. The effective semiconductor thickness in the linear and saturation regimes is then t_s-t_{Sch}, and it is t_s-t_{Sch}-t_{dep} in the off mode. As it is already discussed t_{Sch} increases with applied voltage in the reverse bias which shrinks the effective semiconductor thickness. The absence of the insulator between the top gate and the semiconductor is an advantage for extending t_{Sch} to a much larger distance than t_{dep} can reach for the same voltage applied to the gates. At a certain voltage applied to the top gate, V_{TG}, such that $t_s = t_{Sch}$, the depletion region is extended through the semiconductor thickness and the effect of the parallel resistance is eliminated.

The dual gate transistor consists of an OFET and an OMESFET. The accumulation mode is controlled in the transistor by the OFET gate, whereas the OMESFET governs the depletion mode in the device. Also, the dual gate transistor can resemble a MOSFET transistor in which the Schottky gate contact behaves as the body contact. Nevertheless, the secondary gate is controlling the effective thickness of the semiconductor layer.

Simulations were done in order to verify the effectiveness of the top gate and the correctness of the simple model of the effects of thickness. Experiments were then carried out to demonstrate the effect of a top gate on OFET performance.

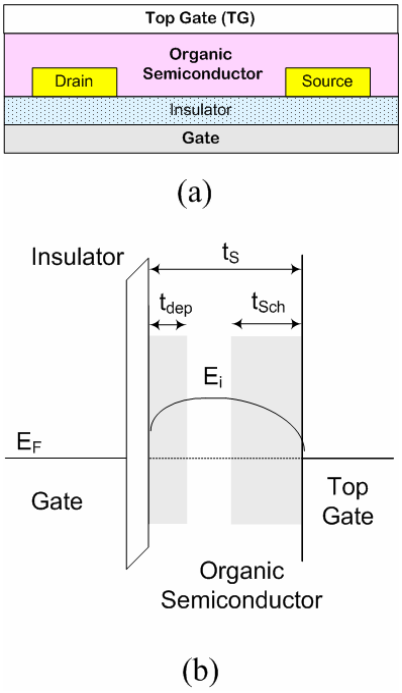


Figure. 6.3. (a) A schematic of a dual gate OFET and (b) the energy diagram at the both gate interfaces (equilibrium condition – V_{GS} =V_{TG} = 0V).

6.4 Simulation

A set of transistors are simulated with organic layer thicknesses ranging from 20 nm to 200 nm, with the thickest layer mimicking a device made by a low-cost printing method [81]. In addition the dual gate configuration is applied on the 200 nm thick film to show the enhancement in the performance of the device. Rr-P3HT is chosen as the semiconductor layer in the devices.

Medici version 4.0 is used as the CAD tool for the device simulation. The input codes are presented in appendix B and the parameters for the organic semiconductor are set as explained

in chapter 3. Since the parameters that we have assigned to rr-P3HT are not accurate, as determined in chapter 5, the simulation results are very likely to be different from the experimental results. However, the focus of the simulation is not on a specific semiconductor, but to study the effect of the thickness and find a solution for the loss in performance observed in thick film transistors.

In the simulation gold is chosen for the drain and source electrodes so that these act as the ohmic contact [40] and aluminium is used for the gate. Also, aluminium is used for the top gate as it makes a Schottky contact with the semiconductor [40]. In the OFETs, SiO_2 is chosen as the insulating layer, with a thickness of 200 nm as most of the time such a thickness is required for a low leakage current. The channel length (L) is set to 4 μm and as mentioned the width (Z) is normalized to 1 μm by default in Medici.

6.4.1 **Simulation results in OFETs with various thicknesses**

To study the effect of the semiconductor thickness on the transistor characteristic in the linear regime, V_{DS} is held at -0.5 V and V_{GS} is scanned from 0 to -40 V. Figure 6.4 shows the transverse characteristic (I_D-V_{GS}) of the device for 20 nm, 100 nm, and 200 nm OFETs in a semi-log plot. The current overlap in the range of -40V < V_{GS} < -20V suggests that gate voltage is sufficiently higher than the threshold voltage for the all thicknesses that the parallel resistance has a little effect.

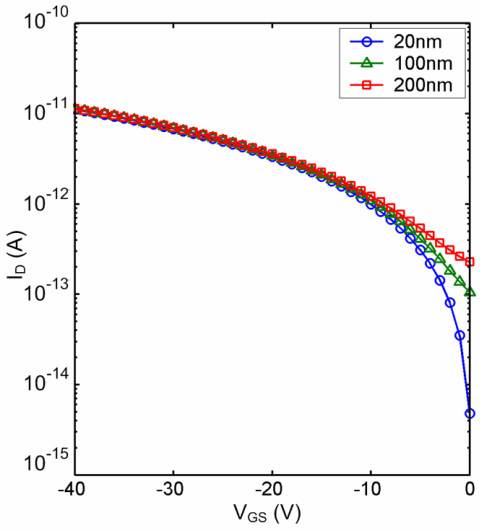


Figure. 6.4. The transverse characteristics of the simulated OFETs with the different semiconductor thicknesses (V_{DS}=-0.5V).

According to equation 6.5, V_{Tapp} is obtained by fitting a linear function to the I_D-V_{GS} curve when $|V_{GS}| > |V_T|$ and finding the voltage intercept. The apparent threshold voltages are obtained for 11 transistors with different thicknesses by the same method and their variations with the thickness is indicated in figure 6.5.

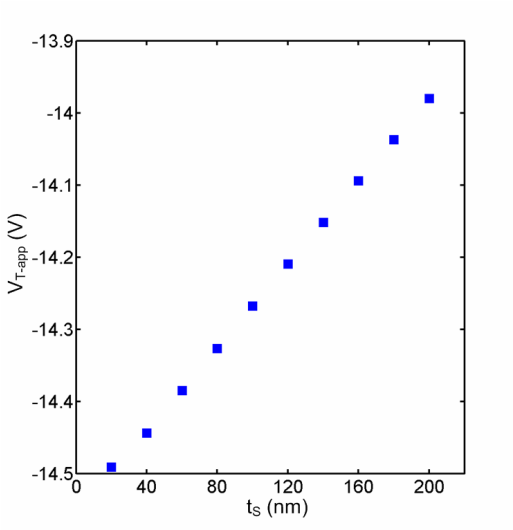


Figure. 6.5. The variation of V_{Tapp} in the simulated OFETs with the semiconductor thickness (V_{DS}=-0.5V).

As equation 6.6 predicts, the apparent threshold voltage is linearly dependent on the semiconductor thickness and it is shifted to the lower magnitudes as thickness is increased. For the selected parameters in the simulation the change in the threshold voltage is about 0.5V when the thickness is changed from 20 nm to 200 nm.

The saturation regime in the transistors is studied by application of -40 V to the gate electrode and scanning the drain voltage from 0 to -60 V. The output characteristic (I_D-V_{DS}) of transistors for three different thicknesses are plotted in figure 6.6. The differences in the slopes in the saturation regimes indicate the dependence of the output resistance on the thickness of the semiconductor as equation 6.7 suggests (the thickest layer has the lowest resistance). The output resistances calculated from the output characteristics (I_D-V_{DS}) are shown versus the semiconductor thickness in figure 6.7. A drop of 300 GΩ (equal to 26%) is observed in the output resistance when the thickness is increased from 20 nm to 200 nm.

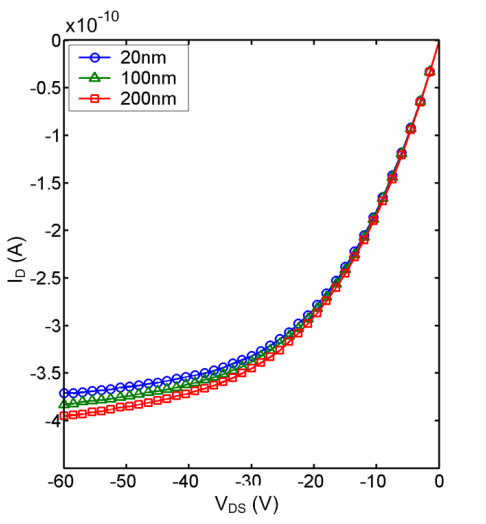


Figure. 6.6. The output characteristics of the simulated OFETs with the different semiconductor thicknesses (V_{GS}=-40V).

The current ratio and the off current are obtained from the simulation results shown in figure 6.4. The I_D values at V_{GS} = -40 V are considered as I_{on} whereas the currents at V_{GS} = 0 V are taken as I_{off}. Figure 6.4 shows a rapid drop of the current below the threshold voltage for 20 nm thick OFET, but the rate is much lower for the thick film transistors. In figure 6.8 the off current and the on/off current ratio are shown versus the semiconductor thickness. An approximately two orders of magnitude rise in the off current is the effect of increasing the thickness from 20

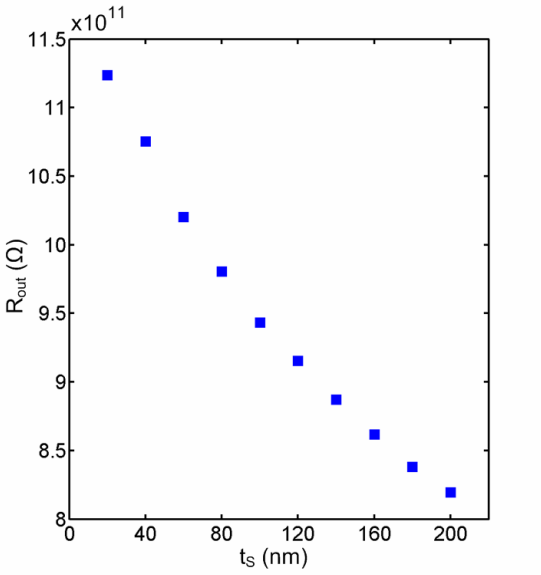


Figure. 6.7. The variation of the output resistance in the simulated OFETs with the semiconductor thickness (-60 V < V_{DS} <-40 V and V_{GS}=-40 V).

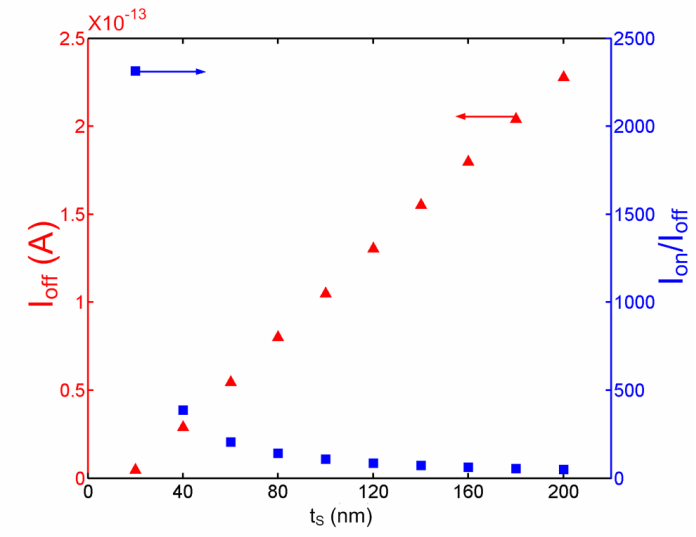


Figure. 6.8. The variation of the off current and the on/off current ratio in the simulated OFETs with the semiconductor thickness (V_{DS}=-0.5V).

nm to 200 nm. Extrapolating the off current in figure 6.8 to cross the thickness axis gives t_{dep}= 16 nm for V_{GS}=0. The current ratio decreased from 2300 to 20 for the same range of the semiconductor thickness. A very rapid increase of the current ratio from 40 nm to 20 nm is predicted by the simulations as the semiconductor thickness, t_S, approaches the depletion depth, t_{dep} (equation 6.10).

The simulation results show that the 200 nm thick OFET has a poor performance relative to the 20 nm transistor, especially in current ratio. 200 nm is a reasonable thickness for most of the low-cost printing methods and is generally needed in order to obtain an electrically continuous film, making it presently impractical to achieve the excellent performance in thinner devices using inexpensive processing. A 200 nm-thick dual gate organic transistor is simulated in order to compare its electrical characteristics with those in the OFET.

6.4.2 **Simulation results in a dual gate organic transistor**

The top gate material is aluminium and makes Schottky contact with the organic semiconductor [40]. To avoid the current leakage through the top gate (TG), a positive potential has to be applied to TG, which drives the Schottky junction in the reverse bias.

To find out the depth of the depletion region from the top gate (t_{Sch}) at different voltages, the transistor is biased at V_{GS} = 0V and V_{DS} = -0.5V and then the V_{TG} is scanned from 0 to 6 V to

measure the off current. Figure 6.9, shows the variation of the off current versus the top gate voltage in a semi-log plot.

A voltage of about 5.4 V on the top gate is sufficient to deplete the entire semiconductor layer, which reduces the off current by more than four orders of magnitude. Above that voltage, the current saturates with the remaining current due to the finite but very small conductance in the depletion region.

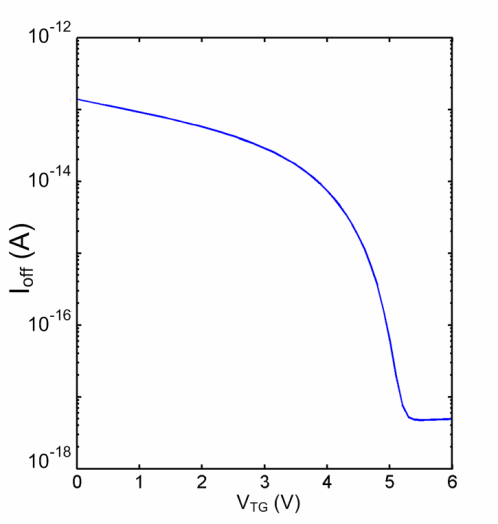


Figure. 6.9. The variation of the off current in the simulated 200 nm-thick dual gate OFET with the Top Gate voltage (V_{DS}=-0.5V and V_{GS}=0V).

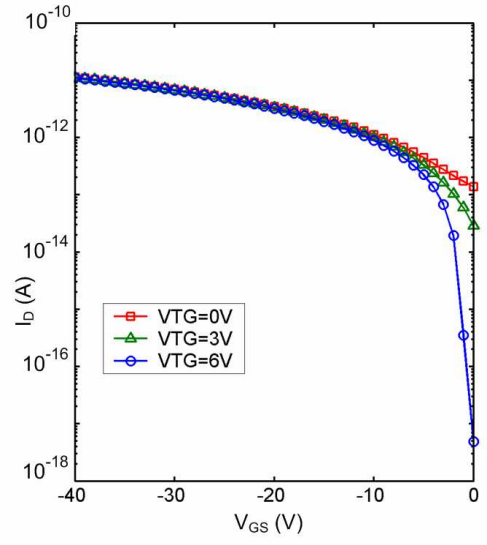


Figure. 6.10. The transverse characteristics of the simulated 200 nm dual gate OFET at different Top Gate biases (V_{DS}=-0.5V).

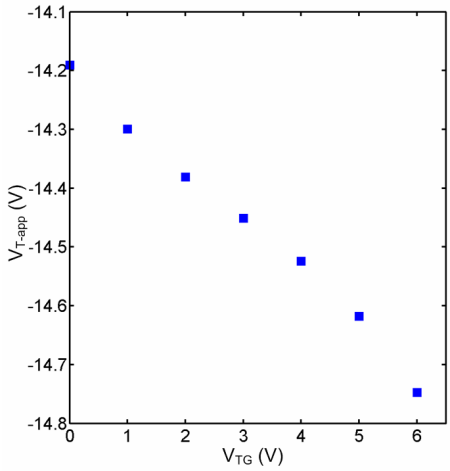


Figure. 6.11. The variation of the apparent threshold voltage in the simulated 200nm-thick dual gate OFET with the Top Gate voltage (V_{DS}=-0.5V and V_{GS}=-40V).

To study the effect of the top gate voltage on the linear regime, the drain-source voltage is held at -0.5 V when the gate voltage is scanned from 0 to -40 V for discrete values of V_{TG} from 0 to 6 V. Figure 6.10 shows the results of the simulation for three different values of top gate voltage. Similarities between figures 6.4 and 6.10 indicate that the top gate is controlling the effective thickness of the semiconductor.

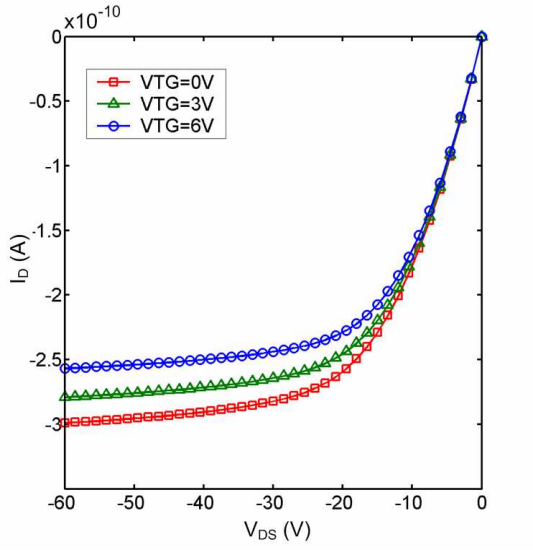


Figure. 6.12. The output characteristics of the simulated 200nm dual gate OFET in different biases of the Top Gate (V_{GS}=-40V).

The effect of V_{TG} on the apparent threshold voltage is shown in figure 6.11. Application of 6 V to the top gate has changed V_{Tapp} for more than 0.5 V. Comparing values in figures 6.5 and 6.11 indicates that when V_{TG} =5 V the threshold voltage in a 200 nm thick dual gate OFET is the same as that in the 20 nm OFET.

The output resistance of a dual gate OFET in the saturation mode is, also, controllable using V_{TG}. The output characteristic of the device (I_D-V_{DS}) is simulated for discrete values of V_{TG} from 0 to 6V when V_{GS} = -40 V. The results show a reduction of the current slope as the top gate voltage is increased, which is just visible in figure 6.12. The estimated output resistances at different top gate voltages are plotted in figure 6.13, which more clearly indicates the change of the output resistance with top gate voltage. Comparing values in figures 6.7 and 6.13, the output resistance is 2.5 times larger in the dual gate transistor when V_{TG} = 6 V than that in the 20 nm thick OFET.

Also, the on/off current ratio is improved in the dual gate structure as the off current is reduced from 10^{-13} to 10^{-17}A (figure 6.9) when the top gate voltage is changed from 0 to 6 V. A ratio more than 10^6 is achieved for a 200 nm thick dual gate OFET (figure 6.14), whereas the ratio is about 200 for an OFET with the same thickness.

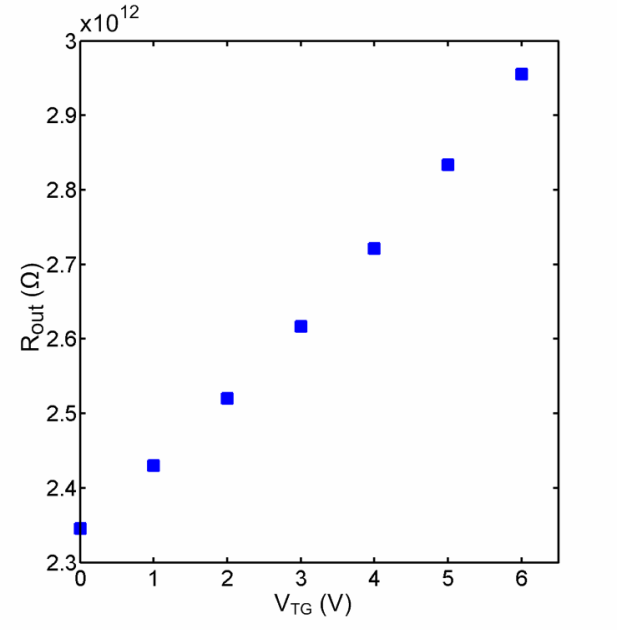


Figure. 6.13. The variation of the output resistance in the simulated 200 nm-thick dual gate OFET with the Top Gate voltage (-60<V_{DS}<-40V and V_{GS}=-40V).

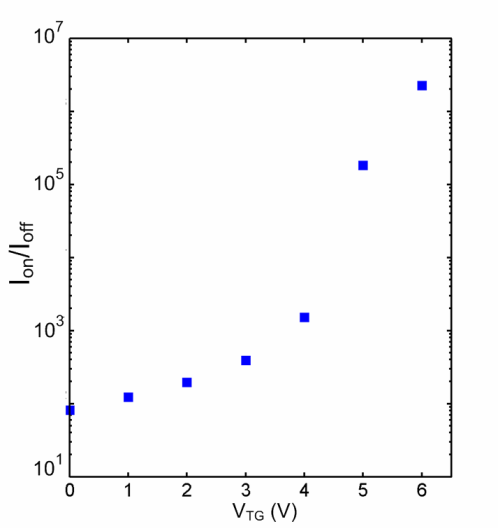


Figure. 6.14. The variation of the on/off current ratio in the simulated 200nm-thick dual gate OFET with the Top Gate voltage (V_{DS}=-0.5V).

6.5 Experimental results

Although the simulation results suggest that the performance of a dual gate thick film organic transistor can be better than that of a thin film OFET, the approach has some practical challenges. The most important one is the voltage stress between the top gate and the drain when the drain voltage reaches to -60 V. Such a large reverse voltage across the Schottky junction might cause breakdown in the device. In practice, the dual gate transistor approach is probably most suitable for a low voltage OFET or for limited drain voltage. These considerations restrict the operation modes to either the off mode or to the linear regime.

In the simulation a gate voltage range of 40 V was chosen for 200 nm thick silicon dioxide, which is reasonable for a defect free SiO_2. In practice, it was not possible to apply a voltage above 20 V in a 350 nm thick SiO_2 because of the low quality of the insulating layer. Therefore, a thick layer OFET was built and characterized over a limited voltage range so as not to damage the device. The secondary gate is then deposited over the OFET and the dual gate transistor is tested without connecting the top gate to any potential in order to reduce the voltage stress across the Schottky contact. The natural depletion region produced by the Schottky contact at equilibrium reduces the effective thickness of the organic layer and causes changes in the OFET characteristic. Despite these limitations, the experiment is performed to help investigate the feasibility of implementing a dual gate transistor for a thick layer of

semiconductor. The simulation results are a guide to the performance improvements that are ultimately possible with the addition of a top gate, given state of the art processing methods used in OFET fabrication.

A micro-electrode (figure 3.1) is applied to build a thick OFET and a dual gate organic transistor. n-doped silicon provides the gate in the OFET with 350 nm thick silicon dioxide as the insulator. Two of the gold electrodes, each having a length of 0.5 mm and a gap of 4 μm, are assigned as the drain and the source connections. After cleaning with piranha a 350 nm thick rr-P3HT layer is deposited on the micro-electrode by dipping it into a solution of 0.8% (weight) of the polymer in chloroform and pulling it out slowly. The sample is then held at 100 °C for 20 minutes to remove the solvents from the film before characterization. The rr-P3HT deposition and electrical tests are done in a dry nitrogen filled glove box.

Figure 6.15 shows the output characteristics of the OFET at various gate voltages. The very thick semiconductor layer makes the I-V curve nearly linear with an inverse slope of 357 MΩ at V_{GS} = 0 V. Also, the current ratio at V_{DS} = -20 V is only 5 over a 20 V range in the gate voltage. The mobility and the apparent threshold voltage are found to be 3.24×10^{-4} $cm^2/V\cdot s$ and 12.5 V, from equation 6.5. The measured mobility is in agreement with previously reported values [60] and our experimental results in chapters 4 and 5. The positive value of threshold voltage is undesired for a p-type transistor. The very large positive V_{Tapp} results from the low field effect mobility, the high conductivity in the bulk semiconductor (high background doping), and the substantial thickness of the polymer (equation 6.6). Also, the 350 nm thick SiO_2 is introducing a relatively low capacitance (C_i = 9.8 nF/cm^2).

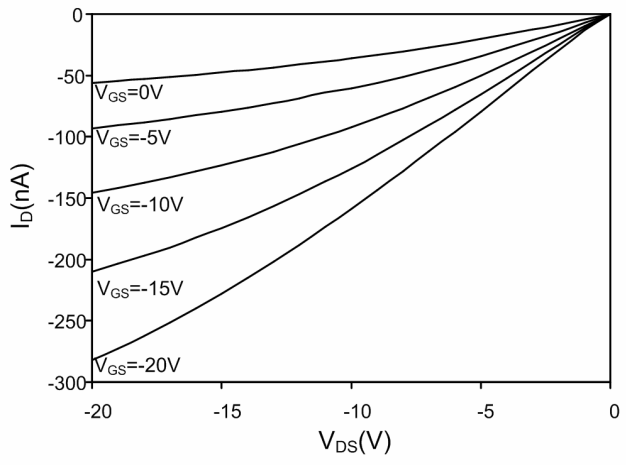


Figure 6.15. The measured output characteristics of a thick-film OFET.

To deposit the top gate the device is transferred to a thermal evaporator without exposing the sample to the air. 110 nm of aluminium is then deposited over the semiconductor layer at a rate of about 1 Å/s. The device is tested as an OFET without any electrical connection to the top gate. Since, the depletion region produced by the top gate has an insulating property the device is expected to behave as an OFET with a reduced semiconductor thickness.

The output characteristics and the schematic of the device after aluminium deposition are shown in figure 6.16. The appearance of the saturation regime in the plot indicates an increase in R_P. The current ratio is enhanced to 20.5 (from 5.2) for the same gate voltage range and the threshold voltage has changed to -0.01V. Although the change in threshold voltage is significant the threshold is not sufficient to switch the transistor off at V_{GS} = 0V, and because of this, the current ratio is still low. The mobility is unchanged, as expected. The value of R_P is estimated to be 4.85 GΩ from the slope of the plot at V_{GS} = 0V, more than ten times larger than the value estimated from figure 6.15.

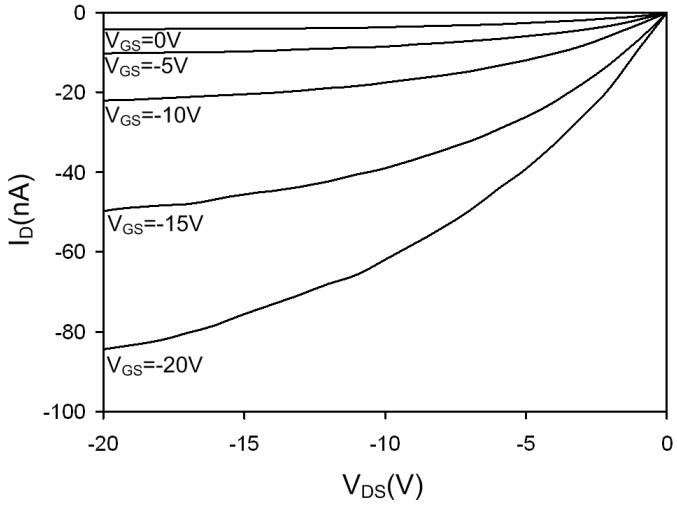


Figure 6.16. The output characteristics of an OFET following aluminium deposition over the semiconducting layer (Dual gate organic transistor).

An alternative explanation for the change in R_p is that the doping density of the organic semiconductor might have been reduced when it was under vacuum during aluminium deposition [32]. This was tested by making an OFET and measuring its output characteristic

before and after storage in a vacuum of 10^{-5} torr for an hour. Negligible changes in the I-V curve strongly suggest that the observed effect in the first sample is due to the formation of a depletion region from the aluminium Schottky contact.

6.6 Discussion

Comparing the experimental results with the simulation, the threshold voltage in the real OFET is very different from what has been predicted. To explain the difference equation 6.6 is written in a new form:

$$V_{Tapp} - V_T = -\frac{\sigma_{blk} t_s}{\mu_f C_i} = -\frac{qN\mu_{blk} t_s}{\mu_f C_i} \tag{6.11}$$

where N is the doping density in the polymer film. In simulation, where the bulk mobility is much lower than the field-effect mobility (see table 5-1), the difference between the apparent and real threshold is small and even variation of the thickness from 20 nm to 200 nm changes the threshold voltage by only 0.5 V. In contrast, in the experiment the field-effect mobility is not much different from the bulk mobility. Substituting measured values into equation 6.11 one finds that the difference between threshold voltages is about 28 V which corresponds to a V_T of 15.5V for a 350 nm thick OFET. The very different mobilities between the high quality lightly doped material used in the simulations and the relatively impure and highly doped polymer used in the experiments thus explains the differences in threshold voltages.

Also, simulation results predicts large current ratio in the dual gate organic transistor whereas the enhancement in the current ratio is relatively small in the experiment. The reason is that in the experiment the top gate is not biased. Figure 6.14 shows that at low voltages (for the top gate) the current ratio is still low, but when the top gate voltage increases the current ratio increases as well. The model suggest what is possible while the experiments show that the basic idea works.

According to equation 6.11, the effective thickness of the semiconductor after aluminium deposition is predicted to be 156 nm which is about 45% of the original thickness.

To enhance the performance of the dual gate transistor a Schottky contact with a breakdown voltage larger than 20 V is required. In such a case the secondary gate can be biased which is then a more effective control on the transistor parameters. Nevertheless, the experimental

result shows the advantages of the application of the dual gate structure over the OFET approach in thick films.

6.7 Summary

To study the effect of the semiconductor thickness, a simple model consisting of an ideal IGFET and a resistor is applied to describe organic field effect transistors. The analytical approach shows degradation of the performance with increasing thickness. The threshold voltage is shifted to more positive values and the output resistance and the current ratio drop. Simulation results from devices with thicknesses of between 20 nm and 200 nm support the model. A linear shift of the threshold voltage of 0.5 V is observed when the thickness is changed. Also, a 26% drop of the output resistance and a tenfold reduction in current ratio are obtained when the thickness is increased from 20 nm to 200 nm.

As a solution a dual gate FET structure is suggested for implementation when there is a poor control over the thickness of the semiconductor layer and/or when the roughness of the substrate determines the minimum thickness of the semiconductor layer. The simulation results for a 200 nm thick dual gate OFET indicate an enhancement in the device performance by changing the secondary gate voltage. Application of 6 V to the top gate has shifted the threshold voltage by 0.5 V. Also, the output resistance is increased by a factor of 2.5. The most significant effect is on the current ratio which is improved by about four orders of magnitude. Altogether, the performance of the simulated 200 nm thick dual gate OFET is better than a simulated 20 nm thick OFET.

In the experiment, the dual gate transistor could not be tested over the full range of the voltage because of the poor quality of the insulator used. A 350 nm thick OFET was fabricated and tested it over a range of 20 V. The device works more as a variable resistor than a transistor due to its large parallel resistance. By applying the secondary gate, the effective cross section of the channel was reduced due to the depletion region. This led to an increase in the transistor's I_{on}/I_{off} and shifted the apparent threshold voltage to enhance the performance of the device.

Chapter 7

Conclusion

In this thesis Schottky diodes, OFETs, OMESFETs and dual gate organic transistors are studied through analytical models, simulations, and experiments. The devices demonstrated here help solve two challenges in organic electronics, namely their need for relatively high voltage operation and their incompatibility with printing techniques. It is demonstrated that low voltage operation of organic transistors can be obtained with reasonable performance using methods compatible with low-cost fabrication. It is also shown that OFETs can be made more compatible with low- cost fabrication methods by adding a second gate, dramatically improving performance.

7.1 Current progress

7.1.1 Organic Schottky Diode

The current in an organic Schottky diode was analyzed using the diffusion model. This model does not rely on the existence of distinct conduction and valence bands in the organic semiconductor. Application of energy bands and classical thermionic models are generally used to describe an organic Schottky diode [44, 59, 72, 123], whereas experiments and models suggest that localized states dominate transport in the organic materials typically used to produce such diodes [44]. Where there is an exponential drop in the density of states away from the mobility edges, as has been observed in many organics, it is shown that the diffusion model predicts an exponential rise in current with voltage, as is commonly observed [44, 59, 72, 123]. In order to validate this model, an important step that needs to be taken is to compare model predictions to measured I-V curves from materials in which density of states and other properties have been measured.

The aging of rr-P3HT based Schottky diodes fabricated in air is studied. Aging effect has been extensively studied in organic Schottky contacts in OLEDs [85-87], but the main concern has been the forward bias characteristics. In this work a resistive characteristic is found in the reverse bias which changes with time, likely due to the oxygen doping effect. In addition an

unexpected steady rise in current at constant voltage in the forward bias is observed in these air-made diodes. The effect produces a positive phase in the impedance at low frequencies. The effect may be due to very slow filling of deep traps. It is described as an apparent inductance.

7.1.2 **Organic metal semiconductor field effect transistor (OMESFET)**

Although the low-voltage operation of organic MESFETs has previously been demonstrated in a few articles [19, 20], the device has never been fully characterized. An objective of this thesis is to evaluate the feasibility of applying OMESFETs as a low-voltage printable organic transistors.

For simulation charge transport in organics is modeled assuming the Multiple Trapping and Release (MTR) mechanism, which is suitable for DC analysis of organic devices at constant temperature [50]. A measured density of localized states in rr-P3HT reported by Tanase *et al* [58] is used in the simulation of organic transistors. The low-voltage operation of the OMESFET is demonstrated in simulation in a thick film geometry, appropriate for printing. The simulation results suggest the possibility of achieving higher current ratio and lower subthreshold swing in the OMESFET than in an OFET with the same dimensions. The primary advantage of the OFET is that it employs field effect mobility, which can be more than an order of magnitude higher than bulk mobility. The operating voltage also allows current to be increased. As a result, except in very thick and highly doped OMESFETs, the conductance, on current and transconductance are all higher than in the OFET. Where current is important and high voltage is not of primary concern, the OFET structure is preferred. The higher mobility will also allow better frequency response for the same channel geometry. Once again these comparisons assume the use of thick semiconductor layers as is currently required in printing approaches.

An OMESFET with a 200 nm thick rr-P3HT, is fabricated The polymer is deposited by dip casting, producing a thick layer similar to that produced by printing methods [81]. The device successfully operates over a voltage range of 5 V, including both in the depletion and enhancement modes. Full measurement of DC characteristics is done which indicates a very low current ratio (<25) in the device. The DC characteristics of the device is compared to a high-performance printed OFET [81] operated with 40 V. The comparison confirms lower mobility in the OMESFET than that in the OFET, which results in lower on current, conductance and transconductance in the OMESFET. To enhance mobility and its related parameters increasing

the doping level and the thickness of the semiconductor layer are recommended. The low current ratio in the OMESFET is likely due to the leakage current through the gate. As a solution, covering the top surface of the drain and source electrodes with an insulating layer is suggested. The mobility and the on current that are achieved in the OMESFET are promising for some low-cost applications such as passive RFIDs, and small AMDs.

In a devised method, the OMESFET structure is applied to measure the variation of the depletion width with the bias voltage across an organic Schottky junction, which indicates an exponential variation of the depletion width with the voltage at reverse or small forward biases.

In summary, the OMESFET is shown to achieve low voltage operation. It is also shown to work well with thick layers of semiconductor. Its main limitations compared to the OFET are lower mobility (and thus speed), and lower current output. Where these properties are important, a dual gate device is suggested as an improvement on the OFET.

7.1.3 **Dual gate organic transistor**

The effect of the semiconductor thickness on OFET performance has previously been studied experimentally [122]. In this work the effect is studied through an analytical model and simulation. Variation of the threshold voltage, and reductions in the output resistance and the current ratio are predicted from the model when the semiconductor thickness increases. The effect of the thickness is studied by simulating rr-P3HT based OFETs with thicknesses from 20 nm to 200 nm. Variation of parameters as thickness is changed in simulated transistors confirms the model predictions. Since the performance of OFETs drops when a thick film semiconductor is applied, the dual gate organic transistor is devised to achieve high performance in such a circumstance. A depletion region, produced from the Schottky contact between the secondary gate and the semiconductor, controls the effective thickness of the semiconductor by the secondary gate voltage. Simulation results from a 200 nm thick dual gate organic transistor show increases in the output resistance and the current ratio over what is predicted for a standard OFET. The voltage at the secondary gate can be used to tune the threshold voltage. In the simulation a 200 nm thick dual gate organic transistor performed better than a 20 nm thick OFET, and in particular demonstrated a substantially higher current ratio.

The advantages of the dual gate transistor are demonstrated by shifting the measured threshold voltage in an OFET from 12.5 V to -0.1 V and increasing the measured current ratio by a factor

of 4 after depositing the secondary gate, on a 350 nm thick semiconductor layer. The breakdown voltage of the Schottky contact prohibited exploring further advantages of the dual gate transistor in practice. If the full benefits of this new device geometry are to be exploited, a Schottky contact with a breakdown voltage of about 40 V is needed, as opposed to the 20 V demonstrated in this work.

From these contributions to the study of organic electronic devices, I may conclude the following:

1. To model the current in an organic Schottky contact the diffusion model is applied which it predicts exponential rise of the current in a limited range of the voltage for an exponential distribution of localized states.

2. The reverse current in an air-made organic Schottky diode is dominated by a resistive characteristics resulted from the oxygen effect on the organic.

3. Organic Schottky diodes made in air mimic an inductive behaviour at low frequencies when the voltage is above a threshold voltage.

4. For a thick film semiconductor possibly deposited by a printing technique the OMESFETs perform better than OFETs in terms of voltage range.

5. The mobility in OMESFETs is lower than that in OFETs (providing the OFET surface preparation is good and the doping level is low). Therefore, for situations which need high speed and high on current OFETs are expected to be better than OMESFETs.

6. The leakage current at the gate terminal is a limiting parameter in the performance of OMESFETs, which reduces the current ratio in practice. Suggestions are made for reducing this effect.

7. The OMESFET structure appears to be a good method to estimate the depletion width in an organic Schottky contact.

8. The bulk semiconductor in an OFET can be modeled as a resistor parallel to the drain and source contacts of the transistor. This helps analyze the variation of the transistor parameters with the semiconductor thickness.

9. A dual gate organic transistor may be used in thick film semiconductors, possibly deposited by a printing method, to overcome the disadvantages of thick semiconductor layers in OFETs.

10. The voltage range and mobility challenges in dual gate organic transistors are same as those in OFETs, but the current ratio and the threshold voltage can be significantly enhanced in the dual gate approach compared to those in an OFET.

7.2 Future work

The achievements this research can be continued in a number of ways, as are now described.

7.2.1 Organic Schottky contact

In order to apply the Schottky contact more effectively in the OMESFET and the dual gate organic transistor, a very low reverse current is necessary. Application of a metal with a work function lower than aluminium ($q\varphi_{Al}$ = 4.28eV) such as magnesium ($q\varphi_{Mg}$ =3.66eV) is a suggestion that potentially can reduce the reverse bias current as the injection of holes from the metal to the semiconductor drops.

The AC characteristics of the organic Schottky diodes fabricated as part of this work also need to be improved to obtain higher bandwidth in the OMESFET. Since the parasitic capacitance (see section 4.6.3.2.1) is limiting the bandwidth of the diode, fabrication of micro-electrodes on a thick insulating substrate is highly recommended. In the absence of the parasitic capacitance the bandwidth should extend to a few MHz, as demonstrated in an organic Schottky diodes of similar structure [124].

In order to obtain a fully organic diode the metal contacts in the diode can be replaced with organic conductors. This replacement may make processing easier. Ohmic contact between rr-P3HT with Poly(3,4-ethylenedioxythiophene) - Polystyrene Sulfonate (PEDOT-PSS) has been demonstrated by others [38]. The work function of a conducting polymer is a function of oxidation state. Therefore, a low work function gate material is likely to be obtained by reducing a conducting polymer, e.g. polypyrrole, which can then be used as the Schottky contact.

7.2.2 **Organic transistors**

The poor current ratio in the OMESFET presented in this thesis may limit immediate application. The off current can likely be reduced by covering the top surface of the drain and the source contact with an insulating layer (figure 5.17). To do so, during the fabrication of micro-electrodes the gold layer can be coated with an insulating layer, e.g. Si_3N_4, before the lift off step. In order to have a low contact resistance from the sides of electrodes, use of gold that is a few hundred nanometers thick is suggested for the source and drain electrodes. Also, the application of a metal with a work function lower than the aluminium likely will increase the current ratio in the OMESFET.

Fabrication of an OMESFET on a flexible substrate using a printing method such as inkjet printing is highly recommended for future work, because it will demonstrate the advantages of simplicity and compatibility with the printing methods. In order to do this it is essential to find a processable low work function material, as mentioned in the previous section.

Fabrication of an OMESFET with a doped semiconductor layer is also suggested to enhance the mobility. $FeCl_3$ is a common agent that behaves as a dopant in most of the conducting polymers [125]. With the application of a doped polymer higher mobility, on current and transconductance are predicted.

The simulation results can be updated using the parameters obtained from measurements of transistor properties. The density of states, the most critical parameter, needs to be measured to obtain more reliable results. Admittance spectroscopy is one possible method that can be used to estimate the density of states.

The performance of the thick film dual-gate organic transistor demonstrated in this work was limited by the breakdown voltage of the Schottky junction. The breakdown voltage will likely be increased by the application of a very thin insulating layer (a few nano meters) between the top contact and the semiconductor. The trade off is a reduction in the sensitivity of the depletion width to gate voltage.

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Appendix A

A.1 Matlab code to convert a Medici output file to an spread sheet format.

```
function y = mediciconv(filename)
                                        % Search for number of string matches per line.
fid = fopen(filename, 'r');             % open the Medici file
outfname=sprintf('%s.xls',filename);    % assign an excel file for the output
fod=fopen(outfname,'w+');
i = 0;
y = 0;
while feof(fid) == 0
  tline = fgetl(fid);                   % read a line from the source file
  matches = findstr(tline, '+ ');       % look for '+" sign
  num = length(matches);                % find the location of '+'
  if num == 0
     if y > 0
        s1 = sprintf('%s %s',s1,tline ) % adjoin the line to the last line
        y=0;
        fprintf(fod,'%s\n',s1);         % save the whole as a line in the output file
     end
  else

    if   y==0
       s1=sprintf('%s',tline);          % initiate a line for the output file
       y=1;
    else
     s1 = sprintf('%s %s',s1,tline );   % adjoint the line to the last line
     y=1;
    end
  end
end
fclose(fod);                            % close files
fclose(fid);
```

Appendix B

B.1 Medici input code to simulate an organic Schottky diode

```
TITLE                   Schottky Diode Au/P-type semiconductor/Al with traps
COMMENT                 April24, 2006


ASSIGN          NAME=width      N.VALUE=12.0
ASSIGN          NAME=poltck     N.VALUE=0.4
ASSIGN          NAME=autck      N.VALUE=0.02
ASSIGN          NAME=altck      N.VALUE=0.02
ASSIGN          NAME=devtck     N.VALUE=@altck+@poltck+@autck
ASSIGN          NAME=auwid      N.VALUE=4.0
ASSIGN          NAME=alwid      N.VALUE=4.0
ASSIGN          NAME=bandg      N.VALUE=1.7


$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
COMMENT                 Creat the Mesh

MESH                    SMOOTH=1
X.MESH          WIDTH=@width    H1=@width/50
Y.MESH          Y.MAX=@altck    H1=@altck/4
Y.MESH          Y.MIN=@altck    Y.MAX=@altck+@poltck    H1=@poltck/50
Y.MESH          Y.MIN=@devtck-@autck    Y.MAX=@devtck   H1=@autck/4

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
COMMENT                 Specify the device material and regions

REGION          NAME=Semi       SEMICOND
REGION          NAME=AnodeC     SEMICOND
+                       X.MIN=(@width-@auwid)/2
+                       X.MAX=(@width+@auwid)/2
+                       Y.MIN=@devtck-@autck
REGION          NAME=CathodC    SEMICOND
+                       X.MIN=(@width-@alwid)/2
+                       X.MAX=(@width+@alwid)/2
+                       Y.MAX=@altck
ELECTR          NAME=Anod       REGION=AnodeC
ELECTR          NAME=Cathod     REGION=CathodC

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

COMMENT                 Impurity and contacts

PROFILE         UNIFORM         CONC=1E16       P.TYPE
MATERIAL                SEMICOND        PERMITTI=3.0    EG.MODEL=0
+                       EG300=@bandg    AFFINITY=3.3

CONTACT                 NAME=Anod       WORKFUNCTION=5.1
CONTACT                 NAME=Cathod     ALUMINUM

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

COMMENT                 Symbolic
SYMBOLIC                NEWTON CARRIERS=1       HOLES
MOBILITY                MUP0=0.1
MODELS          SRH     FERMIDIR


ASSIGN          NAME=EV         N.VAL=-@bandg/2
ASSIGN          NAME=EC         N.VAL=@bandg/2

TRAP            E1=-0.85  N.TOT="-1E21"             COND="@FNENER=1"
TRAP            E2=-0.82  N.TOT="-4.15128E+20"      COND="@FNENER=2"
TRAP            E3=-0.79  N.TOT="-1.72331E+20"      COND="@FNENER=3"
TRAP            E4=-0.76  N.TOT="-7.15394E+19"      COND="@FNENER=4"
TRAP            E5=-0.73  N.TOT="-2.9698E+19"       COND="@FNENER=5"
```

```
TRAP            E6=-0.70  N.TOT="-1.23285E+19"     COND="@FNENER=6"
TRAP            E7=-0.67  N.TOT="-5.11789E+18"     COND="@FNENER=7"
TRAP            E8=-0.64  N.TOT="-2.12458E+18"     COND="@FNENER=8"
TRAP            E9=-0.61  N.TOT="-8.81971E+17"     COND="@FNENER=9"
TRAP            E10=-0.58 N.TOT="-3.66131E+17"     COND="@FNENER=10"
TRAP            E11=-0.55 N.TOT="-1.51991E+17"     COND="@FNENER=11"
TRAP            E12=-0.52 N.TOT="-6.30957E+16"     COND="@FNENER=12"
TRAP            E13=-0.49 N.TOT="-2.61928E+16"     COND="@FNENER=13"
TRAP            E14=-0.46 N.TOT="-1.08734E+16"     COND="@FNENER=14"
TRAP            E15=-0.43 N.TOT="-4.51383E+15"     COND="@FNENER=15"
TRAP            E16=-0.40 N.TOT="-1.87382E+15"     COND="@FNENER=16"
TRAP            E17=-0.37 N.TOT="-7.77874E+14"     COND="@FNENER=17"
TRAP            E18=-0.34 N.TOT="-3.22917E+14"     COND="@FNENER=18"
TRAP            E19=-0.31 N.TOT="-1.34052E+14"     COND="@FNENER=19"

COMMENT                   Symbolic
SYMBOLIC        GUMM      CARRIERS=0
SOLVE

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

COMMENT                   Symbolic
SYMBOLIC        NEWTON    CARRIERS=1      HOLES
MOBILITY        MUP0=0.1
MODELS          SRH       FERMIDIR
SOLVE

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

COMMENT                   No bias
LOG             OUT.FILE=~/simulate/Aprl24e.wtb
SOLVE    V(Anod)=0 V(Cathod)=0


COMMENT                   No bias
LOG             OUT.FILE=~/simulate/dec15.wtb
SOLVE    V(Anod)=0 V(Cathod)=0

PLOT.1D         POTENTIA  NEG
+               Y.START=0  Y.END=@devtck
+          TOP=1 BOTTOM=-1  COLOR=2
+          X.START=@width/2  X.END=@width/2
+          UNCHANGE LINE=2
+          DEVICE=CP/POSTSCRIPT PLOT.OUT=~/simulate/dec15.ps


PLOT.1D         QFN  NEG
+               Y.START=0  Y.END=@devtck
+          X.START=@width/2  X.END=@width/2
+          COLOR=1
+          UNCHANGE
+          DEVICE=CP/POSTSCRIPT PLOT.OUT=~/simulate/dec15.ps
```

B.2 Medici input code to simulate a 400nm thick OFET

```
TITLE               OFET
COMMENT                     Aprl24, 2006


$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
$           In the original paper the P3HT film has 400nm
$           Al  as the gate
$           100nm SiO2 Au  as the source and drain
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
$           L=4micron and W=1micron
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

ASSIGN              NAME=width          N.VALUE=16.0
ASSIGN              NAME=poltck         N.VALUE=0.4
ASSIGN              NAME=autck          N.VALUE=0.020
ASSIGN              NAME=altck          N.VALUE=0.020
ASSIGN              NAME=oxtck          N.VALUE=0.1
ASSIGN              NAME=devtck         N.VALUE=@altck+@poltck+@autck+@oxtck
ASSIGN              NAME=auwid          N.VALUE=4.0
ASSIGN              NAME=chl            N.VALUE=4.0
ASSIGN              NAME=alwid          N.VALUE=16.0
ASSIGN              NAME=bandg          N.VALUE=1.7


$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
COMMENT                     Creat the Mesh

MESH                        SMOOTH=1
X.MESH              WIDTH=@width        H1=@width/100
Y.MESH              Y.MAX=@poltck       H1=@poltck/50
Y.MESH              Y.MIN=@poltck       Y.MAX=@autck+@poltck                H1=@autck/20
Y.MESH              Y.MIN=@poltck+@autck    Y.MAX=@devtck-@altck            H1=@oxtck/4
Y.MESH              Y.MIN=@devtck-@altck    Y.MAX=@devtck                   H1=@autck/4

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
COMMENT                     Specify the device material and regions

REGION              NAME=Semi           SEMICOND
REGION              NAME=DrainC         SEMICOND
+                   X.MIN=(@width-@chl)/2-@auwid
+                   X.MAX=(@width-@chl)/2
+                   Y.MIN=@poltck
+                   Y.MAX=@poltck+@autck
REGION              NAME=SourC          SEMICOND
+                   X.MIN=(@width+@chl)/2
+                   X.MAX=(@width+@chl)/2+@auwid
+                   Y.MIN=@poltck
+                   Y.MAX=@poltck+@autck
REGION              NAME=Oxdlay         OXIDE
+                   Y.MIN=@poltck+@autck
+                   Y.MAX=@poltck+@autck+@oxtck



REGION              NAME=GateC          SEMICOND
+                   Y.MIN=@devtck-@altck

ELECTR              NAME=Drain          REGION=DrainC
ELECTR              NAME=Source         REGION=SourC
ELECTR              NAME=Gate           REGION=GateC

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

COMMENT                     Impurity and contacts

PROFILE             UNIFORM             CONC=1E16           P.TYPE
MATERIAL            SEMICOND            PERMITTI=3.0        EG.MODEL=0
+                   EG300=@bandg        AFFINITY=3.3
```

```
CONTACT                 NAME=Drain      WORKFUNCTION=5.1
CONTACT                 NAME=Source     WORKFUNCTION=5.1
CONTACT                 NAME=Gate       ALUMINUM

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

COMMENT                 Symbolic
SYMBOLIC        NEWTON CARRIERS=1       HOLES
MOBILITY        MUP0=0.1
MODELS          SRH     FERMIDIR


$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
$
COMMENT         Simulation with traps
$
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

ASSIGN          NAME=EV         N.VAL=-@bandg/2
ASSIGN          NAME=EC         N.VAL=@bandg/2

TRAP            E1=-0.85  N.TOT="-1E21"             COND="@FNENER=1"
TRAP            E2=-0.82  N.TOT="-4.15128E+20"      COND="@FNENER=2"
TRAP            E3=-0.79  N.TOT="-1.72331E+20"      COND="@FNENER=3"
TRAP            E4=-0.76  N.TOT="-7.15394E+19"      COND="@FNENER=4"
TRAP            E5=-0.73  N.TOT="-2.9698E+19"       COND="@FNENER=5"
TRAP            E6=-0.70  N.TOT="-1.23285E+19"      COND="@FNENER=6"
TRAP            E7=-0.67  N.TOT="-5.11789E+18"      COND="@FNENER=7"
TRAP            E8=-0.64  N.TOT="-2.12458E+18"      COND="@FNENER=8"
TRAP            E9=-0.61  N.TOT="-8.81971E+17"      COND="@FNENER=9"
TRAP            E10=-0.58 N.TOT="-3.66131E+17"      COND="@FNENER=10"
TRAP            E11=-0.55 N.TOT="-1.51991E+17"      COND="@FNENER=11"
TRAP            E12=-0.52 N.TOT="-6.30957E+16"      COND="@FNENER=12"
TRAP            E13=-0.49 N.TOT="-2.61928E+16"      COND="@FNENER=13"
TRAP            E14=-0.46 N.TOT="-1.08734E+16"      COND="@FNENER=14"
TRAP            E15=-0.43 N.TOT="-4.51383E+15"      COND="@FNENER=15"
TRAP            E16=-0.40 N.TOT="-1.87382E+15"      COND="@FNENER=16"
TRAP            E17=-0.37 N.TOT="-7.77874E+14"      COND="@FNENER=17"
TRAP            E18=-0.34 N.TOT="-3.22917E+14"      COND="@FNENER=18"
TRAP            E19=-0.31 N.TOT="-1.34052E+14"      COND="@FNENER=19"

COMMENT                 Symbolic
SYMBOLIC        GUMM    CARRIERS=0
SOLVE           V(Drain)=0      V(Gate)=0 V(Source)=0

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

COMMENT                 Symbolic
SYMBOLIC        NEWTON CARRIERS=1       HOLES
MOBILITY        MUP0=0.1
MODELS          SRH     FERMIDIR
SOLVE           V(Drain)=0      V(Gate)=0 V(Source)=0

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$


COMMENT                 IV Curve
LOG             OUT.FILE=~/simulate/ofet/aprl24a.wtz
SOLVE           V(Drain)=-0.5   V(Gate)=0 V(Source)=0
+               ELEC=Gate       VSTEP=-1NSTEP=40
LOG             CLOSE

COMMENT                 IV Curve
LOG             OUT.FILE=~/simulate/ofet/aprl24b.wta
SOLVE           V(Drain)=0      V(Gate)=-40     V(Source)=0
+               ELEC=Drain      VSTEP=-1NSTEP=40
LOG             CLOSE

COMMENT                 IV Curve
LOG             OUT.FILE=~/simulate/ofet/aprl24c.wta
SOLVE           V(Drain)=0      V(Gate)=-30     V(Source)=0
+               ELEC=Drain      VSTEP=-1NSTEP=40
LOG             CLOSE
```

```
COMMENT                 IV Curve
LOG             OUT.FILE=~/simulate/ofet/aprl24d.wta
SOLVE           V(Drain)=0      V(Gate)=-20     V(Source)=0
+               ELEC=Drain      VSTEP=-1NSTEP=40
LOG             CLOSE

COMMENT                 IV Curve
LOG             OUT.FILE=~/simulate/ofet/aprl24e.wta
SOLVE           V(Drain)=0      V(Gate)=-10     V(Source)=0
+               ELEC=Drain      VSTEP=-1NSTEP=40
LOG             CLOSE

COMMENT                 IV Curve
LOG             OUT.FILE=~/simulate/ofet/aprl24f.wta
SOLVE           V(Drain)=0      V(Gate)=0 V(Source)=0
+               ELEC=Drain      VSTEP=-1NSTEP=40
LOG             CLOSE

TITLE           OFET with traps transfer @ VDS=-0.5
PLOT.1D         IN.FILE=~/simulate/ofet/aprl24a.wtz
+               Y.LOG   Y.AXIS=I(Drain)         X.AXIS=V(Gate)
+               COLOR=2
+               DEVICE=CP/POSTSCRIP     PLOT.OUT=~/simulate/ofet/Aprl24g.ps

TITLE           OFET with traps transfer @ VDS=-0.5
PLOT.1D         IN.FILE=~/simulate/ofet/aprl24a.wtz
+               Y.AXIS=I(Gate)          X.AXIS=V(Gate)
+               COLOR=2
+               DEVICE=CP/POSTSCRIP     PLOT.OUT=~/simulate/ofet/Aprl24g.ps


TITLE           OFET with traps output
PLOT.1D         IN.FILE=~/simulate/ofet/aprl24b.wta
+               Y.AXIS=I(Drain)         X.AXIS=V(Drain)
+               COLOR=2
+               DEVICE=CP/POSTSCRIP     PLOT.OUT=~/simulate/ofet/Aprl24g.ps

PLOT.1D         IN.FILE=~/simulate/ofet/aprl24c.wta
+               Y.AXIS=I(Drain)         X.AXIS=V(Drain)
+               COLOR=2
+               UNCHANGE
+               DEVICE=CP/POSTSCRIP     PLOT.OUT=~/simulate/ofet/Aprl24g.ps

PLOT.1D         IN.FILE=~/simulate/ofet/aprl24d.wta
+               Y.AXIS=I(Drain)         X.AXIS=V(Drain)
+               COLOR=2
+               UNCHANGE
+               DEVICE=CP/POSTSCRIP     PLOT.OUT=~/simulate/ofet/Aprl24g.ps

PLOT.1D         IN.FILE=~/simulate/ofet/aprl24e.wta
+               Y.AXIS=I(Drain)         X.AXIS=V(Drain)
+               COLOR=2
+               UNCHANGE
+               DEVICE=CP/POSTSCRIP     PLOT.OUT=~/simulate/ofet/Aprl24g.ps

PLOT.1D         IN.FILE=~/simulate/ofet/aprl24f.wta
+               Y.AXIS=I(Drain)         X.AXIS=V(Drain)
+               COLOR=2
+               UNCHANGE
+               DEVICE=CP/POSTSCRIP     PLOT.OUT=~/simulate/ofet/Aprl24g.ps
```

B.3 Medici input code to simulate a 400nm thick OMESFET

```
TITLE               D MESFET
COMMENT                     April24


$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
$           P3HT film thickness 400 nm
$           Al  as the gate
$            Au  as the source and drain
$           mobility of 0.1 cm2/Vs
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
$           Here we go for L=4micron and W=1micron
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

ASSIGN              NAME=width          N.VALUE=16.0
ASSIGN              NAME=topgtk         N.VALUE=0.02
ASSIGN              NAME=poltck         N.VALUE=0.4
ASSIGN              NAME=autck          N.VALUE=0.020
ASSIGN              NAME=altck          N.VALUE=0.020
ASSIGN              NAME=oxtck          N.VALUE=0.1
ASSIGN              NAME=devtck         N.VALUE=@topgtk+@poltck+@autck
ASSIGN              NAME=auwid          N.VALUE=4.0
ASSIGN              NAME=chl            N.VALUE=4.0
ASSIGN              NAME=alwid          N.VALUE=16.0
ASSIGN              NAME=bandg          N.VALUE=1.7

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
COMMENT                     Creat the Mesh
MESH                        SMOOTH=1
X.MESH              WIDTH=@width        H1=@width/100
Y.MESH              Y.MAX=@topgtk       H1=@topgtk/4
Y.MESH              Y.MIN=@topgtk       Y.MAX=@poltck+@topgtk               H1=@poltck/50
Y.MESH              Y.MIN=@poltck+@topgtk       Y.MAX=@autck+@poltck+@topgtk
+                   H1=@autck/10
$Y.MESH             Y.MIN=@poltck+@autck        Y.MAX=@devtck-@altck        H1=@oxtck/4
$Y.MESH             Y.MIN=@devtck-@altck        Y.MAX=@devtck               H1=@altck/4

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
COMMENT                     Specify the device material and regions

REGION              NAME=Semi           SEMICOND
REGION              NAME=DrainC         SEMICOND
+                   X.MIN=(@width-@chl)/2-@auwid
+                   X.MAX=(@width-@chl)/2
+                   Y.MIN=@poltck+@topgtk
+                   Y.MAX=@poltck+@autck+@topgtk
REGION              NAME=SourC          SEMICOND
+                   X.MIN=(@width+@chl)/2
+                   X.MAX=(@width+@chl)/2+@auwid
+                   Y.MIN=@poltck+@topgtk
+                   Y.MAX=@poltck+@autck+@topgtk
REGION              NAME=TGateC         SEMICOND
+                   Y.MAX=@topgtk


ELECTR              NAME=Drain          REGION=DrainC
ELECTR              NAME=Source         REGION=SourC
ELECTR              NAME=TGate          REGION=TGateC

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
COMMENT                     Impurity and contacts
PROFILE             UNIFORM             CONC=1E16           P.TYPE
MATERIAL            SEMICOND            PERMITTI=3.0        EG.MODEL=0
+                   EG300=@bandg        AFFINITY=3.3

CONTACT                     NAME=Drain          WORKFUNCTION=5.1
CONTACT                     NAME=Source         WORKFUNCTION=5.1
CONTACT                     NAME=TGate          ALUMINUM
```

```
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

COMMENT                 Symbolic
SYMBOLIC        NEWTON CARRIERS=1       HOLES
MOBILITY        MUP0=0.1
MODELS          SRH     FERMIDIR



ASSIGN          NAME=EV         N.VAL=-@bandg/2
ASSIGN          NAME=EC         N.VAL=@bandg/2

TRAP            E1=-0.85  N.TOT="-1E21"               COND="@FNENER=1"
TRAP            E2=-0.82  N.TOT="-4.15128E+20"       COND="@FNENER=2"
TRAP            E3=-0.79  N.TOT="-1.72331E+20"       COND="@FNENER=3"
TRAP            E4=-0.76  N.TOT="-7.15394E+19"       COND="@FNENER=4"
TRAP            E5=-0.73  N.TOT="-2.9698E+19"        COND="@FNENER=5"
TRAP            E6=-0.70  N.TOT="-1.23285E+19"       COND="@FNENER=6"
TRAP            E7=-0.67  N.TOT="-5.11789E+18"       COND="@FNENER=7"
TRAP            E8=-0.64  N.TOT="-2.12458E+18"       COND="@FNENER=8"
TRAP            E9=-0.61  N.TOT="-8.81971E+17"       COND="@FNENER=9"
TRAP            E10=-0.58 N.TOT="-3.66131E+17"       COND="@FNENER=10"
TRAP            E11=-0.55 N.TOT="-1.51991E+17"       COND="@FNENER=11"
TRAP            E12=-0.52 N.TOT="-6.30957E+16"       COND="@FNENER=12"
TRAP            E13=-0.49 N.TOT="-2.61928E+16"       COND="@FNENER=13"
TRAP            E14=-0.46 N.TOT="-1.08734E+16"       COND="@FNENER=14"
TRAP            E15=-0.43 N.TOT="-4.51383E+15"       COND="@FNENER=15"
TRAP            E16=-0.40 N.TOT="-1.87382E+15"       COND="@FNENER=16"
TRAP            E17=-0.37 N.TOT="-7.77874E+14"       COND="@FNENER=17"
TRAP            E18=-0.34 N.TOT="-3.22917E+14"       COND="@FNENER=18"
TRAP            E19=-0.31 N.TOT="-1.34052E+14"       COND="@FNENER=19"


COMMENT                 Symbolic
SYMBOLIC        GUMM    CARRIERS=0
SOLVE           V(Drain)=0      V(TGate)=0      V(Source)=0


$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

COMMENT                 Symbolic
SYMBOLIC        NEWTON CARRIERS=1       HOLES
MOBILITY        MUP0=0.1
MODELS          SRH     FERMIDIR
SOLVE           V(Drain)=0      V(TGate)=0      V(Source)=0

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

COMMENT                 IV Curve
LOG             OUT.FILE=~/simulate/MESFET/Aprl24a.wtz
SOLVE           V(Drain)=-0.5   V(TGate)=0      V(Source)=0
+               ELEC=TGate      VSTEP=0.1               NSTEP=70
LOG             CLOSE

COMMENT                 IV Curve
LOG             OUT.FILE=~/simulate/MESFET/Aprl24b.wta
SOLVE           V(Drain)=0      V(TGate)=0      V(Source)=0
+               ELEC=Drain      VSTEP=-0.1              NSTEP=100
LOG             CLOSE

COMMENT                 IV Curve
LOG             OUT.FILE=~/simulate/MESFET/Aprl24c.wta
SOLVE           V(Drain)=0      V(TGate)=1      V(Source)=0
+               ELEC=Drain      VSTEP=-0.1              NSTEP=100
LOG             CLOSE


COMMENT                 IV Curve
LOG             OUT.FILE=~/simulate/MESFET/Aprl24d.wta
SOLVE           V(Drain)=0      V(TGate)=2      V(Source)=0
+               ELEC=Drain      VSTEP=-0.1              NSTEP=100
LOG             CLOSE
```

```
COMMENT                 IV Curve
LOG             OUT.FILE=~/simulate/MESFET/Aprl24e.wta
SOLVE           V(Drain)=0      V(TGate)=3      V(Source)=0
+               ELEC=Drain      VSTEP=-0.1              NSTEP=100
LOG             CLOSE

COMMENT                 IV Curve
LOG             OUT.FILE=~/simulate/MESFET/Aprl24f.wta
SOLVE           V(Drain)=0      V(TGate)=4      V(Source)=0
+               ELEC=Drain      VSTEP=-0.1              NSTEP=100
LOG             CLOSE


COMMENT                 IV Curve
LOG             OUT.FILE=~/simulate/MESFET/Aprl24g.wta
SOLVE           V(Drain)=0      V(TGate)=5      V(Source)=0
+               ELEC=Drain      VSTEP=-0.1              NSTEP=100
LOG             CLOSE

TITLE           MESFET with traps transfer @ VDS=-0.5
PLOT.1D         IN.FILE=~/simulate/MESFET/Aprl24a.wtz
+               Y.LOG   Y.AXIS=I(Drain)         X.AXIS=V(TGate)
+               COLOR=2
+               DEVICE=CP/POSTSCRIP     PLOT.OUT=~/simulate/MESFET/Aprl24i.ps

TITLE           MESFET with traps transfer @ VDS=-0.5
PLOT.1D         IN.FILE=~/simulate/MESFET/Aprl24a.wtz
+               Y.AXIS=I(TGate)         X.AXIS=V(TGate)
+               COLOR=2
+               DEVICE=CP/POSTSCRIP     PLOT.OUT=~/simulate/MESFET/Aprl24i.ps


TITLE           MESFET with traps output
PLOT.1D         IN.FILE=~/simulate/MESFET/Aprl24b.wta
+               Y.AXIS=I(Drain)         X.AXIS=V(Drain)
+               COLOR=2
+               DEVICE=CP/POSTSCRIP     PLOT.OUT=~/simulate/MESFET/Aprl24i.ps

PLOT.1D         IN.FILE=~/simulate/MESFET/Aprl24c.wta
+               Y.AXIS=I(Drain)         X.AXIS=V(Drain)
+               COLOR=2
+               UNCHANGE
+               DEVICE=CP/POSTSCRIP     PLOT.OUT=~/simulate/MESFET/Aprl24i.ps

PLOT.1D         IN.FILE=~/simulate/MESFET/Aprl24d.wta
+               Y.AXIS=I(Drain)         X.AXIS=V(Drain)
+               COLOR=2
+               UNCHANGE
+               DEVICE=CP/POSTSCRIP     PLOT.OUT=~/simulate/MESFET/Aprl24i.ps

PLOT.1D         IN.FILE=~/simulate/MESFET/Aprl24e.wta
+               Y.AXIS=I(Drain)         X.AXIS=V(Drain)
+               COLOR=2
+               UNCHANGE
+               DEVICE=CP/POSTSCRIP     PLOT.OUT=~/simulate/MESFET/Aprl24i.ps

PLOT.1D         IN.FILE=~/simulate/MESFET/Aprl24f.wta
+               Y.AXIS=I(Drain)         X.AXIS=V(Drain)
+               COLOR=2
+               UNCHANGE
+               DEVICE=CP/POSTSCRIP     PLOT.OUT=~/simulate/MESFET/Aprl24i.ps

PLOT.1D         IN.FILE=~/simulate/MESFET/Aprl24g.wta
+               Y.AXIS=I(Drain)         X.AXIS=V(Drain)
+               COLOR=2
+               UNCHANGE
+               DEVICE=CP/POSTSCRIP     PLOT.OUT=~/simulate/MESFET/Aprl24i.ps
```

B.4 Medici input code to simulate OFETs with various thicknesses

```
TITLE               polthick 20nm to 200nm/5e16  L=4u bottom
COMMENT                     October30, 2006

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
$           Al  as the gate
$           mobility of 0.1 cm2/Vs
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
$           Here we go for L=4micron and W=1micron
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

ASSIGN              NAME=width          N.VALUE=12.0
ASSIGN              NAME=poltck         N.VALUE=0.02
$                           N.VALUE=0.04
$                           N.VALUE=0.06
$                           N.VALUE=0.08
$                           N.VALUE=0.10
$                           N.VALUE=0.12
$                           N.VALUE=0.14
$                           N.VALUE=0.16
$                           N.VALUE=0.18
$                           N.VALUE=0.20

ASSIGN              NAME=autck          N.VALUE=0.020
ASSIGN              NAME=altck          N.VALUE=0.020
ASSIGN              NAME=oxtck          N.VALUE=0.2
ASSIGN              NAME=devtck         N.VALUE=@altck+@poltck+@oxtck
ASSIGN              NAME=auwid          N.VALUE=4.0
ASSIGN              NAME=chl            N.VALUE=4.0
ASSIGN              NAME=alwid          N.VALUE=12.0
ASSIGN              NAME=bandg          N.VALUE=1.7

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
COMMENT                     Creat the Mesh
MESH                SMOOTH=1
X.MESH              WIDTH=@width        H1=@width/75
Y.MESH              Y.MAX=@poltck       H1=@poltck/20
Y.MESH              Y.MIN=@poltck       Y.MAX=@devtck-@altck        H1=@oxtck/4
Y.MESH              Y.MIN=@devtck-@altck        Y.MAX=@devtck               H1=@altck/4

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
COMMENT                     Specify the device material and regions

REGION              NAME=Semi           SEMICOND
REGION              NAME=DrainC         SEMICOND
+                   X.MIN=(@width-@chl)/2-@auwid
+                   X.MAX=(@width-@chl)/2
+                   Y.MIN=@poltck-@autck
+                   Y.MAX=@poltck
REGION              NAME=SourC          SEMICOND
+                   X.MIN=(@width+@chl)/2
+                   X.MAX=(@width+@chl)/2+@auwid
+                   Y.MIN=@poltck-@autck
+                   Y.MAX=@poltck
REGION              NAME=Oxdlay         OXIDE
+                   Y.MIN=@poltck
+                   Y.MAX=@poltck+@oxtck
REGION              NAME=GateC          SEMICOND
+                   Y.MIN=@devtck-@altck
ELECTR              NAME=Drain          REGION=DrainC
ELECTR              NAME=Source         REGION=SourC
ELECTR              NAME=Gate           REGION=GateC

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

COMMENT                     Impurity and contacts
```

```
PROFILE         UNIFORM         CONC=5E16       P.TYPE
MATERIAL        SEMICOND        PERMITTI=3.0    EG.MODEL=0
+               EG300=@bandg    AFFINITY=3.3
CONTACT                 NAME=Drain      WORKFUNCTION=5.1
CONTACT                 NAME=Source     WORKFUNCTION=5.1
CONTACT                 NAME=Gate       ALUMINUM

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

COMMENT                 Symbolic
SYMBOLIC        NEWTON CARRIERS=1       HOLES
MOBILITY        MUP0=0.1
MODELS          SRH     FERMIDIR


$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
$
COMMENT         Simulation with traps
$
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

ASSIGN          NAME=EV         N.VAL=-@bandg/2
ASSIGN          NAME=EC         N.VAL=@bandg/2

TRAP            E1=-0.85  N.TOT="-1E21"             COND="@FNENER=1"
TRAP            E2=-0.82  N.TOT="-4.15128E+20"      COND="@FNENER=2"
TRAP            E3=-0.79  N.TOT="-1.72331E+20"      COND="@FNENER=3"
TRAP            E4=-0.76  N.TOT="-7.15394E+19"      COND="@FNENER=4"
TRAP            E5=-0.73  N.TOT="-2.9698E+19"       COND="@FNENER=5"
TRAP            E6=-0.70  N.TOT="-1.23285E+19"      COND="@FNENER=6"
TRAP            E7=-0.67  N.TOT="-5.11789E+18"      COND="@FNENER=7"
TRAP            E8=-0.64  N.TOT="-2.12458E+18"      COND="@FNENER=8"
TRAP            E9=-0.61  N.TOT="-8.81971E+17"      COND="@FNENER=9"
TRAP            E10=-0.58 N.TOT="-3.66131E+17"      COND="@FNENER=10"
TRAP            E11=-0.55 N.TOT="-1.51991E+17"      COND="@FNENER=11"
TRAP            E12=-0.52 N.TOT="-6.30957E+16"      COND="@FNENER=12"
TRAP            E13=-0.49 N.TOT="-2.61928E+16"      COND="@FNENER=13"
TRAP            E14=-0.46 N.TOT="-1.08734E+16"      COND="@FNENER=14"
TRAP            E15=-0.43 N.TOT="-4.51383E+15"      COND="@FNENER=15"
TRAP            E16=-0.40 N.TOT="-1.87382E+15"      COND="@FNENER=16"
TRAP            E17=-0.37 N.TOT="-7.77874E+14"      COND="@FNENER=17"
TRAP            E18=-0.34 N.TOT="-3.22917E+14"      COND="@FNENER=18"
TRAP            E19=-0.31 N.TOT="-1.34052E+14"      COND="@FNENER=19"

COMMENT                 Symbolic
SYMBOLIC        GUMM    CARRIERS=0

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

COMMENT                 Symbolic
SYMBOLIC        NEWTON CARRIERS=1       HOLES
MOBILITY        MUP0=0.1
MODELS          SRH     FERMIDIR
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$


COMMENT                 IV Curve
LOG             OUT.FILE=~/simulate/SolidS/20ofe16.wtz
SOLVE           V(Drain)=-0.5   V(Gate)=0 V(Source)=0
+               ELEC=Gate       VSTEP=-0.25     NSTEP=160
LOG             CLOSE

COMMENT                 IV Curve
LOG             OUT.FILE=~/simulate/SolidS/20ofe16.wte
SOLVE           V(Drain)=0      V(Gate)=-40     V(Source)=0
+               ELEC=Drain      VSTEP=-0.25     NSTEP=240
LOG             CLOSE

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
```

```
PLOT.1D         IN.FILE=~/simulate/SolidS/20ofe16.wte
+               Y.AXIS=I(Drain)     X.AXIS=V(Drain)
+               COLOR=1             SYM=1
+               DEVICE=CP/POSTSCRIP     PLOT.OUT=~/simulate/SolidS/20ofe16o.ps

PLOT.1D         IN.FILE=~/simulate/SolidS/20ofe16.wtz
+               Y.LOG   Y.AXIS=I(Drain)     X.AXIS=V(Gate)
+               COLOR=1             SYM=1
+               DEVICE=CP/POSTSCRIP     PLOT.OUT=~/simulate/SolidS/20ofe16.ps
```

B.5 Medici input code to simulate a dual gate organic transistors

```
TITLE               MESOFET 200nm L=4u
COMMENT                     October 30, 2006


$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
$           P3HT film with 200nm thickness
$           Al  as the gate
$           100nm SiO2 Au  as the source and drain
$           mobility of 0.1 cm2/Vs
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
$           Here we go for L=4micron and W=1micron
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

ASSIGN              NAME=width      N.VALUE=12.0
ASSIGN              NAME=topgtk     N.VALUE=0.02
ASSIGN              NAME=poltck     N.VALUE=0.20
ASSIGN              NAME=autck      N.VALUE=0.020
ASSIGN              NAME=altck      N.VALUE=0.020
ASSIGN              NAME=oxtck      N.VALUE=0.2
ASSIGN              NAME=devtck     N.VALUE=@altck+@poltck+@oxtck+@topgtk
ASSIGN              NAME=auwid      N.VALUE=4.0
ASSIGN              NAME=chl        N.VALUE=4.0
ASSIGN              NAME=alwid      N.VALUE=12.0
ASSIGN              NAME=bandg      N.VALUE=1.7


$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
COMMENT                     Creat the Mesh
MESH                SMOOTH=1
X.MESH              WIDTH=@width    H1=@width/75
Y.MESH              Y.MAX=@topgtk   H1=@topgtk/4
Y.MESH              Y.MIN=@topgtk   Y.MAX=@topgtk+@poltck-@autck       H1=(@poltck-@autck)/60
Y.MESH              Y.MIN=@topgtk+@poltck-@autck Y.MAX=@topgtk+@poltck  H1=@autck/20
Y.MESH              Y.MIN=@poltck+@topgtk       Y.MAX=@devtck-@altck
+                   H1=@oxtck/4
Y.MESH              Y.MIN=@devtck-@altck        Y.MAX=@devtck           H1=@altck/4

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
COMMENT                     Specify the device material and regions
REGION              NAME=Semi       SEMICOND
REGION              NAME=TGateC     SEMICOND
+                   Y.MAX=@topgtk
REGION              NAME=DrainC     SEMICOND
+                   X.MIN=(@width-@chl)/2-@auwid
+                   X.MAX=(@width-@chl)/2
+                   Y.MIN=@poltck+@topgtk-@autck
+                   Y.MAX=@poltck+@topgtk
REGION              NAME=SourC      SEMICOND
+                   X.MIN=(@width+@chl)/2
+                   X.MAX=(@width+@chl)/2+@auwid
+                   Y.MIN=@poltck+@topgtk-@autck
+                   Y.MAX=@poltck+@topgtk
REGION              NAME=Oxdlay     OXIDE
+                   Y.MIN=@poltck+@topgtk
+                   Y.MAX=@poltck+@oxtck+@topgtk
REGION              NAME=GateC      SEMICOND
+                   Y.MIN=@devtck-@altck

ELECTR              NAME=Drain      REGION=DrainC
ELECTR              NAME=Source     REGION=SourC
ELECTR              NAME=Gate       REGION=GateC
ELECTR              NAME=TGate      REGION=TGateC

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COMMENT                     Impurity and contacts
```

```
PROFILE         UNIFORM         CONC=5E16       P.TYPE
MATERIAL        SEMICOND        PERMITTI=3.0    EG.MODEL=0
+               EG300=@bandg    AFFINITY=3.3

CONTACT                 NAME=Drain      WORKFUNCTION=5.1
CONTACT                 NAME=Source     WORKFUNCTION=5.1
CONTACT                 NAME=Gate       ALUMINUM
CONTACT                 NAME=TGate      ALUMINUM


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COMMENT                 Symbolic
SYMBOLIC        NEWTON CARRIERS=1       HOLES
MOBILITY        MUP0=0.1
MODELS          SRH     FERMIDIR

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ASSIGN          NAME=EV         N.VAL=-@bandg/2
ASSIGN          NAME=EC         N.VAL=@bandg/2

TRAP            E1=-0.85  N.TOT="-1E21"             COND="@FNENER=1"
TRAP            E2=-0.82  N.TOT="-4.15128E+20"      COND="@FNENER=2"
TRAP            E3=-0.79  N.TOT="-1.72331E+20"      COND="@FNENER=3"
TRAP            E4=-0.76  N.TOT="-7.15394E+19"      COND="@FNENER=4"
TRAP            E5=-0.73  N.TOT="-2.9698E+19"       COND="@FNENER=5"
TRAP            E6=-0.70  N.TOT="-1.23285E+19"      COND="@FNENER=6"
TRAP            E7=-0.67  N.TOT="-5.11789E+18"      COND="@FNENER=7"
TRAP            E8=-0.64  N.TOT="-2.12458E+18"      COND="@FNENER=8"
TRAP            E9=-0.61  N.TOT="-8.81971E+17"      COND="@FNENER=9"
TRAP            E10=-0.58 N.TOT="-3.66131E+17"      COND="@FNENER=10"
TRAP            E11=-0.55 N.TOT="-1.51991E+17"      COND="@FNENER=11"
TRAP            E12=-0.52 N.TOT="-6.30957E+16"      COND="@FNENER=12"
TRAP            E13=-0.49 N.TOT="-2.61928E+16"      COND="@FNENER=13"
TRAP            E14=-0.46 N.TOT="-1.08734E+16"      COND="@FNENER=14"
TRAP            E15=-0.43 N.TOT="-4.51383E+15"      COND="@FNENER=15"
TRAP            E16=-0.40 N.TOT="-1.87382E+15"      COND="@FNENER=16"
TRAP            E17=-0.37 N.TOT="-7.77874E+14"      COND="@FNENER=17"
TRAP            E18=-0.34 N.TOT="-3.22917E+14"      COND="@FNENER=18"
TRAP            E19=-0.31 N.TOT="-1.34052E+14"      COND="@FNENER=19"

COMMENT                 Symbolic
SYMBOLIC        GUMM    CARRIERS=0
SOLVE           V(Drain)=0      V(Gate)=0 V(TGate)=0      V(Source)=0

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COMMENT                 Symbolic
SYMBOLIC        NEWTON CARRIERS=1       HOLES
MOBILITY        MUP0=0.1
MODELS          SRH     FERMIDIR
SOLVE           V(Drain)=0      V(Gate)=0 V(TGate)=0      V(Source)=0

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COMMENT                 MESOFET L=4u Vtgate=0 IV Curve
LOG             OUT.FILE=~/simulate/SolidS/200mst.wtx
SOLVE           V(Drain)=-0.5   V(Gate)=0 V(TGate)=0      V(Source)=0
+               ELEC=TGate      VSTEP=0.1       NSTEP=60
LOG             CLOSE



COMMENT                 MESOFET L=4u Vtgate=0 IV Curve
LOG             OUT.FILE=~/simulate/SolidS/200msti.wta
SOLVE           V(Drain)=-0.5   V(Gate)=0 V(TGate)=0      V(Source)=0
+               ELEC=Gate       VSTEP=-0.25     NSTEP=160
LOG             CLOSE

COMMENT                 MESOFET L=4u Vtgate=0 IV Curve
SOLVE           V(Drain)=-0.5   V(Gate)=0 V(TGate)=1      V(Source)=0
+               ELEC=Gate       VSTEP=-0.25     NSTEP=160
```

```
LOG             CLOSE

COMMENT                 MESOFET L=4u Vtgate=0 IV Curve
LOG             OUT.FILE=~/simulate/SolidS/200msti.wtc
SOLVE           V(Drain)=-0.5       V(Gate)=0 V(TGate)=2        V(Source)=0
+               ELEC=Gate           VSTEP=-0.25         NSTEP=160
LOG             CLOSE

COMMENT                 MESOFET L=4u Vtgate=0 IV Curve
LOG             OUT.FILE=~/simulate/SolidS/200msti.wtd
SOLVE           V(Drain)=-0.5       V(Gate)=0 V(TGate)=3        V(Source)=0
+               ELEC=Gate           VSTEP=-0.25         NSTEP=160
LOG             CLOSE

COMMENT                 MESOFET L=4u Vtgate=0 IV Curve
LOG             OUT.FILE=~/simulate/SolidS/200msti.wte
SOLVE           V(Drain)=-0.5       V(Gate)=0 V(TGate)=4        V(Source)=0
+               ELEC=Gate           VSTEP=-0.25         NSTEP=160
LOG             CLOSE

COMMENT                 MESOFET L=4u Vtgate=5 IV Curve
LOG             OUT.FILE=~/simulate/SolidS/200msti.wtf
SOLVE           V(Drain)=-0.5       V(Gate)=0 V(TGate)=5        V(Source)=0
+               ELEC=Gate           VSTEP=-0.25         NSTEP=160
LOG             CLOSE

COMMENT                 MESOFET L=4u Vtgate=6 IV Curve
LOG             OUT.FILE=~/simulate/SolidS/200msti.wtg
SOLVE           V(Drain)=-0.5       V(Gate)=0 V(TGate)=6        V(Source)=0
+               ELEC=Gate           VSTEP=-0.25         NSTEP=160
LOG             CLOSE


COMMENT                 MESOFET L=4u Vtgate=0 IV Curve
LOG             OUT.FILE=~/simulate/SolidS/200mst.wta
SOLVE           V(Drain)=0          V(Gate)=-40         V(TGate)=0          V(Source)=0
+               ELEC=Drain          VSTEP=-0.25         NSTEP=240
LOG             CLOSE


COMMENT                 MESOFET L=4u Vtgate=0 IV Curve
LOG             OUT.FILE=~/simulate/SolidS/200mst.wtb
SOLVE           V(Drain)=0          V(Gate)=-40         V(TGate)=1          V(Source)=0
+               ELEC=Drain          VSTEP=-0.25         NSTEP=240
LOG             CLOSE

COMMENT                 MESOFET L=4u Vtgate=0 IV Curve
LOG             OUT.FILE=~/simulate/SolidS/200mst.wtc
SOLVE           V(Drain)=0          V(Gate)=-40         V(TGate)=2          V(Source)=0
+               ELEC=Drain          VSTEP=-0.25         NSTEP=240
LOG             CLOSE

COMMENT                 MESOFET L=4u Vtgate=0 IV Curve
LOG             OUT.FILE=~/simulate/SolidS/200mst.wtd
SOLVE           V(Drain)=0          V(Gate)=-40         V(TGate)=3          V(Source)=0
+               ELEC=Drain          VSTEP=-0.25         NSTEP=240
LOG             CLOSE

COMMENT                 MESOFET L=4u Vtgate=0 IV Curve
LOG             OUT.FILE=~/simulate/SolidS/200mst.wte
SOLVE           V(Drain)=0          V(Gate)=-40         V(TGate)=4          V(Source)=0
+               ELEC=Drain          VSTEP=-0.25         NSTEP=240
LOG             CLOSE

COMMENT                 MESOFET L=4u Vtgate=0 IV Curve
LOG             OUT.FILE=~/simulate/SolidS/200mst.wtf
SOLVE           V(Drain)=0          V(Gate)=-40         V(TGate)=5          V(Source)=0
+               ELEC=Drain          VSTEP=-0.25         NSTEP=240
LOG             CLOSE

COMMENT                 MESOFET L=4u Vtgate=0 IV Curve
LOG             OUT.FILE=~/simulate/SolidS/200mst.wtg
SOLVE           V(Drain)=0          V(Gate)=-40         V(TGate)=6          V(Source)=0
```

```
+                ELEC=Drain          VSTEP=-0.25          NSTEP=240
LOG              CLOSE


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TITLE            MESOFET L=4u Vt=0 200nm
PLOT.1D          IN.FILE=~/simulate/SolidS/200mst.wta
+                Y.AXIS=I(Drain)     X.AXIS=V(Drain)
+                COLOR=1             SYM=1
+                DEVICE=CP/POSTSCRIP       PLOT.OUT=~/simulate/SolidS/200msto.ps

TITLE            MESOFET L=4u Vt=1 200nm
PLOT.1D          IN.FILE=~/simulate/SolidS/200mst.wtb
+                Y.AXIS=I(Drain)     X.AXIS=V(Drain)
+                COLOR=1             SYM=1
+                DEVICE=CP/POSTSCRIP       PLOT.OUT=~/simulate/SolidS/200msto.ps

TITLE            MESOFET L=4u Vt=2 200nm
PLOT.1D          IN.FILE=~/simulate/SolidS/200mst.wtc
+                Y.AXIS=I(Drain)     X.AXIS=V(Drain)
+                COLOR=1             SYM=1
+                DEVICE=CP/POSTSCRIP       PLOT.OUT=~/simulate/SolidS/200msto.ps

TITLE            MESOFET L=4u Vt=3 200nm
PLOT.1D          IN.FILE=~/simulate/SolidS/200mst.wtd
+                Y.AXIS=I(Drain)     X.AXIS=V(Drain)
+                COLOR=1             SYM=1
+                DEVICE=CP/POSTSCRIP       PLOT.OUT=~/simulate/SolidS/200msto.ps

TITLE            MESOFET L=4u Vt=4 200nm
PLOT.1D          IN.FILE=~/simulate/SolidS/200mst.wte
+                Y.AXIS=I(Drain)     X.AXIS=V(Drain)
+                COLOR=1             SYM=1
+                DEVICE=CP/POSTSCRIP       PLOT.OUT=~/simulate/SolidS/200msto.ps

TITLE            MESOFET L=4u Vt=5 200nm
PLOT.1D          IN.FILE=~/simulate/SolidS/200mst.wtf
+                Y.AXIS=I(Drain)     X.AXIS=V(Drain)
+                COLOR=1             SYM=1
+                DEVICE=CP/POSTSCRIP       PLOT.OUT=~/simulate/SolidS/200msto.ps

TITLE            MESOFET L=4u Vt=6 200nm
PLOT.1D          IN.FILE=~/simulate/SolidS/200mst.wtg
+                Y.AXIS=I(Drain)     X.AXIS=V(Drain)
+                COLOR=1             SYM=1
+                DEVICE=CP/POSTSCRIP       PLOT.OUT=~/simulate/SolidS/200msto.ps

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TITLE            MESOFET L=4u Vt=0 200nm
PLOT.1D          IN.FILE=~/simulate/SolidS/200msti.wta
+                Y.AXIS=I(Drain)     X.AXIS=V(Gate)
+                COLOR=1             SYM=1
+                DEVICE=CP/POSTSCRIP       PLOT.OUT=~/simulate/SolidS/200msti.ps

TITLE            MESOFET L=4u Vt=1 200nm
PLOT.1D          IN.FILE=~/simulate/SolidS/200msti.wtb
+                Y.AXIS=I(Drain)     X.AXIS=V(Gate)
+                COLOR=1             SYM=1
+                DEVICE=CP/POSTSCRIP       PLOT.OUT=~/simulate/SolidS/200msti.ps

TITLE            MESOFET L=4u Vt=2 200nm
PLOT.1D          IN.FILE=~/simulate/SolidS/200msti.wtc
+                Y.AXIS=I(Drain)     X.AXIS=V(Gate)
+                COLOR=1             SYM=1
+                DEVICE=CP/POSTSCRIP       PLOT.OUT=~/simulate/SolidS/200msti.ps
```

```
TITLE          MESOFET L=4u Vt=3 200nm
PLOT.1D        IN.FILE=~/simulate/SolidS/200msti.wtd
+              Y.AXIS=I(Drain)     X.AXIS=V(Gate)
+              COLOR=1             SYM=1
+              DEVICE=CP/POSTSCRIP       PLOT.OUT=~/simulate/SolidS/200msti.ps

TITLE          MESOFET L=4u Vt=4 200nm
PLOT.1D        IN.FILE=~/simulate/SolidS/200msti.wte
+              Y.AXIS=I(Drain)     X.AXIS=V(Gate)
+              COLOR=1             SYM=1
+              DEVICE=CP/POSTSCRIP       PLOT.OUT=~/simulate/SolidS/200msti.ps

TITLE          MESOFET L=4u Vt=5 200nm
PLOT.1D        IN.FILE=~/simulate/SolidS/200msti.wtf
+              Y.AXIS=I(Drain)     X.AXIS=V(Gate)
+              COLOR=1             SYM=1
+              DEVICE=CP/POSTSCRIP       PLOT.OUT=~/simulate/SolidS/200msti.ps
TITLE          MESOFET L=4u Vt=6 200nm
PLOT.1D        IN.FILE=~/simulate/SolidS/200msti.wtg
+              Y.AXIS=I(Drain)     X.AXIS=V(Gate)
+              COLOR=1             SYM=1
+              DEVICE=CP/POSTSCRIP       PLOT.OUT=~/simulate/SolidS/200msti.ps

TITLE          MESOFET L=4u Vt=0 200nm
PLOT.1D        IN.FILE=~/simulate/SolidS/200mst.wtx
+              Y.AXIS=I(Drain)     X.AXIS=V(TGate)
+              COLOR=1             SYM=1    Y.LOG
+              DEVICE=CP/POSTSCRIP       PLOT.OUT=~/simulate/SolidS/200mst.ps
```

Appendix C

C.1 Fabrication of micro-electrodes

In this appendix the details of the electrode patterning process are described both to inform the reader and to provide a guide for future students. The process is summarized in Figure C.1.

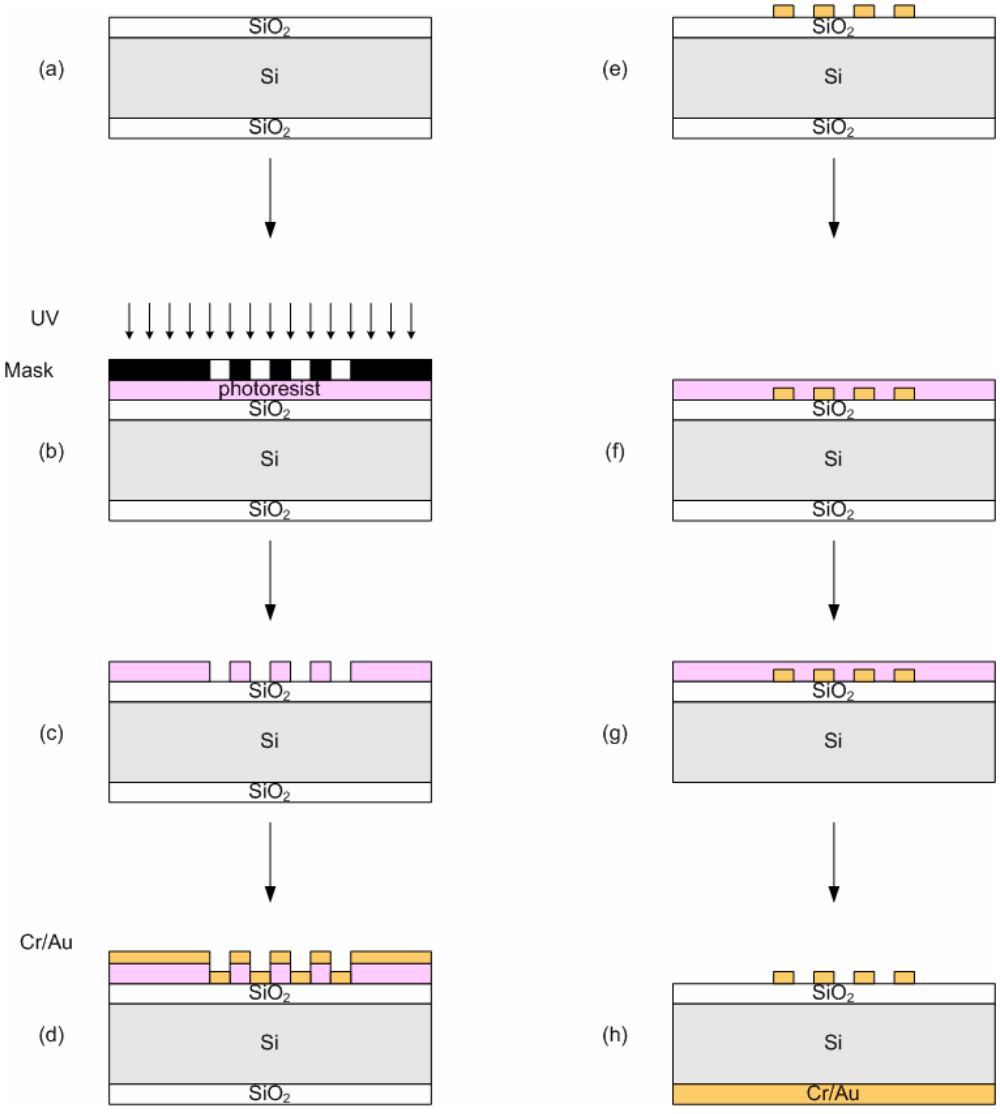

Figure C.1. Micro-electrode fabrication steps: (a) SiO_2/Si/SiO_2 wafer (b) photolithography (c) developing (d) metal deposition (e) lift-off (f) photoresist coating (g) SiO_2 back side etching (h) the backside electrode deposition.

C.1.1 **Wafer Cleaning**

The first step in the process of photolithography is to chemically clean the silicon wafer to make sure that the wafer is free of any grease, chemical residuals, and dust particle. The silicon wafer is first washed with acetone using a squeeze bottle. Since, acetone leaves some residue on the surface the wafer is washed with either isopropanol or methanol immediately after washing with acetone. Deionized water (DI water) is, then, jetted on the wafer surface to wash off all organic solvents. Following that the wafer is dried by blowing nitrogen gas over it. This step of cleaning is taken as a primary cleaning process which removes major dirt and dust from the wafer. To remove all chemicals the RCA-1 cleaning recipe is applied [126].

In the RCA-1 cleaning process, a solution including DI water, ammonium hydroxide (NH_4OH), and hydrogen peroxide (H_2O_2) is utilized. First, 5 parts of DI water are mixed with 1 part 27% NH_4OH and heated to 70 ˚C. Then, 1 part 30% H_2O_2 is added while the temperature is controlled at 70 ˚C. The silicon wafer is then put in the solution and kept there for 15 to 30 min. After that, the wafer is rinsed with a plenty of DI water and dried with nitrogen. In order to dispose of the solution it is diluted with large amounts of water and poured down the drain. Also, the beaker and all tools involved with the solution have to be washed with lots of water.

Note that hydrogen peroxide is explosive and should be kept away from solvents. The whole cleaning process is done in a fume hood. As an important step in the process, always H_2O_2 has to be added to NH_4OH and never the other way around [126].

C.1.2 **Photoresist coating**

Since the photolithography process is very sensitive to dust particles and the white light, the whole process is done in a class 1000 cleanroom illuminated with yellow light (yellow room).

The cleaned wafer is loaded on a spinner to coat it with photoresist. First, the wafer is coated with a layer of hexamethyldisilazane (HMDS) as an adhesion layer. 1 or 2 ml of HMDS is dropped on the surface of the wafer by means of a glass pipette so as to cover about 2/3 of the surface. The wafer is, then, spun for 40 sec at a speed of 4000 rpm. The result is an invisible layer of HMDS providing there is no defect on the deposited layer. The wafer is then left to dry for one minute. As with HMDS the photoresist is dropped on the surface and then the wafer is

spun at 5000 rpm for 40 sec. The photoresist is 2-ethoxyethyl acetate based positive type AZ4620 (Celanese corp [127]).

A very smooth and defect free layer of photoresist is necessary to achieve high resolution patterning. The photoresist film has to be visually inspected. If there is a defect in the film, the photoresist should be washed away with acetone and the cleaning process redone before proceeding to coating. There are a few reasons for an unacceptable photoresist film. If the spinner is not leveled or the spinner stage is not balanced, the photoresist spreads over the wafer surface non-uniformly. Starting with a dirty wafer or even a wafer that has not been cleaned enough is very likely to produce a low quality of photoresist layer. Using old photoresist or photoresist solution that has been exposed to white light are other factors that lead to poor quality. It is highly recommended that the wafer be handled with clean tweezers and never be touched. Also, a fresh disposable pipet has to be used for dropping the photoresist on the wafer. When there are small bubbles in the photoresist solution on top of the wafer before spinning, the photoresist film is found to have defects on the bubble spots after spinning. Therefore, all the bubbles have to be removed before the spinning. This can be achieved using the pipette.

C.1.3 **Soft Baking**

It is recommended to wait about a minute before removing the wafer from spinner in order to dry the film. The photoresist is then baked to make a film that is stable for light exposure. The process is called soft baking, in which the photoresist is treated by heating the wafer for 10 min at 90 ˚C. The oven used in the baking process should be pre-heated. Although, the yellow light in the cleanroom is supposed to be harmless for the photoresist, I achieved higher quality patterns when I turned off the lights until the developing step was complete.

C.1.4 **Mask alignment and exposure**

An optical mask is required to apply the desired pattern. The mask is designed by means of a CAD tool from Cadence company [128] for a 4” mask aligner machine. The mask consists of 8 sets of micro-electrode patterns which provides 8 sets of micro-electrodes in each batch. The mask used in the experiments presented in this thesis were fabricated at the University of Alberta in a negative pattern (the desired metalization pattern is the transparent region and the remainder of the mask is coated with chromium). In combination with the positive resist, this mask enables a lift off process to be employed.

A Canon PLA-501F mask aligner is used to apply the pattern on the photoresist layer. The photoresist coated wafer is loaded and following that the mask is put in the mask aligner. The contact mode is chosen which puts the mask on top of the sample without any gap between the two. Then UV light is shined for 11 s. The timing is very critical as under exposing or over exposing causes non developed or over developed patterns. Also, the user has to check the calibration of the light intensity regularly.

C.1.5 **Developing**

The non-exposed area of the photoresist is chemically more resistant, whereas the exposed area is washed away more readily by the developer. The developer solution used consists of 1 part AZ400K (from Clariant) [129] and 4 parts deionized water. The solution is prepared in a plastic bath and mixed well before putting the wafer in. In 2-3 minutes the pattern appears on the photoresist while the user is shaking the bath. The sample is then put in a water bath (deionized) for about 3 minutes to wash the developer from the sample. It is then dried using nitrogen.

For micron scale feature sizes it is recommended to check the pattern using an optical microscope to be sure that the pattern is well developed. If it is underdeveloped, it can be put back into the developer solution for one minute more, but if it is overdeveloped, the photoresist has to be removed from the surface and the process started over again.

The developer solution has to be diluted with a plenty of water before disposing of it down the drain.

C.1.6 **Metal deposition**

The wafer with the developed pattern is transferred to an e-beam evaporator to deposit the metal layer. I have patterned gold electrodes, but because of low adhesion between gold and silicon dioxide a layer of chromium is deposited first. Therefore, the gold and chromium sources are loaded in the evaporator as well as the sample. The machine is pumped down to about 10^{-6} torr before starting the deposition. A layer of chromium is then deposited with a thickness of 10 to 15 nm followed by 60 to 70 nm of gold. The rate of deposition is controlled to be around 1 Å/s.

C.1.7 **Lift off**

To remove the photoresist the sample is sonicated in acetone for about 10 minutes. The buried photoresist lifts off and the metallic micro-electrodes stay on the surface of the wafer. Then the sample is washed with acetone and methanol to remove the chemical residue, rinsed with deionized water and dried with nitrogen.

C.1.8 **Back electrode**

The electrodes are almost ready for use. However in order to build transistors a connection to the silicon (under the SiO_2 layer) is needed. To achieve this the silicon dioxide on the backside of the wafer is etched and a metal layer is deposited on the backside. During this process the front side of the wafer must be protected.

To protect the fabricated electrodes a layer of photoresist is deposited all over the electrode side of the wafer using the same method explained in section 3.2.1.2. Since the surface of the wafer is not flat anymore the photoresist layer might not be as smooth as it was the first time. Nevertheless, the smoothness is not crucial in this step as the layer is not used for any fine patterning process. The photoresist has to be baked in a process called hard backing before etching the SiO_2 layer in the backside of the wafer. In hard baking the sample is loaded in an oven with a temperature of 120 ˚C for 25 minutes.

In order to remove the backside silicon dioxide now the wafer is put in a solution containing HF acid. A buffered oxide etch solution, BOE, is used. The BOE solution includes dilute hydrofluoric acid (HF), but the concentration of HF is still much higher than what is required, so it is diluted by mixing 1 part BOE with 10 parts deionized water. Since, the solution dissolves glass all containers and laboratory tools involved with the process have to be made of plastic, including the tweezers. Also, the process has to be run under a fume hood. Wearing acid gloves, a face mask, and an acid apron are mandatory when a person is working with BOE. The etching rate of SiO_2 for the prepared solution is about 60 nm/min. To remove 350 nm thick SiO_2 layer the wafer is placed in the BOE solution for 6 minutes. Then it is transferred to a deionized water bath and kept there for about 6 minutes to wash away the HF. The effectivness of the removal of the oxide can be tested by observing the hydrophobicity of the surface. If a droplet of water spreads over the surface the surface is hydrophilic, whereas a non-spreading droplet indicates a hydrophobic surface. Silicon is a hydrophilic surface and silicon dioxide is a hydrophobic one.

Therefore, one can simply test whether SiO_2 is completely removed or not. If it has not removed the wafer can be put in the BOE solution for one more minute. After etching the backside SiO_2 layer the sample and all tools have to be washed with plenty of deionized water. Also, the solution has to be diluted with tap water, leaving it under running water for about 3 minutes before letting it flow down the drain.

The wafer is then dried with nitrogen and loaded into the evaporator to deposit a layer of Cr/Au directly on to the silicon surface, following the same procedure as described above. The hard baked photoresist on the front side now can be removed by sonicating the wafer in acetone. The wafer is then diced with a diamond saw to obtain 8 sets of individual micro-electrodes. Figure C.1 is an overview of the steps in the microfabrication process.