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Simulation of a dual gate organic transistor compatible with printing methods

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Abstract

In fabricating organic field-effect transistors (OFET) the deposition of a very thin and electrically continuous semiconductor layer using a low-cost process such as a printing method is a challenge. A simple model is proposed which relates performance to thickness, and shows that the thick layers typical of low-cost methods lead to poor device properties. The analytical model of thickness dependence is shown to match OFET simulation results for a range of thickness. These results indicate a change in the threshold voltage and drops in the output impedance and the current ratio with an increase in the semiconductor thickness.

As a solution a dual gate structure is suggested for organic transistors, in which the secondary gate controls the effective thickness of the organic layer through a Schottky contact with the semiconductor. Simulation results for a 200 nm thick dual gate OFET show a performance much better than is observed in a near optimal 20 nm thick OFET, by achievement of a current ratio of 10^6, versus 2500 in the OFET.

Keywords: Organic field-effect transistor (OFET); rr-P3HT; Schottky contact; Semiconductor thickness

1. Introduction

Methods including printing, casting, stamping, spin coating and vapor deposition have been used to fabricate organic field-effect transistors (OFETs) [1]. Most of the high-performance OFETs that have been demonstrated are made by vapor deposition methods from small organic molecules as the semiconductor [2]. Although the evaporation methods have been very useful to study the electrical characteristics of the organic semiconductors, the methods are too expensive to be used for low-cost electronic applications such as RFID tags [3]. Among different techniques, the printing methods are the most inexpensive patterning and deposition processes with the capability of roll-to-roll production for the organic electronics, but the device performance is relatively poor because the deposited film is too thick with a poor molecular order [4]. Most of the simple printing techniques such as inkjet printing have a thickness resolution around a few hundred of nanometers [5], whereas the optimum thickness for an OFET is about 30 nm [6]. Many research groups around the world are working on the development of printing techniques to meet the organic electronics requirements [7]. However, the price of advanced printing machines affects the cost of the product especially in low production quantities.

In this paper, the dependency of OFET characteristics on the semiconductor thickness is studied by simulation of the device. Then, the application of a Schottky contact as the secondary gate is shown to greatly enhance the performance of a thick film transistor.

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2. Modeling

An OFET (Fig. 1a) is basically an isolated-gate field effect transistor (IGFET) which works in the accumulation mode when the transistor is on. In this case, the applied gate voltage accumulates carriers at the insulator–semiconductor interface to increase the conductance between the drain and the source contacts. The depth of the accumulation layer is about 2–3 nm which is equal to a few monolayers of the organic semiconductor [8]. The remaining thickness in the semiconductor acts as a resistor between the drain and source. Excluding the effect of the resistor, similar to any IGFET, the output characteristic of the transistor shows two distinct regimes: linear and saturation. When $|V_{GS} - V_T| > |V_{DS}|$ the transistor is in the linear regime, where V_{GS} is the gate voltage versus the source, V_T is the threshold voltage and V_{DS} is the voltage between the drain and source. The transistor saturates when $|V_{GS} - V_T| < |V_{DS}|$. Ideally, in the off mode, the transistor has a zero conductance between the drain and source when $|V_{GS}| < |V_T|$.

Fig. 1 shows a schematic of a bottom contact OFET with an equivalent circuit for the device, in which the effect of the bulk resistance is represented by the parallel resistor (R_P). Assuming that the thickness of the semiconductor is much larger than the depth of the accumulation layer, R_P is expressed by

$$R_P = \frac{L}{\sigma_{blk} Z t_s} \tag{1}$$

where L is the distance between the drain and source, Z is the width of the drain/source electrodes and t_s is the thickness of the semiconductor in the channel and σ_{blk} is the bulk semiconductor conductivity.

The current in the transistor element (I_1) is a function of the gate voltage. In the linear regime, I_1 is [9]

$$I_{1-Lin} = \left(\frac{Z\mu_{field}C_i}{L}\right)[(V_{GS} - V_T)V_{DS}] \tag{2}$$

where C_i is the gate capacitance per unit of area and μ_{field} is the field effect mobility of the carrier in the channel. For the saturation regime, the current is a quadratic function of the gate voltage:

$$I_{1-sat} = \left(\frac{Z\mu_{field}C_i}{2L}\right)(V_{GS} - V_T)^2 \tag{3}$$

and in the off mode, ideally $I_{1-off} = 0$.

According to the model the drain terminal current for the device is the summation of the currents in the transistor and the resistor. Therefore, the current in the linear regime is

$$I_{D-lin} = I_{1-Lin} + I_2 = \left(\frac{Z\mu_{field}C_i}{L}\right)[(V_{GS} - V_T)V_{DS}] + \frac{V_{DS}}{R_P} \tag{4}$$

Replacing R_P from Eq. (1) into Eq. (4) and rearranging after gives

$$I_{D-lin} = \left(\frac{Z\mu_{field}C_i}{L}\right)[V_{GS} - V_{Tapp}]V_{DS} \tag{5}$$

where V_{Tapp} is the apparent threshold voltage described by

$$V_{Tapp} = \left(V_T - \frac{\sigma_{blk}t_s}{\mu_{field}C_i}\right) \tag{6}$$

As Eqs. (5) and (6) suggest, the effect of the parallel resistor appears only in the threshold voltage of the device in the linear mode. Therefore, the field effect mobility can be calculated from the slope of I_D–V_{GS} plot [7] in the linear regime regardless of the semiconductor thickness, but the apparent threshold voltage is a function of the thickness. Indeed, for a very thick semiconductor, especially when the bulk conductivity is relatively high, the sign of the apparent threshold voltage is different from V_T which means that the transistor can not be switched off even at $V_{GS} = 0$. The implication for device operation is that high on/off ratios can only be obtained when gate voltages can be made both negative and positive relative to the source, a significant disadvantage, particularly in a low-cost device.

Considering the effect of the parallel resistor, the saturation current is not independent of the V_{DS} anymore, and the slope of the I_D–V_{DS} curve is R_P^{-1}:

$$I_{D-sat} = \left(\frac{Z\mu_{field}C_i}{2L}\right)(V_{GS} - V_T)^2 + \frac{V_{DS}}{R_P} \tag{7}$$

Since R_P is proportional to the inverse of the semiconductor thickness, the slope of the current in I_D–V_{DS} increases with the thickness (t_s). Indeed, R_P is the output impedance (Z_{out}) of the device in the saturation regime which drops with the semiconductor thickness. Also, Eq. (7) indicates that derivation of the field effect mobility from $\sqrt{I_D}$–V_{GS} curve is not accurate in the saturation regime, except when R_P is very large.

Furthermore, the semiconductor thickness has a significant effect on the off mode of the device as the current is not zero when $|V_{GS}| < |V_T|$. Assuming that the transistor is off when $V_{GS} = 0$, the device behaves as a resistor between the drain and source terminals. The value of the resistance in the off mode R'_P is actually different from the

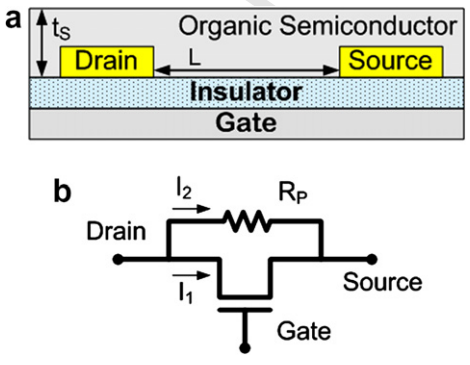

Fig. 1. (a) A schematic of a bottom contact OFET and (b) a simple model for the device consisted of an ideal IGFET and a parallel resistor.

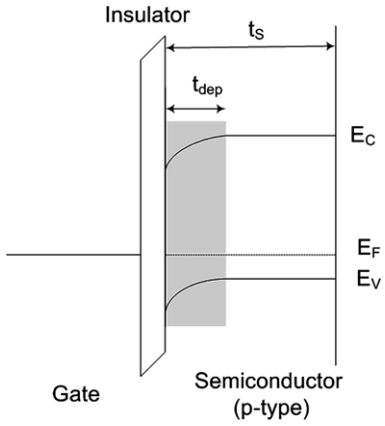

Fig. 2. The energy band diagram for a MIS device at the equilibrium ($V_{GS} = 0$).

bulk resistance (R_P) because of the depletion region produced from the band bending at the $V_{GS} = 0$. Fig. 2 depicts the band bending at zero gate voltage for a p-type metal–insulator–semiconductor (MIS) device. Because of the depletion region, the effective thickness of the semiconductor is reduced to t_s–t_{dep}. Therefore R'_P is expressed as:

$$R'_P = \frac{L}{\sigma_{blk} Z(t_s - t_{dep})} \tag{8}$$

And consequently the off current is

$$I_{D-off} = \frac{\sigma_{blk} Z(t_s - t_{dep})}{L} V_{DS} \tag{9}$$

To reduce the off current, one can apply large enough voltage to the gate in the depletion mode to extend the depletion region close to t_s. For a thick layer of the semiconductor the required gate voltage is so high that insulator breakdown will likely occur before the semiconductor can be fully depleted. In a very thin semiconductor layer, t_s might be even smaller than t_{dep} which in this case, the depletion region is restricted to the semiconductor thickness and the semiconductor is fully depleted at $V_{GS} = 0$.

Considering $V_{GS} = 0$ as the off state, the on/off current ratio is written in the linear mode by taking the ratio of Eqs. (5) and (9):

$$\frac{I_{on}}{I_{off}} = \left(\frac{\mu_{field} C_i}{\sigma_{blk}(t_s - t_{dep})}\right)[V_{GS} - V_{Tapp}] \tag{10}$$

The current ratio drops with increasing semiconductor thickness, and there is also an influence due to a shift in the apparent threshold. Eq. (10) also shows that the current ratio is independent of the channel length (L) and width (Z). Increasing the value of R_P by changing L and/or Z does not improve the current ratio.

In summary, the thickness of the semiconductor has negative effects on the apparent threshold voltage, output impedance, and the on/off current ratio. Hence, the performance of the device improves with a reduction in the semiconductor thickness. Theoretically, the peak performance is achieved when the semiconductor is just as thick as the depth of the accumulation layer, which is less than 3 nm. In practice, such a thin film is hardly continuous and shows a poor current ratio due to the contact resistances and leakage current in the off mode [6]. Consequently, the optimum thickness is measured to be around 30 nm [6]. Most of the inexpensive deposition methods such as printing or dip casting have resolution much lower than 30 nm. As a result the performance is very poor in the devices made with these simple methods relative to those made by evaporation techniques.

To reduce the effect of the thickness on device performance a secondary gate is suggested on top of the semiconductor. The top gate (TG), shown in Fig. 3, makes a Schottky contact with the semiconductor, which produces a depletion region in the semiconductor with a depth of t_{Sch}. Therefore, the effective semiconductor thickness in the linear and saturation regimes is t_s–t_{Sch}, and it is t_s–t_{Sch}–t_{dep} in the off mode. The depth of the depletion region in a crystalline semiconductor is given by [9]:

$$t_{Sch} = \sqrt{\frac{2\varepsilon_S}{qN_S}(V_A + V_b)} \tag{11}$$

where V_A is the applied voltage in the reverse bias across the Schottky junction, V_b is the built in voltage in the junction, ε_S is the permittivity of the semiconductor and q is the unit charge. N_S is the charge density in the depletion region, which is assumed to be uniform all along the depletion region. For crystalline semiconductors, N_S is usually equal to the dopant density, but in amorphous semiconductors, such as organics, the trapped charge in the localized states is considered as well. Nevertheless, t_{Sch} increases with applied voltage in the reverse bias which shrinks the effective

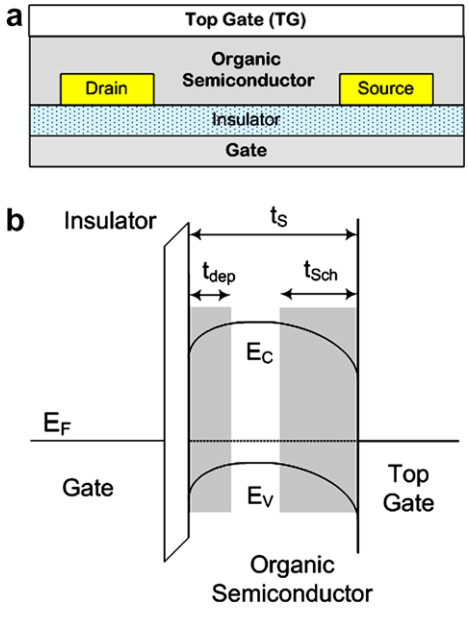

Fig. 3. (a) A schematic of a dual gate OFET and (b) the energy band diagram at the both gate interfaces (equilibrium condition – $V_{GS} = V_{TG} = 0$ V).

semiconductor thickness. The absence of the insulator between the top gate and the semiconductor is an advantage for extending t_{Sch} to a much larger distance than t_{dep} can reach for the same voltage applied to the gates.

At a certain voltage applied to the top gate such that $t_s = t_{Sch}$, the depletion region is extended through the semiconductor thickness and the effect of the parallel resistance is eliminated.

Simulations were done in order to verify the effectiveness of the top gate and the correctness of the simple model of the effects of thickness.

3. Simulation

A set of transistors are simulated with organic layer thicknesses ranging from 20 to 200 nm, with the thickest layer mimicking a device made by a low-cost printing method [5]. In addition the dual gate configuration is applied on the 200 nm thick film to show the enhancement in the performance of the device.

Medici version 4.0 (produced by Synopsys [10]) is used as the CAD tool for the device simulation. Medici models the two-dimensional distributions of potential and carrier concentrations in a device. The program solves Poisson's equation and the continuity equation in every node of a two-dimensional mesh determined by the user. The third dimension is always assumed to be 1 μm. Since in a FET transistor the currents are proportional to the width of the device, the simulation results are normalized for a 1 μm width. Medici 4.0 supports amorphous semiconductor simulation by including the effect of localized states as traps.

Regioregular-poly 3 hexylthiophene (rr-P3HT), which is a very stable p-type polymer semiconductor [1], is chosen as the semiconductor for the device simulation. Rr-P3HT has shown the highest field effect mobility among the soluble organic semiconductors [11], making it a good candidate for printing. The band gap of this semiconductor is 1.7 eV [12]. The electron affinity is calculated to be 3.15 eV from the ionization energy and the band gap of rr-P3HT [13]. Since rr-P3HT is a p-type material, the simulation is done on holes as carriers and the effect of electrons is ignored. Therefore, only the density of localized states close to the valence band is considered. The densities of localized states are applied as discrete trap levels which are intended to mimic the density of states measured by Tanase et al. [14]. In the trap model simulation, mobility of holes in the valence band is required, which is different from the bulk mobility resulting from hopping carriers between localized states. Although the mobility in the valence band is not available for rr-P3HT, the highest reported field effect mobility (0.1 $cm^2/V\,s$ [11]), is used in the simulation. A relative dielectric constant, $\varepsilon_s = 3$, is assumed [15], and the doping density is set at $5 \times 10^{16}\ cm^{-3}$ for rr-P3HT, assuming that the polymer is exposed to air for a long time [16]. For simplicity, gold with a work function of 5.1 eV, that makes ohmic contact with rr-P3HT [17], is chosen for the drain and source electrodes , and aluminum with work function of 4.3 eV is considered for the gate. Also, aluminum is used for the top gate as we know that it makes a Schottky contact with the semiconductor [17]. In the OFETs, SiO_2 is chosen as the insulating layer, with a thickness of 200 nm as most of the time such a thickness is required for a low leakage current. The channel length (L) is set to 4 μm and as mentioned the width $Z = 1$ μm. As the effect of the channel length and width is not concerned in our discussion they are chosen in a way to avoid the short channel effect [18] and gain the maximum resolution given the numerical limitations of the software.

4. Simulation results

To study the effect of the semiconductor thickness on the transistor characteristic in the linear regime, V_{DS} is held at −0.5 V and V_{GS} is scanned from 0 to −40 V. Fig. 4 shows the transverse characteristic (I_D–V_{GS}) of the device for 20, 100, and 200 nm OFETs in a semi-log plot. The current overlap in $-40\ V < V_{GS} < -20\ V$ suggests that gate voltage is sufficiently higher than the threshold voltage for the all thicknesses.

According to Eq. (5), V_{Tapp} is obtained by fitting a linear function to the I_D–V_{GS} curve when $|V_{GS}| > |V_T|$ and finding the voltage intercept. The apparent threshold voltages are obtained for 11 transistors with different thicknesses by the same method and their variations with the thickness is indicated in Fig. 5.

As Eq. (6) predicts, the apparent threshold voltage is linearly dependent on the semiconductor thickness and it is shifted to the lower magnitudes with the thickness. For the selected parameters in the simulation the change in

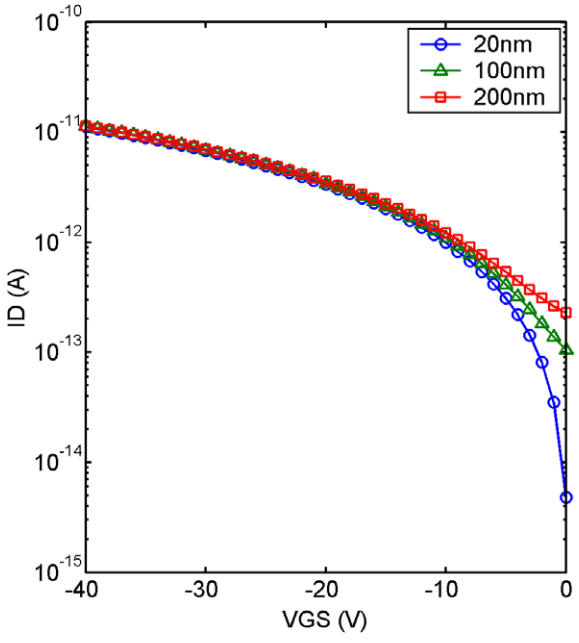

Fig. 4. The transverse characteristics of the simulated OFETs with the different semiconductor thicknesses ($V_{DS} = -0.5$ V).

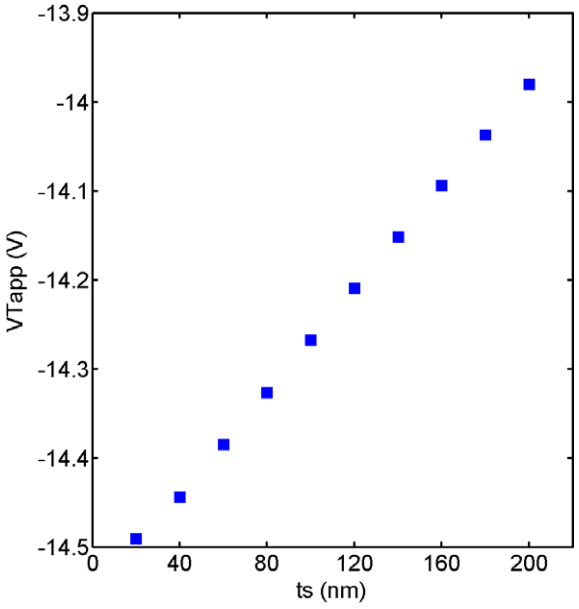

Fig. 5. The variation of V_{Tapp} in the OFETs with the semiconductor thickness ($V_{DS} = -0.5$ V).

the threshold voltage is about 0.5 V when the thickness is changed from 20 to 200 nm.

The saturation regime in the transistors is studied by application of −40 V to the gate electrode and scanning the drain voltage from 0 to −60 V. The output characteristic (I_D–V_{DS}) of transistors for three different thicknesses are plotted in Fig. 6. The differences in the slopes in the saturation regimes indicate the dependence of the output impedance on the thickness of the semiconductor as Eq. (7) suggests (the thickest layer has the lowest impedance).

The output impedances calculated from the output characteristics (I_D–V_{DS}) are shown versus the semiconductor thickness in Fig. 7. A drop of 300 G Ω (equal to 26%) is observed in the output impedance when the thickness is increased from 20 to 200 nm.

The current ratio and the off current are obtained from the simulation results shown in Fig. 4. The I_D values at $V_{GS} = -40$ V are considered as I_{on} whereas the currents at $V_{GS} = 0$ V are taken as I_{off}. Fig. 4 shows a rapid drop of the current below the threshold voltage for 20 nm thick OFET, but the rate is much lower for the thick film transistors. In Fig. 8 the off current and the on/off current ratio are shown versus the semiconductor thickness. An approximately two orders of magnitude rise in the off current is the effect of increasing the thickness from 20 to 200 nm. Extrapolating the off current in Fig. 8 to cross the thickness axis gives $t_{dep} = 16$ nm for $V_{GS} = 0$. Also, the current ratio decreased from 2300 to 20 for the same range of the semiconductor thickness. A very rapid increase of the current ratio from 40 to 20 nm is predicted by the simulations as the semiconductor thickness, t_S, approaches the depletion depth, t_{dep} (Eq. (10)).

The simulation results show that the 200 nm thick OFET has a poor performance relative to the 20 nm transistor, especially in current ratio. 200 nm is a reasonable thickness for most of the low-cost printing methods and is generally needed in order to obtain an electrically continuous film, making it currently impractical to achieve the excellent performance of thinner devices using inexpensive processing. We have chosen to simulate a 200 nm thick dual gate organic transistor to compare its electrical characteristics with those in the OFET. The top gate material

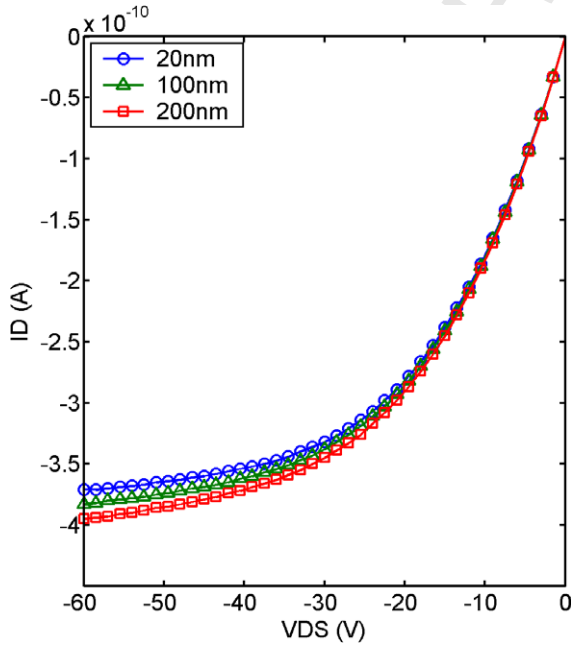

Fig. 6. The output characteristics of the OFETs with the different semiconductor thicknesses ($V_{GS} = -40$ V).

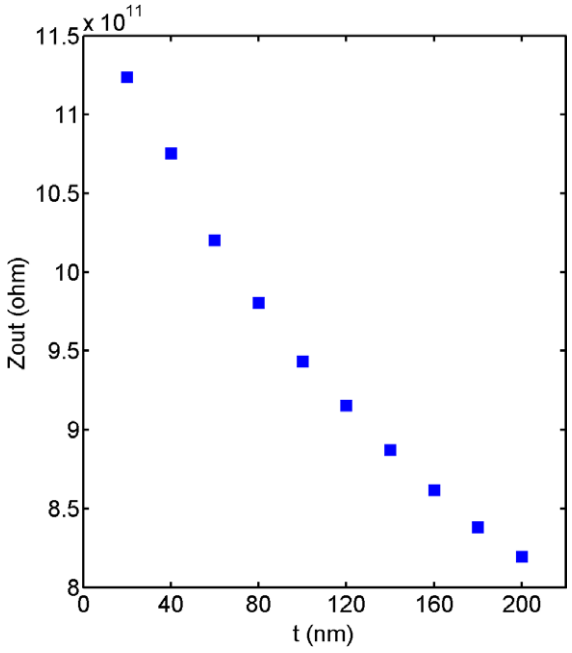

Fig. 7. The variation of the output impedance in the OFETs with the semiconductor thickness (-60 V $< V_{DS} < -40$ V and $V_{GS} = -40$ V).

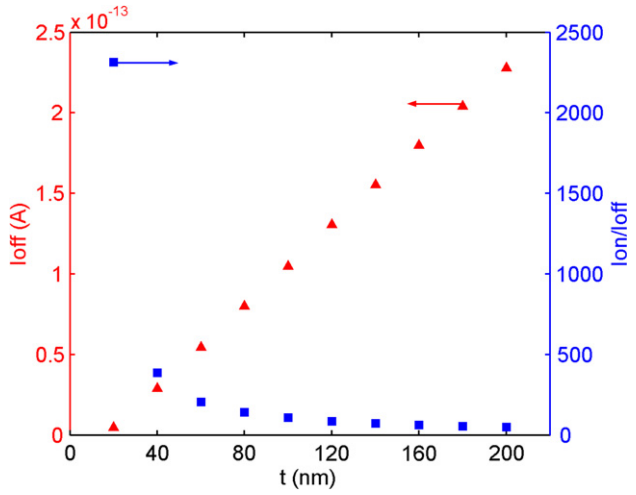

Fig. 8. The variation of the off current and the on/off current ratio in the OFETs with the semiconductor thickness ($V_{DS} = -0.5$ V).

is aluminum and makes Schottky contact with the organic semiconductor [17]. To avoid the current leakage through the top gate (TG), a positive potential has to be applied to TG, which drives the Schottky junction in the reverse bias.

To find out the depth of the depletion region from the top gate (t_{Sch}) at different voltages, the transistor is biased at $V_{GS} = 0$ V and $V_{DS} = -0.5$ V and then the V_{TG} is scanned from 0 to 6 V to measure the off current. Fig. 9, shows the variation of the off current versus the top gate voltage in a semilog plot.

A voltage about 5.4 V to the top gate is sufficient to deplete the entire semiconductor layer, which reduces the off current by more than four orders of magnitude. Above that voltage, the current saturates with the remaining current due to the finite but very small conductance in the depletion region.

To study the effect of the top gate voltage on the linear regime, the drain–source voltage is held at −0.5 V when the gate voltage is scanned from 0 to −40 V for discrete values of V_{TG} from 0 to 6 V. Fig. 10 shows the results of the simulation for three different values of top gate voltage. Similarities between Figs. 4 and 10 indicate that the top gate is controlling the effective thickness of the semiconductor.

The effect of V_{TG} on the apparent threshold voltage is shown in Fig. 11. Application of 6 V to the top gate has changed V_{Tapp} for more than 0.5 V. Comparing values in Figs. 5 and 11 indicates that when $V_{TG} = 5$ V the threshold voltage in a 200 nm thick dual gate OFET is same as that in the 20 nm OFET.

The output resistance of a dual gate OFET in the saturation mode is also controllable using V_{TG}. The output characteristic of the device (I_D–V_{DS}) is simulated for discrete values of V_{TG} from 0 to 6 V when $V_{GS} = -40$ V.

The results (Fig. 12) show a reduction of the current slope as the top gate voltage is increased. The calculated output resistances at different top gate voltages are plotted in Fig. 13, which indicates the change of the output impedance with top gate voltage. Comparing values in Figs. 7 and 13, the output impedance is 2.5 times larger in the dual gate transistor when $V_{TG} = 6$ V than that in the 20 nm thick OFET.

Also, the on/off current ratio is improved in the dual gate structure as the off current is reduced from 10^{-13} to 10^{-17} A (Fig. 9) when the top gate voltage is changed from 0 to 6 V. A ratio more than 10^6 is achieved for a 200 nm

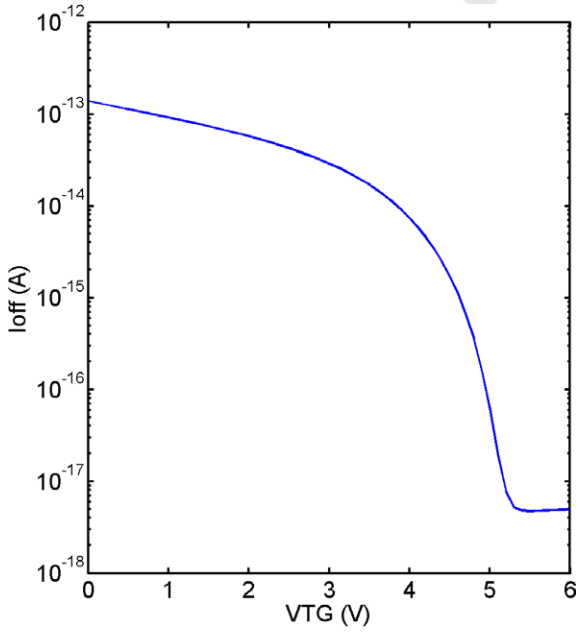

Fig. 9. The variation of the off current in the 200 nm thick dual gate OFET with the top gate voltage ($V_{DS} = -0.5$ V and $V_{GS} = 0$ V).

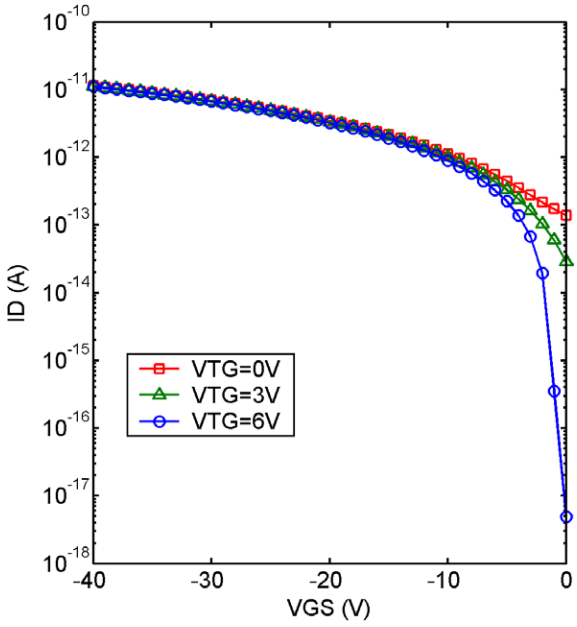

Fig. 10. The transverse characteristics of the simulated 200 nm dual gate OFET at different top gate biases ($V_{DS} = -0.5$ V).

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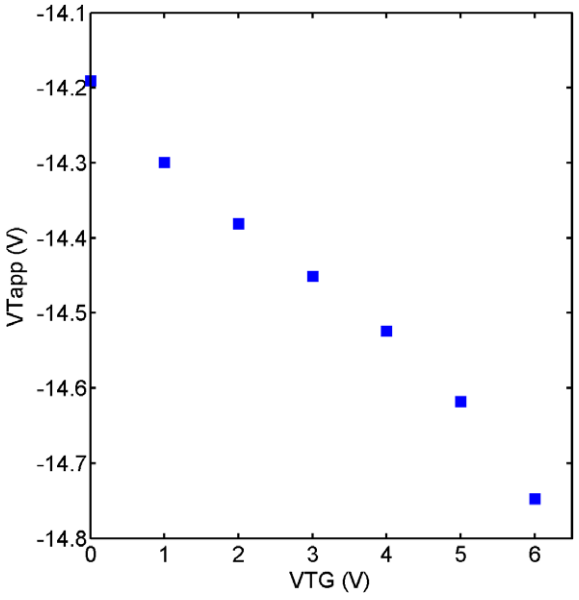

Fig. 11. The variation of the apparent threshold voltage in the 200 nm thick dual gate OFET with the top gate voltage ($V_{DS} = -0.5$ V and $V_{GS} = -40$ V).

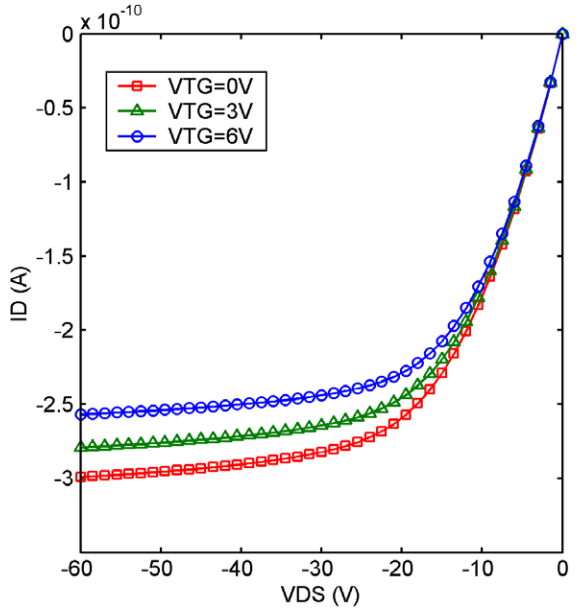

Fig. 12. The output characteristics of the simulated 200 nm dual gate OFET in different biases of the top gate ($V_{GS} = -40$ V).

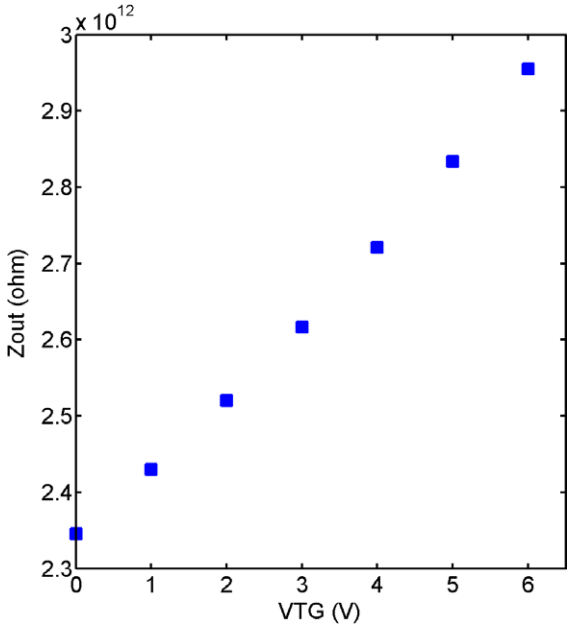

Fig. 13. The variation of the output impedance in the 200 nm thick dual gate OFET with the top gate voltage ($-60 < V_{DS} < -40$ V and $V_{GS} = -40$ V).

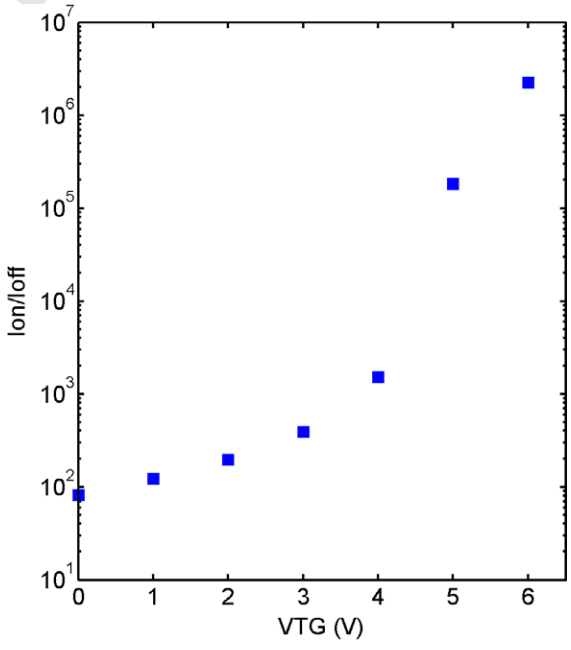

Fig. 14. The variation of the on/off current ratio in the 200 nm thick dual gate OFET with the top gate voltage ($V_{DS} = -0.5$ V).

thick dual gate OFET (Fig. 14), whereas the ratio is about 200 for an OFET with the same thickness.

Although the simulation results show that the performance of a dual gate thick film organic transistor can be better than that in a thin film OFET, the approach has some practical challenges. The most important one is the voltage stress between the top gate and the drain when the drain voltage reaches to −60 V. Such a large reverse voltage across the Schottky junction might cause breakdown in the device. In practice, the dual gate transistor approach is more suitable for a low voltage OFET or for limited drain voltage which restricts the operation modes to either the off mode or the linear regime same as in digital circuit applications.

5. Conclusion

To study the effect of the semiconductor thickness, a simple model consisting of an ideal IGFET and a resistor is applied to organic field-effect transistors. The analytical

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approach shows degradation of the performance with the thickness as the threshold voltage is changed and the output impedance and the current ratio are dropped. Simulation results from devices with thicknesses of between 20 and 200 nm support the model. A linear shift of the threshold voltage of 0.5 V is observed when the thickness is changed. Also, a 26% drop of the output impedance and a tenfold reduction in current ratio are obtained when the thickness is increased from 20 to 200 nm.

As a solution a dual gate FET structure is suggested in cases where there is a poor control of deposited semiconductor film thickness. The simulation results for a 200 nm thick dual gate OFET indicate an enhancement in the device performance by changing the secondary gate voltage. Application of 6 V to the top gate has shifted the threshold voltage by 0.5 V. Also, the output impedance is increased by a factor of 2.5. The most significant effect is on the current ratio which is improved by about four orders of magnitude. Altogether, the performance of a 200 nm thick dual gate OFET is better than a 20 nm thick OFET.

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