Towards Reliable 5Gbps Wave-pipelined and 3Gbps Surfing Interconnect in 65nm FPGAs

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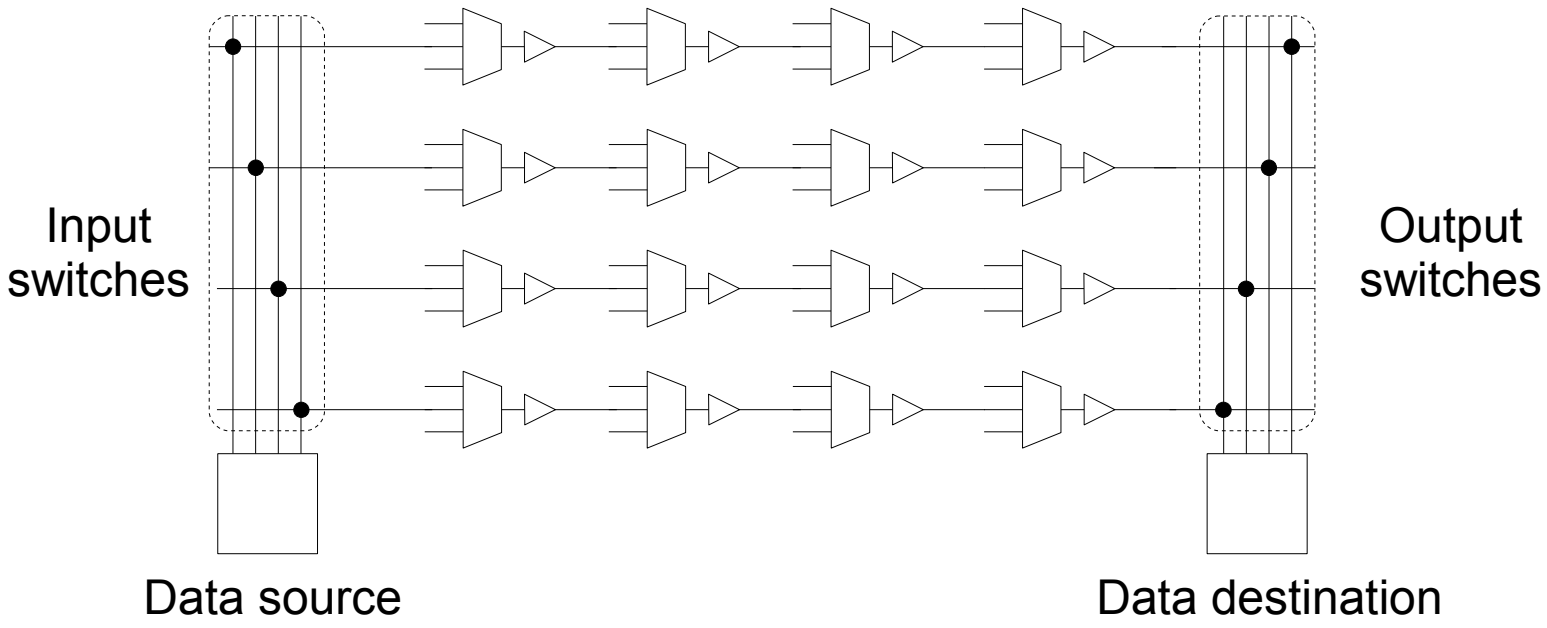
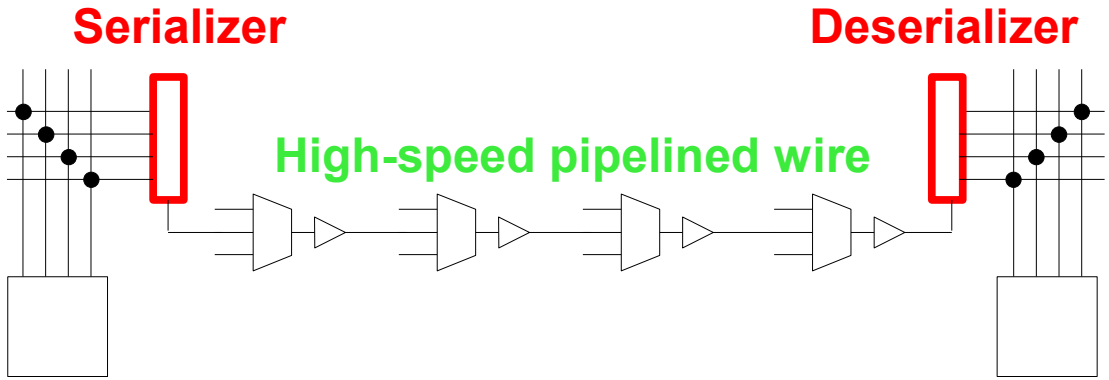
Guy Lemieux
Mark Greenstreet

Serial interconnect concept

Regular interconnect

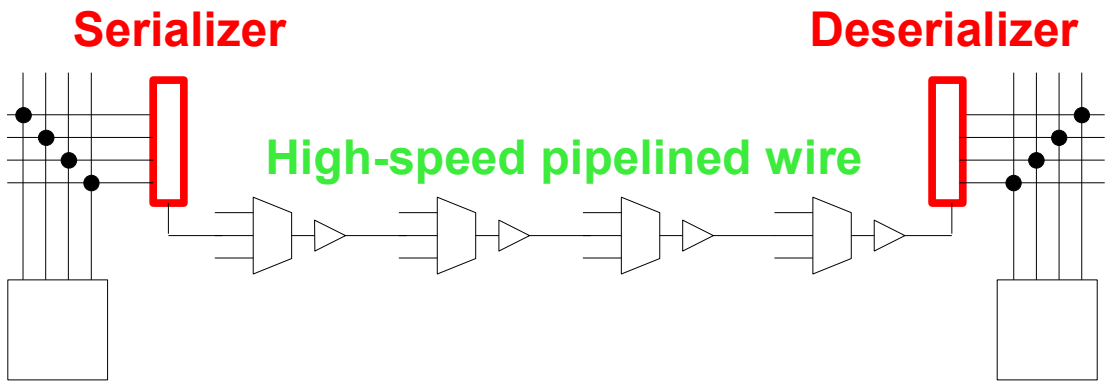


Serial interconnect



Motivation: Area and Bandwidth

- Wires use lots of area (muxes, buffers)
  - Serial may reduce total interconnect area
- Wire bandwidth usually 200Mbps (user clock)
  - Achievable wire bandwidth 30X higher
  - Serial good for high-throughput



Key points

Base design

- Wave pipelining, source synchronous timing
- Minimal modification to existing FPGA

Feasibility

- Very high throughput, good area savings
- Moderate to large latency and power penalties

Reliability

- Wave pipelining vulnerable to noise
- Use surfing pipelining for better robustness

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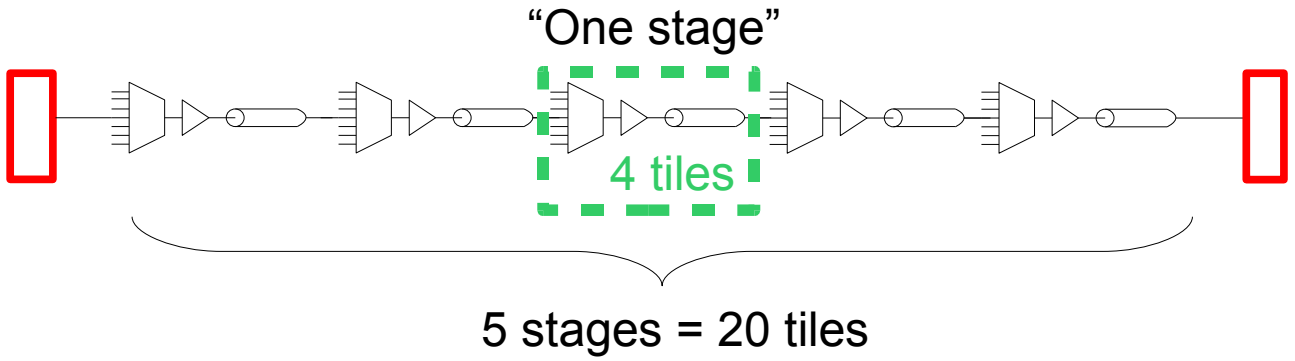
Design: Interconnect model

Multi-stage link:
circuit schematic



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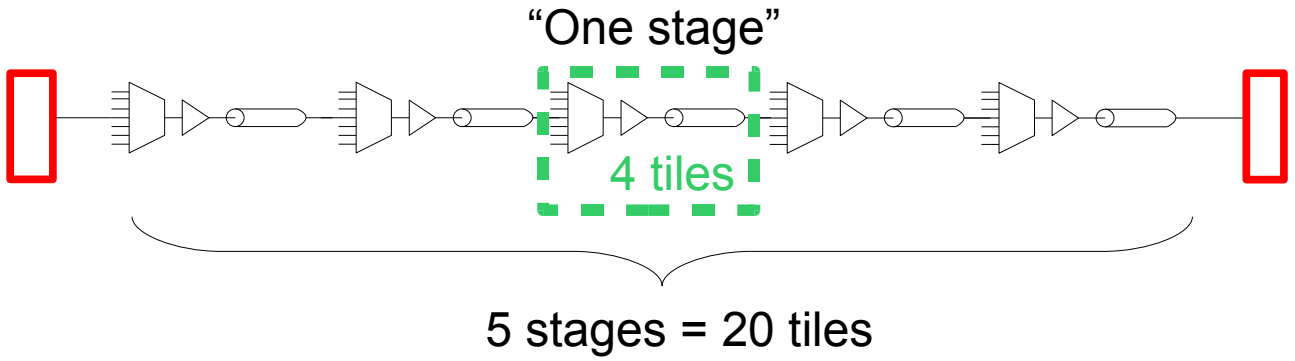
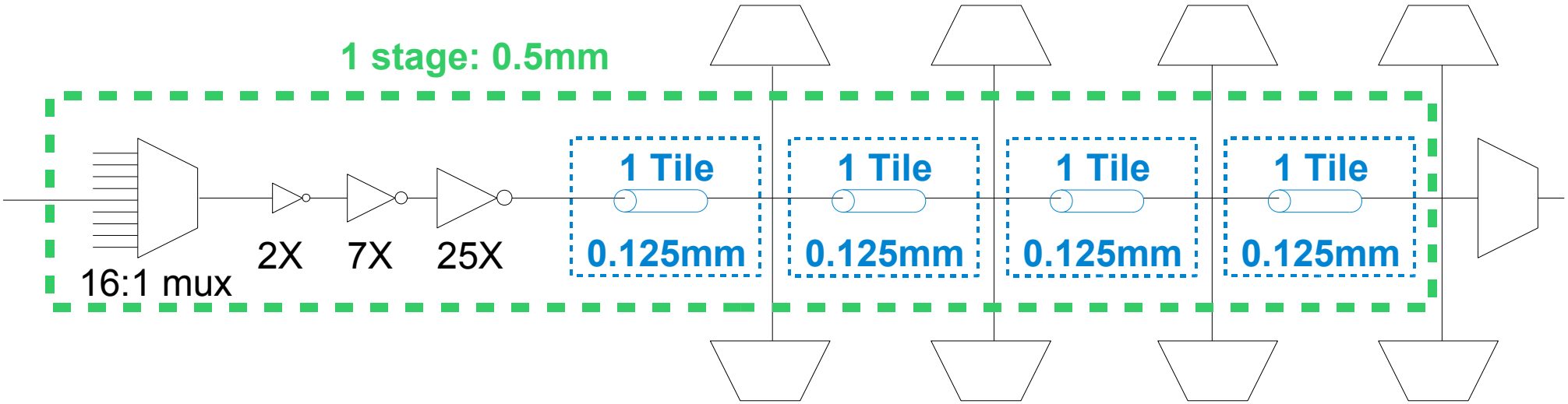
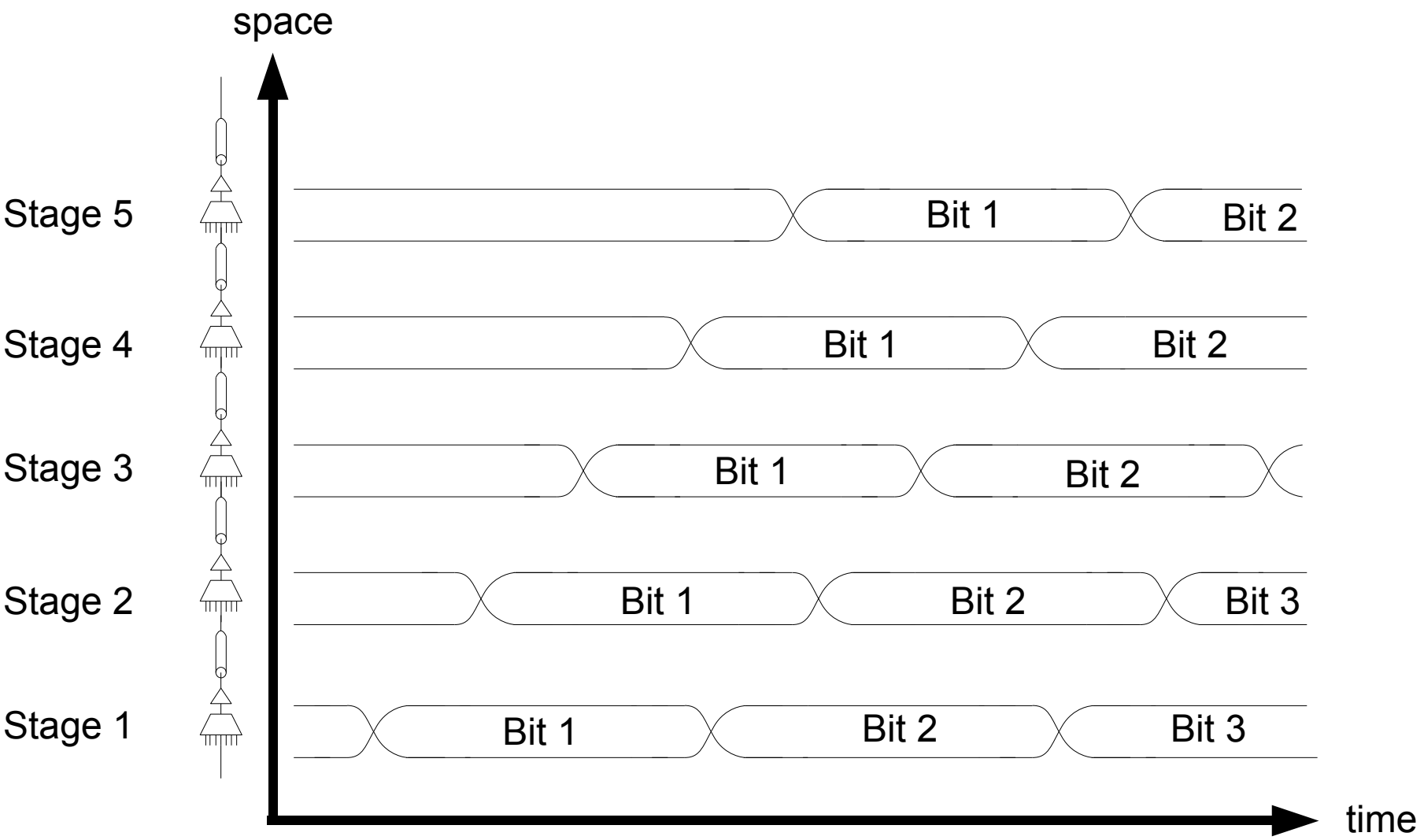




Design: Wave pipelining



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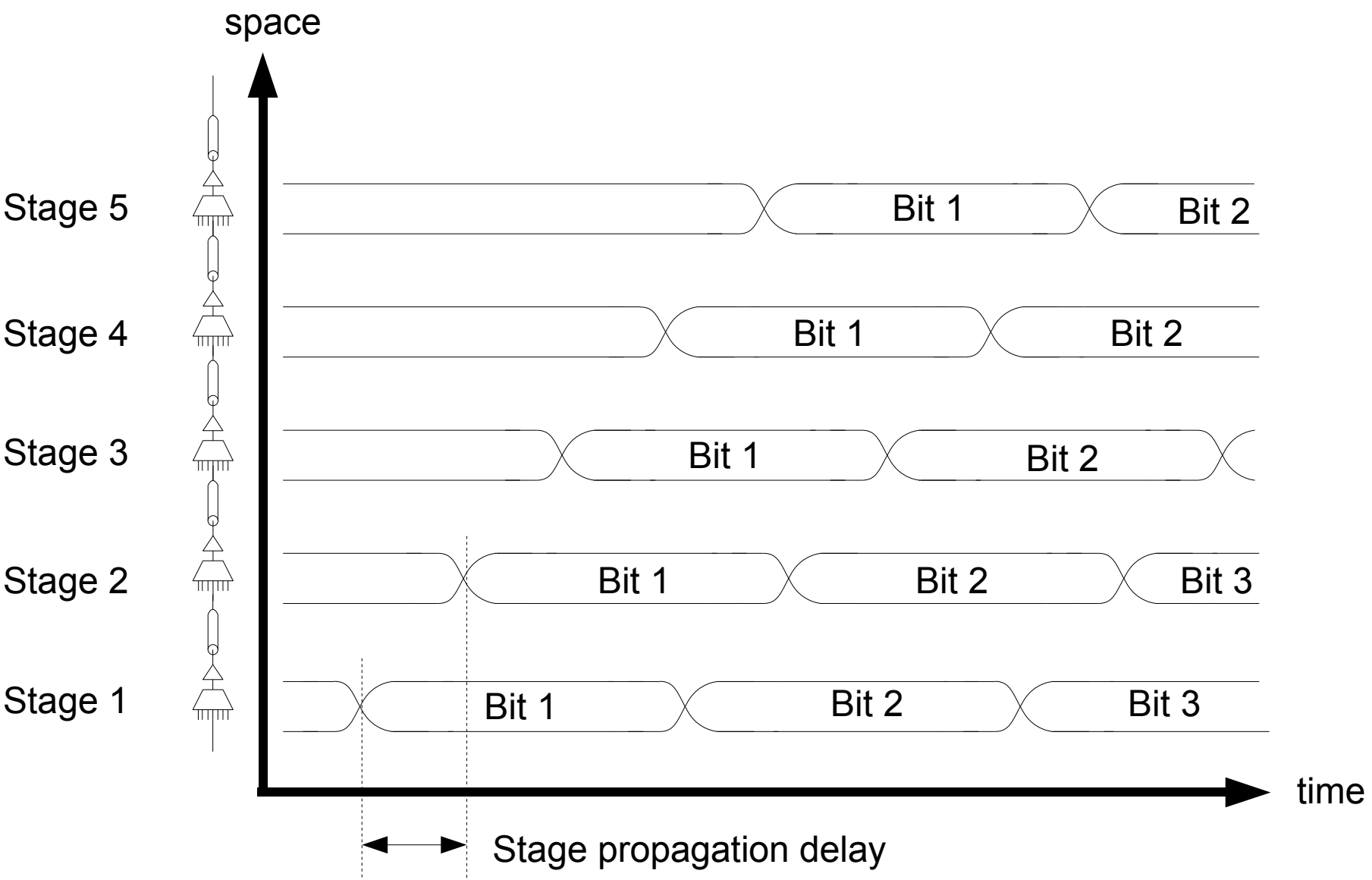
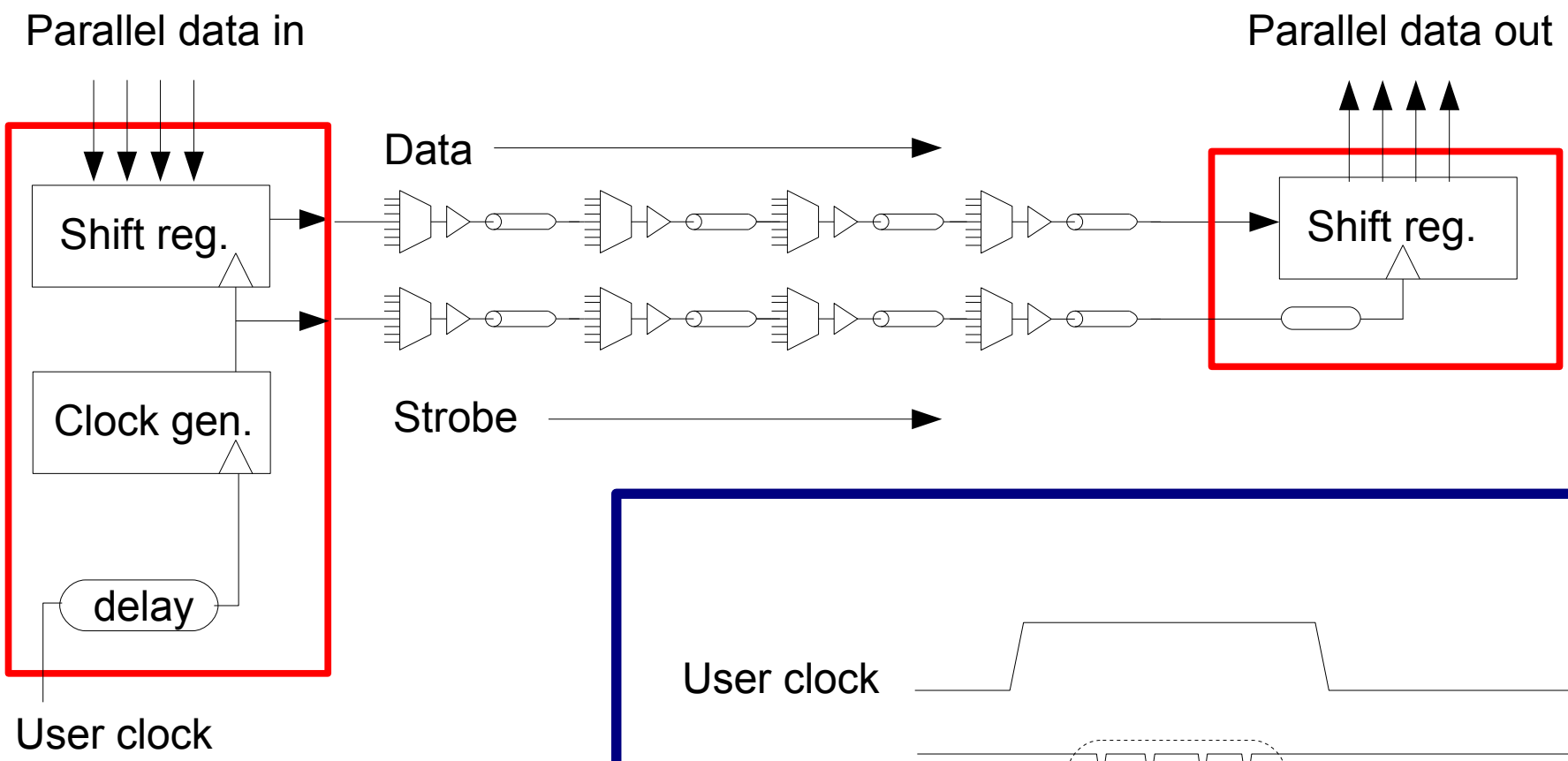
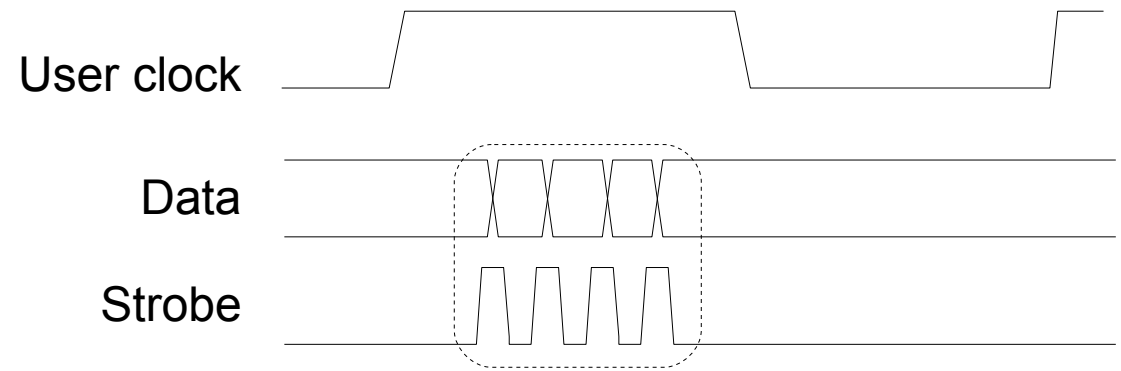


Design: Source-synchronous timing





Wave-pipelined transmission

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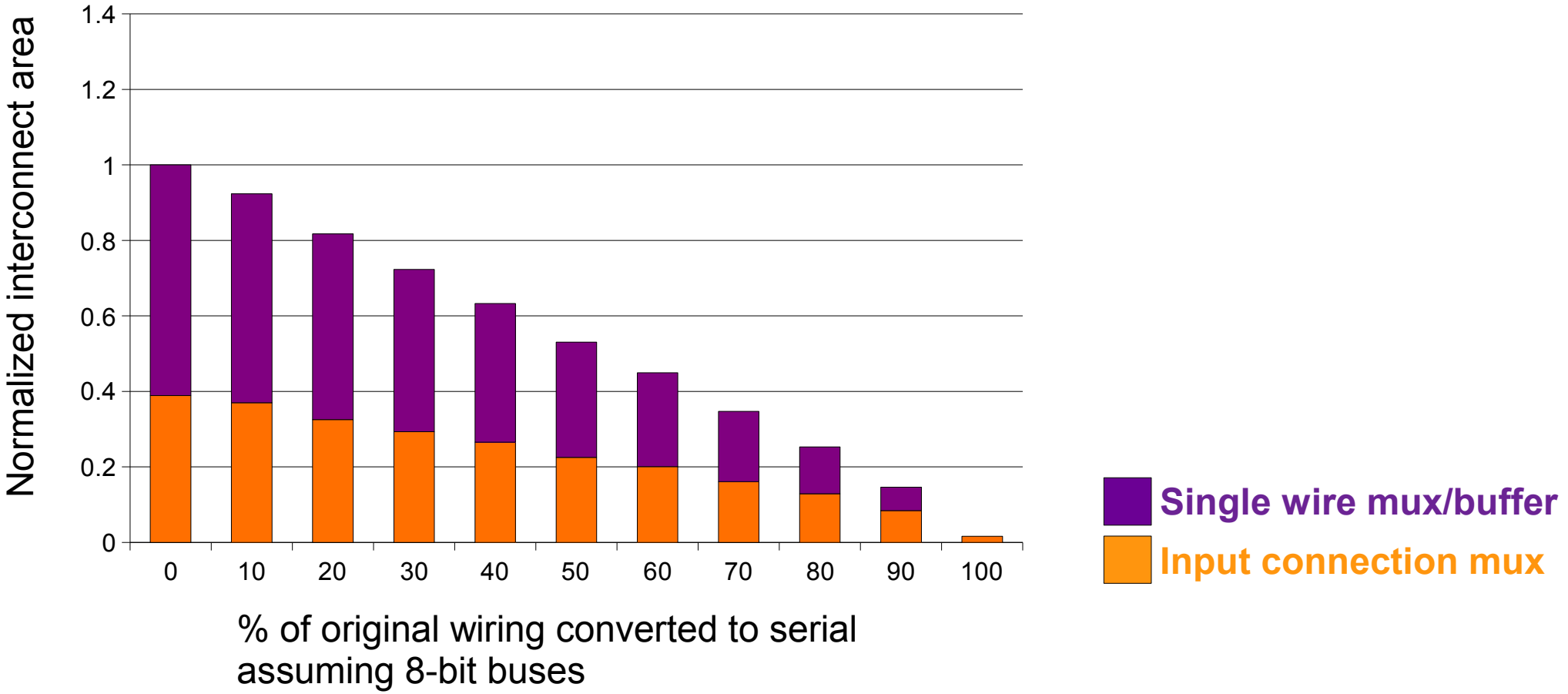
Interconnect area savings: 10-50%



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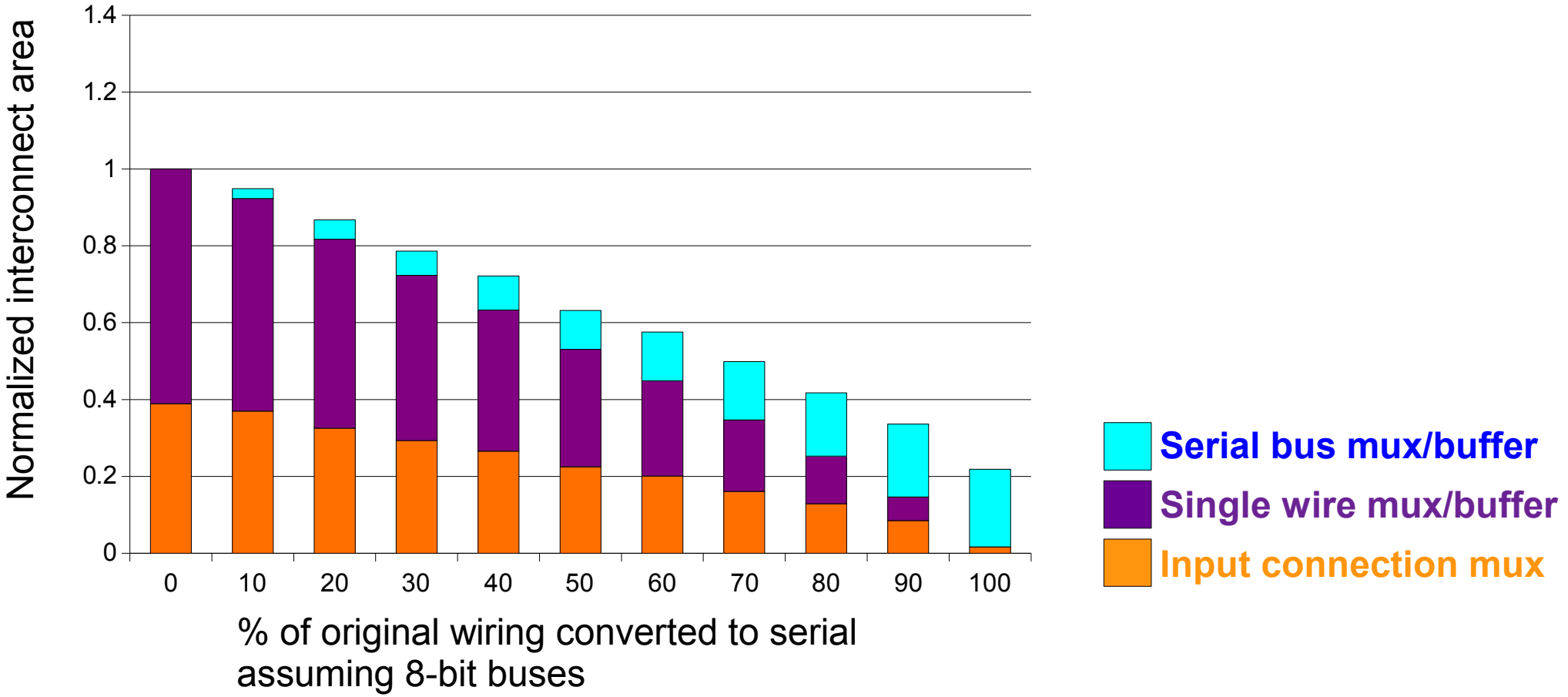

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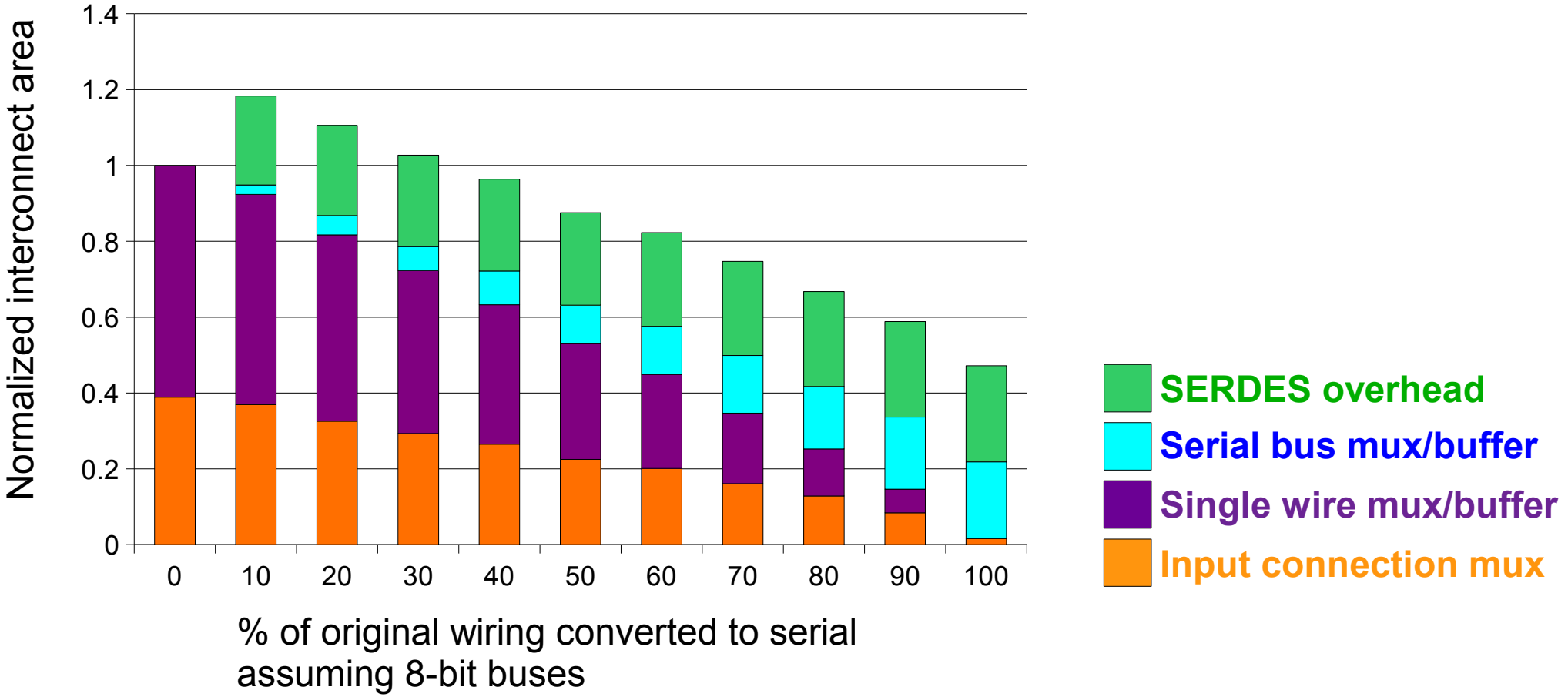
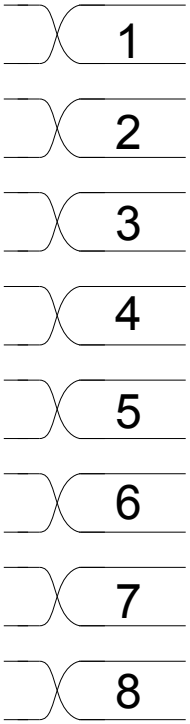


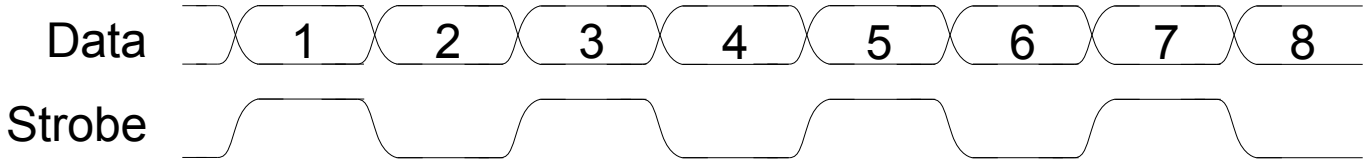
Significant power overhead

Parallel:
12.5% data activity



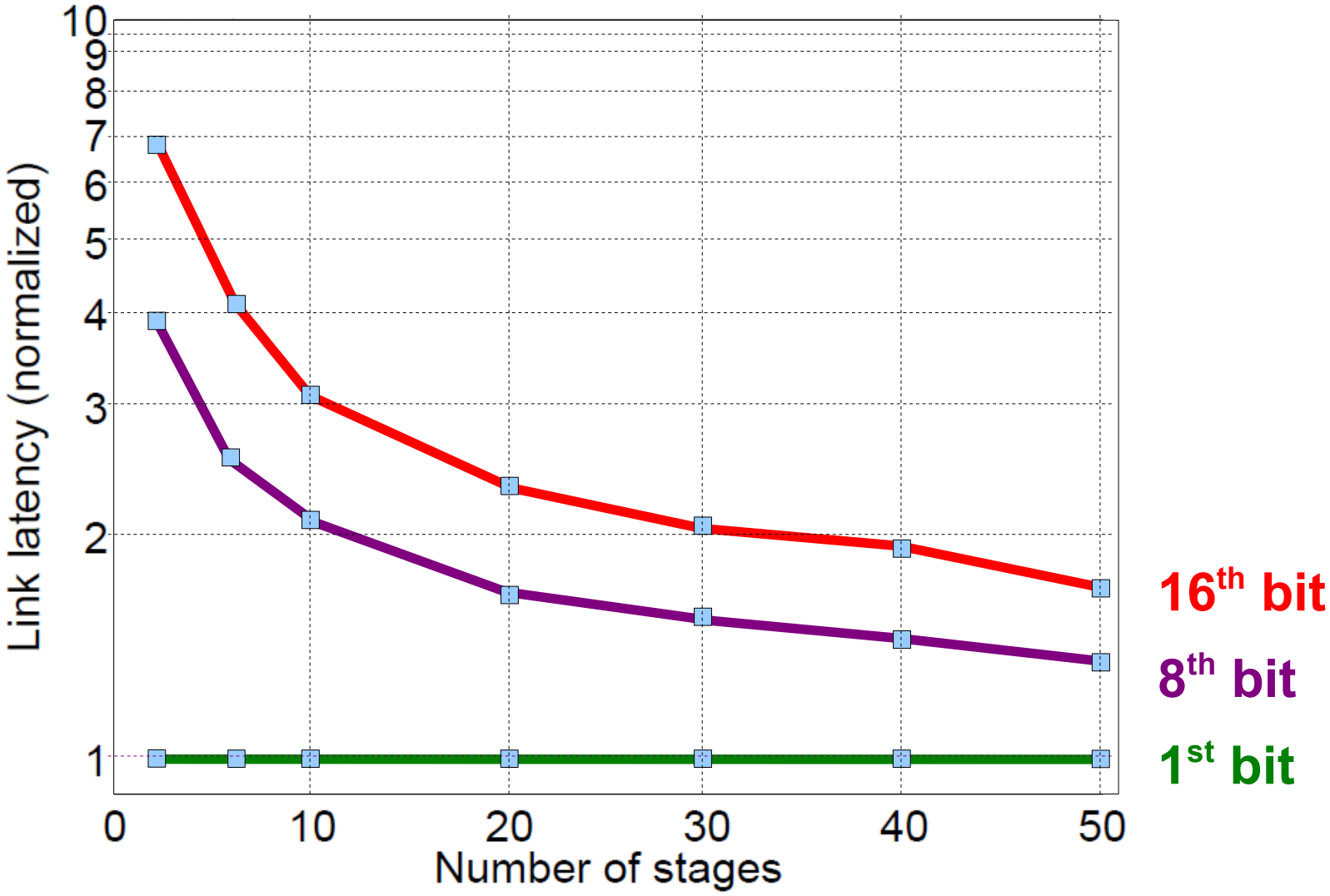
Serial:
50% data activity, 100% strobe activity

Power penalty 6X to 10X (future work)



DDR clocking to save power

Moderate latency overhead



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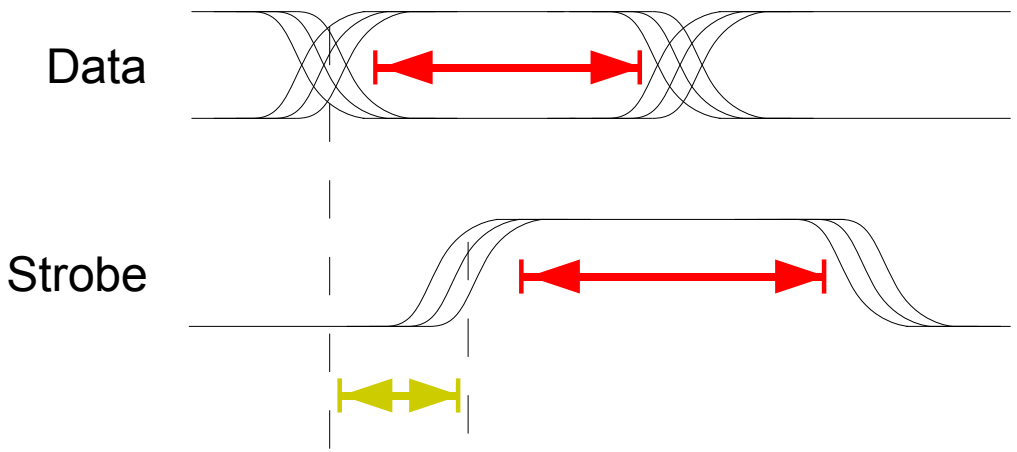
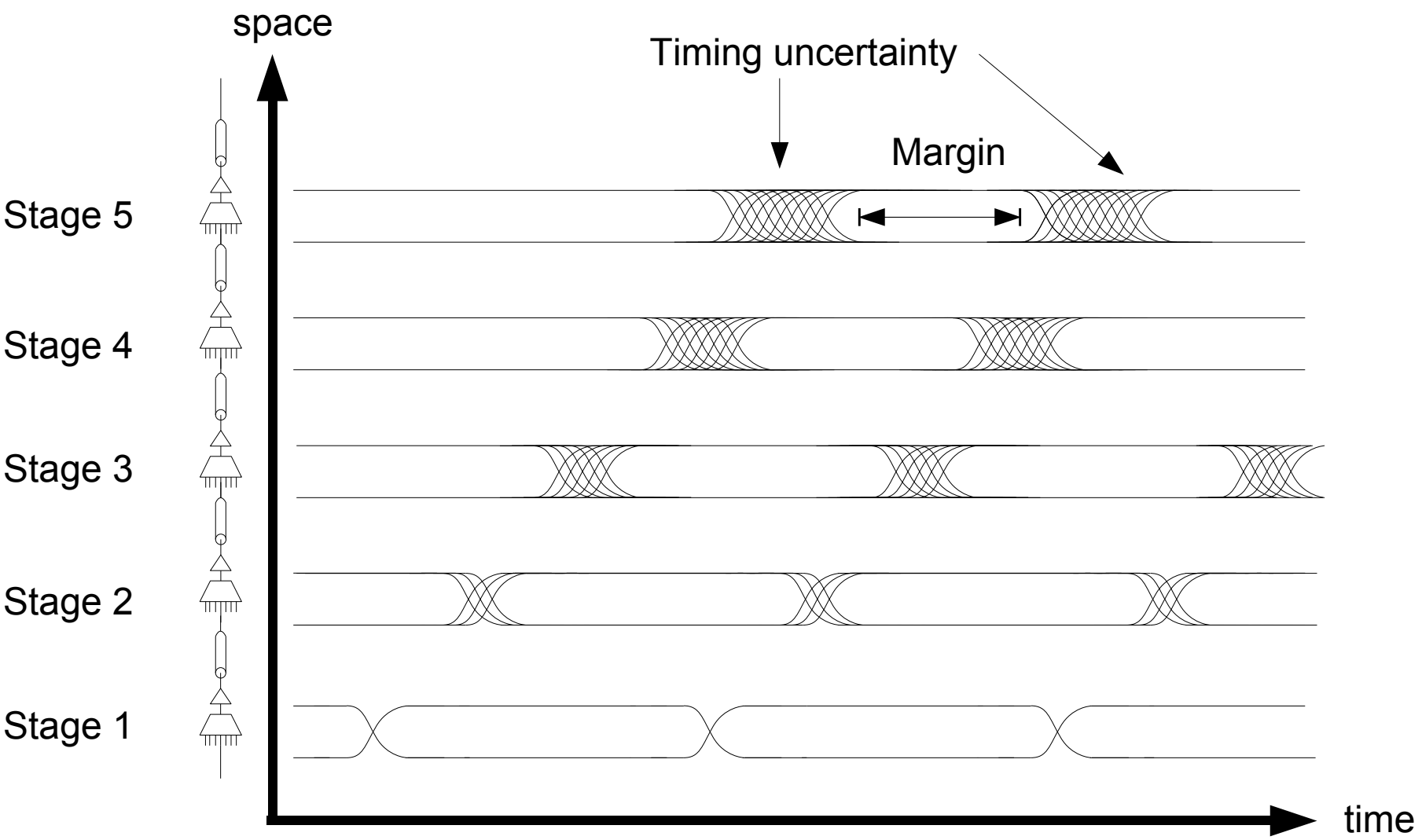
Timing uncertainty: failure modes

Jitter: pulses collapse



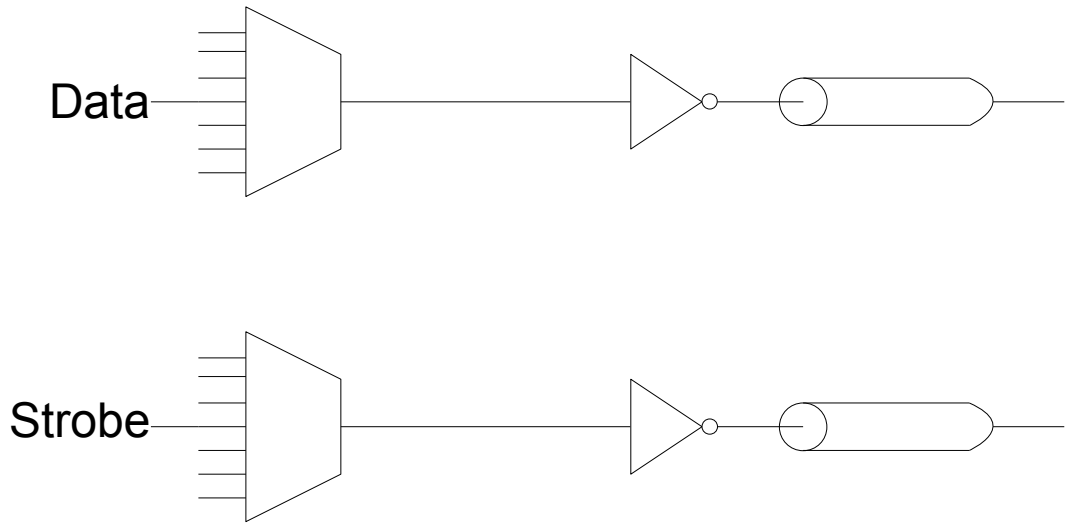
Skew: sampling failure

Timing uncertainty accumulates



Surfing: removing timing uncertainty

- Add feedback and control
- Variable-strength buffers modulate timing



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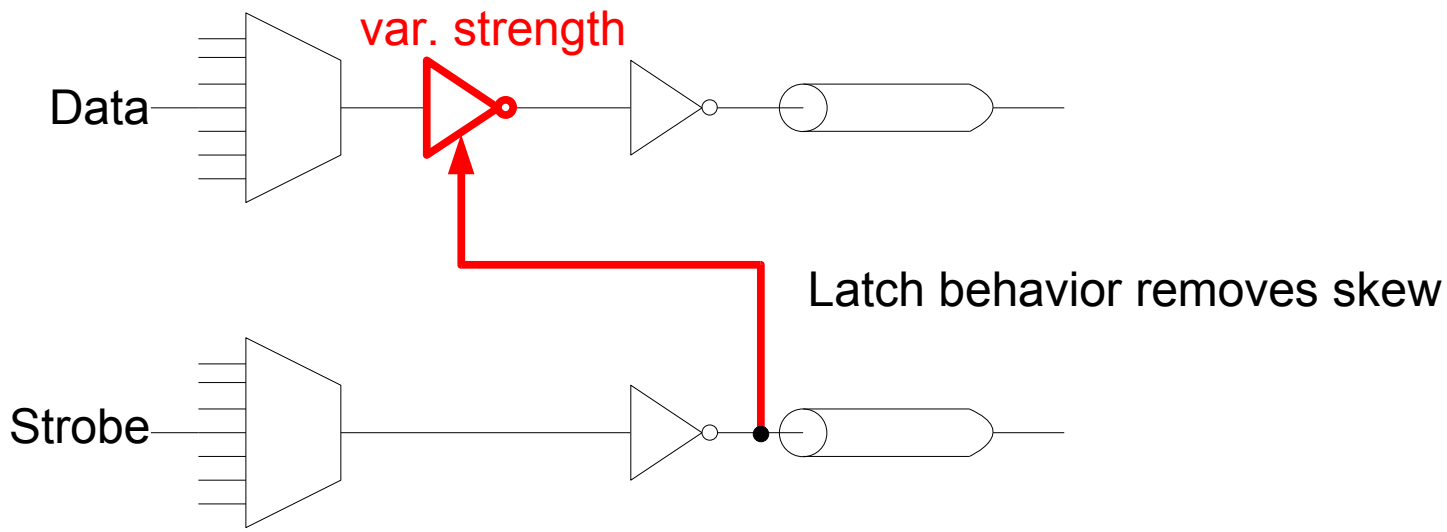

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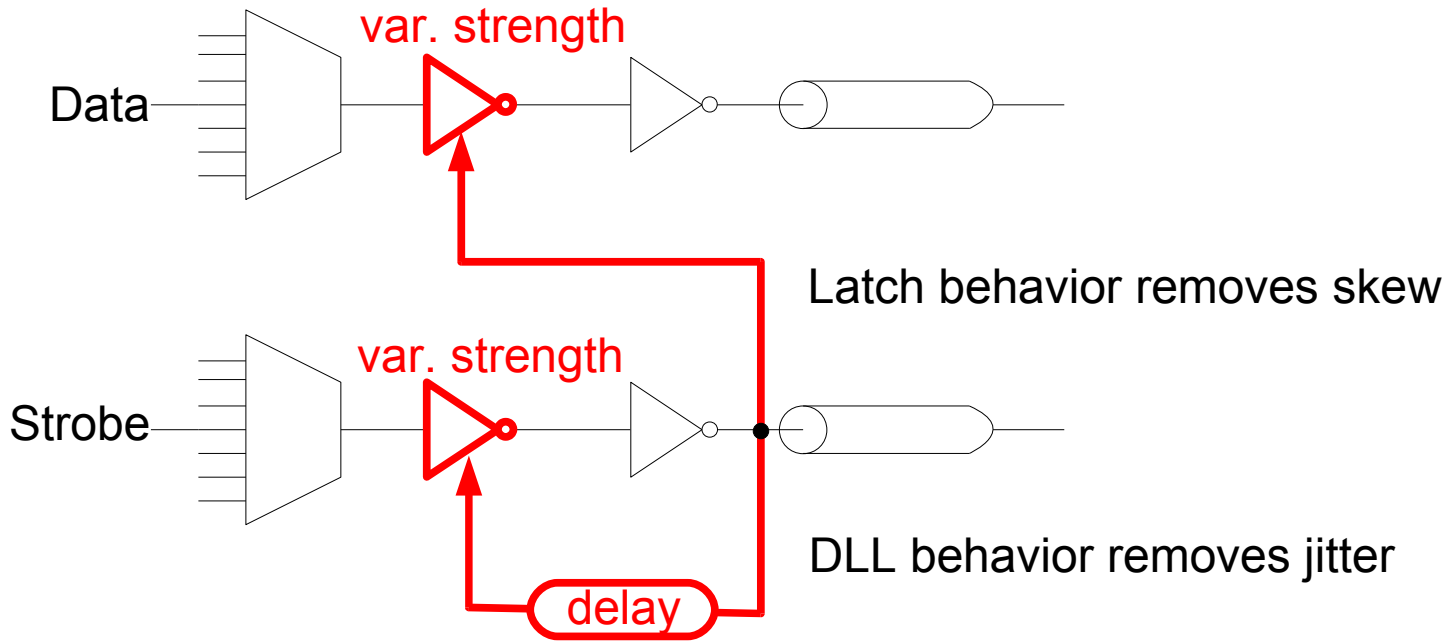
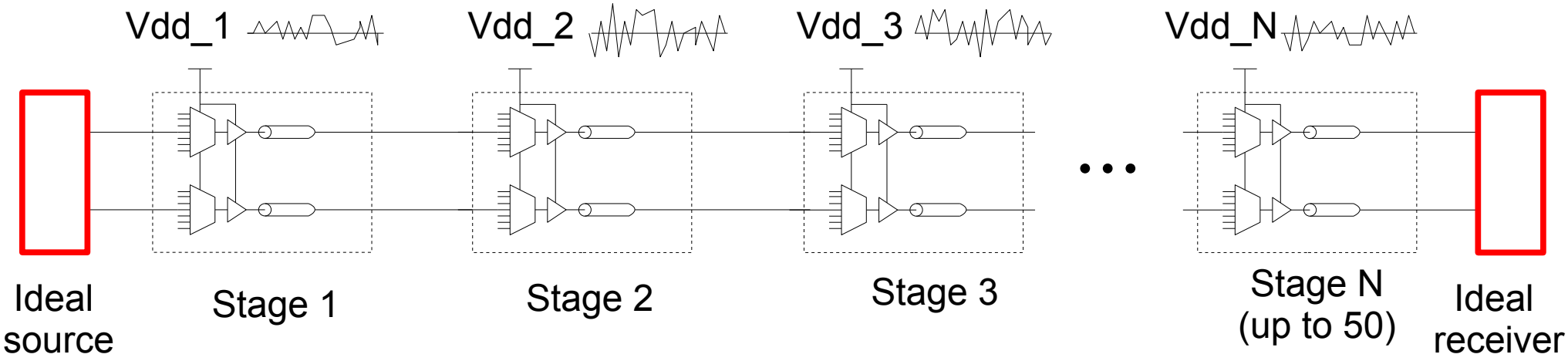
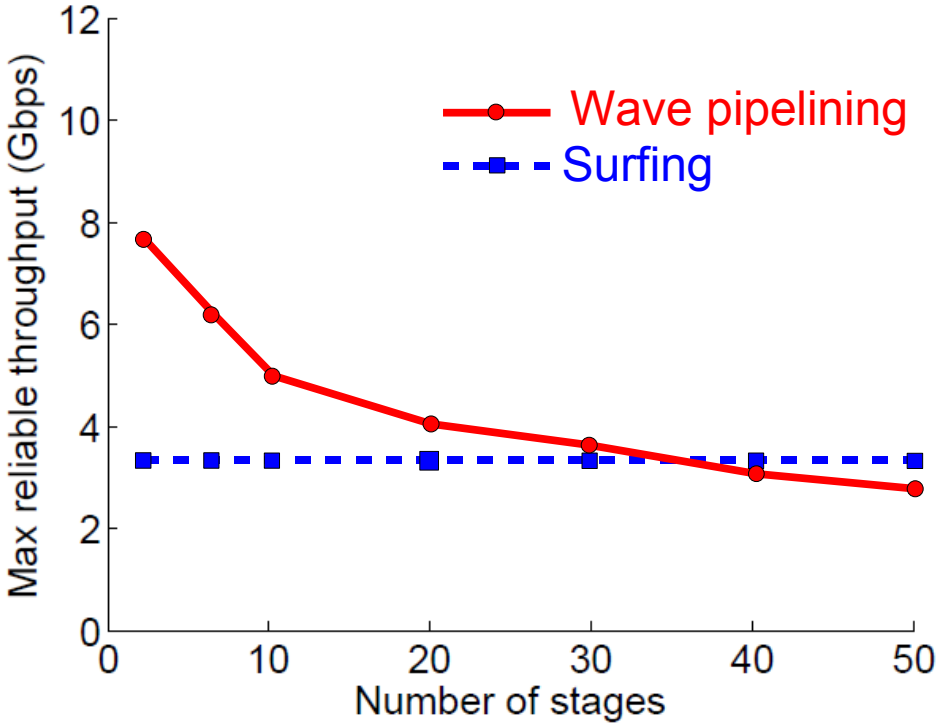


Simulation prototype circuit

- Goal: Determine maximum safe throughput
- Compare wave pipelining with surfing
- Add Vdd noise to create timing uncertainty

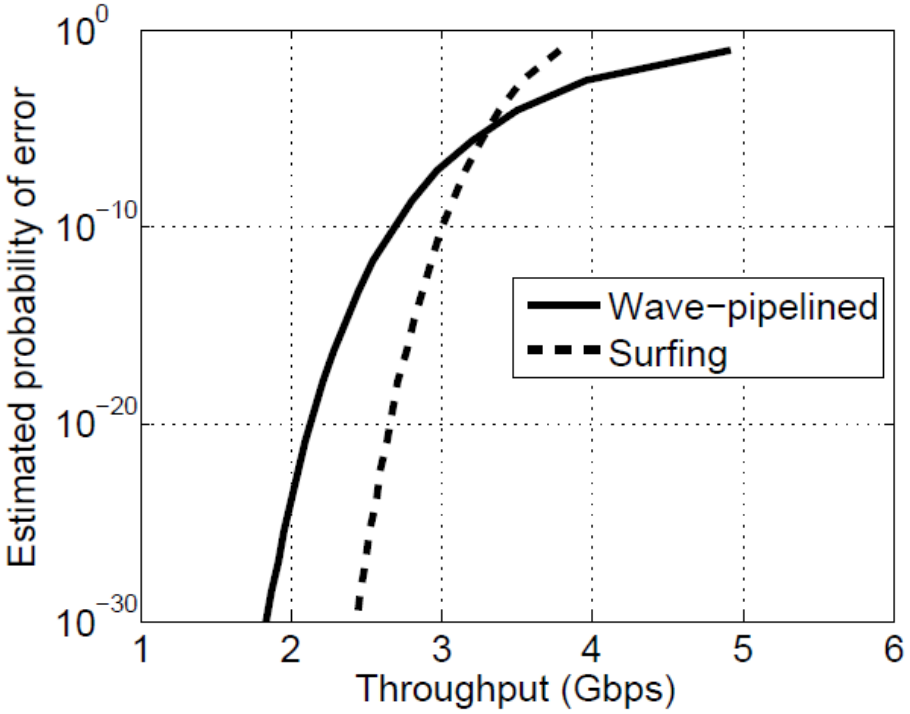


Throughput vs link length

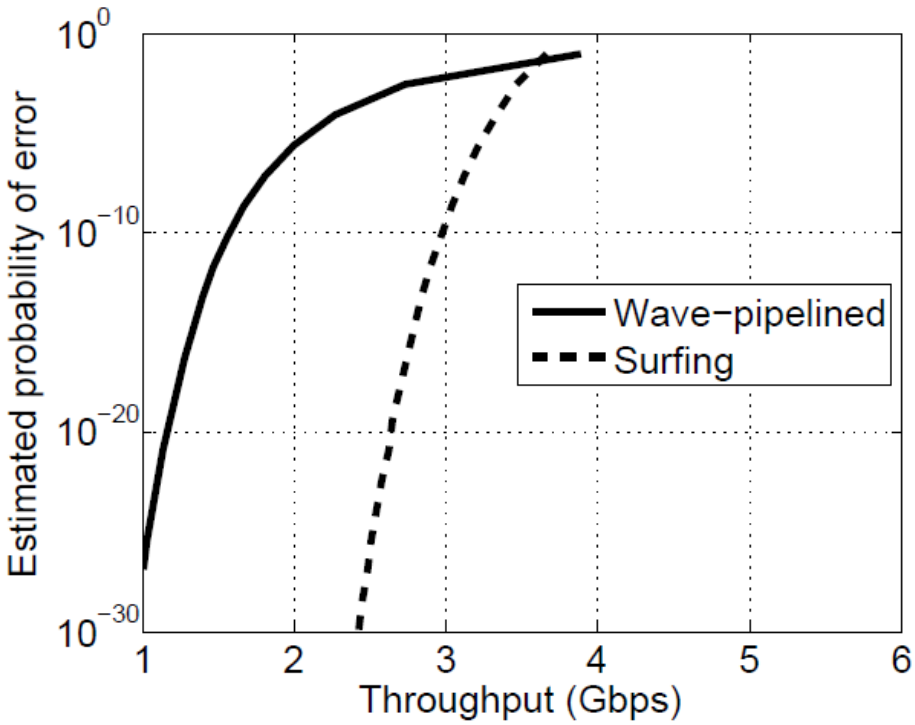


- Measured from 65nm HSPICE simulation with moderate supply noise
- Wave pipelining faster, surfing more robust

Throughput vs probability of error



10-stage link



50-stage link

- Calculate P(E) assuming normal random noise
- Surfing much more robust

Summary

- Serial pipelined interconnect enables very high throughput, large area savings
  - Surfing: robust at 3Gbps
  - Wave pipelining: up to 5Gbps, but less robust
  - Future work: robust high speed wave pipelining
  - Future work: architectural study/benchmarking
- Latency, power penalties are high
  - Future work: low-power signaling schemes
- Pay attention to reliability

Acknowledgements

Suwen Yang: UBC

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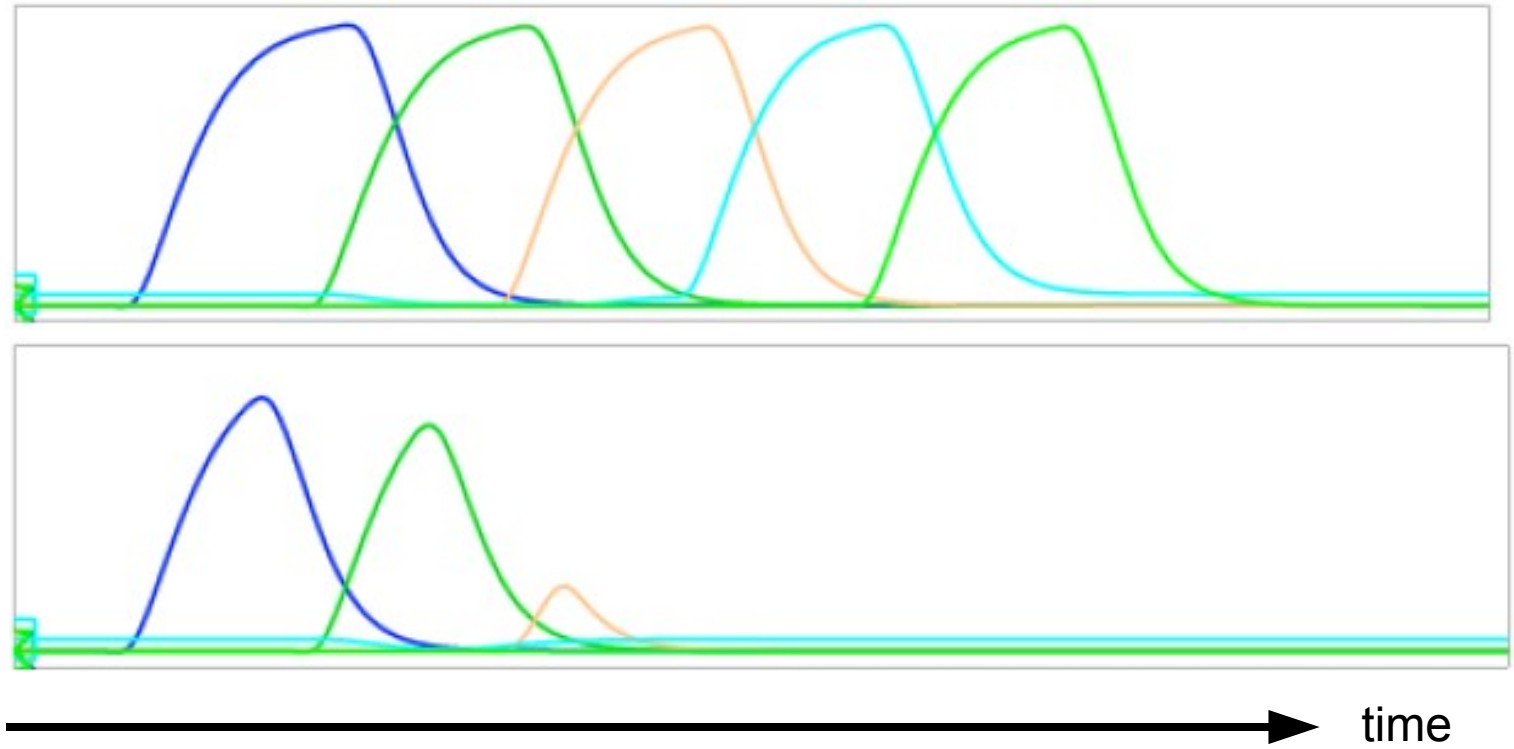
Narrow pulses get dropped

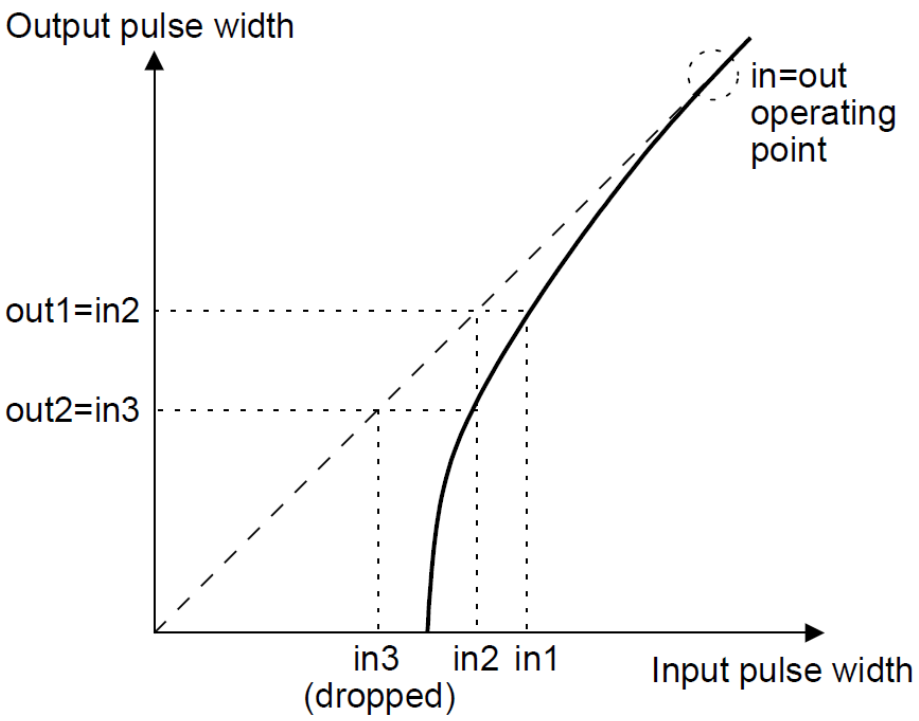
Voltage waveforms of first 5 stages

Safe pulse width (150ps)

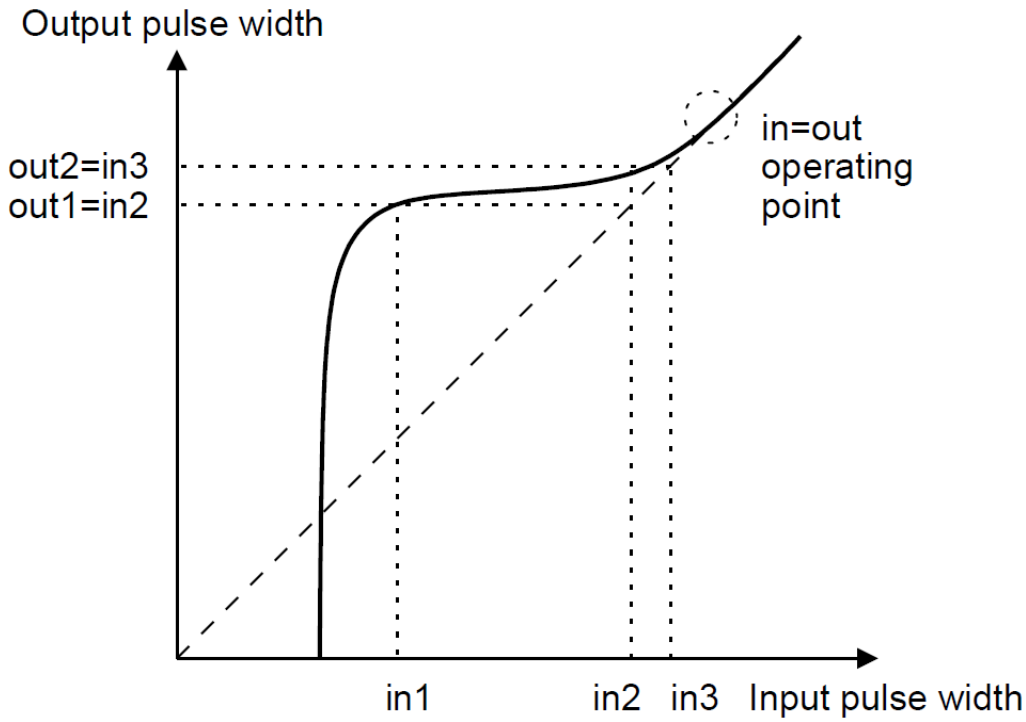
Unsafe pulse width (90ps)



Pulse transfer behavior



Wave pipelining
(unstable)



Surfing
(stable)

Waveforms

Wave pipelining

Surfing