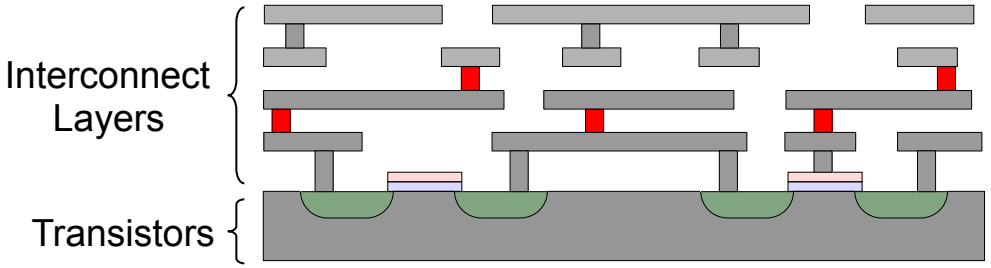
Impact of **Interconnect Architecture** on **VPSAs** (Via-Programmed Structured ASICs)

Usman Ahmed **Guy Lemieux** Steve Wilton

System-on-Chip Lab
University of British Columbia

What is a Structured ASIC?

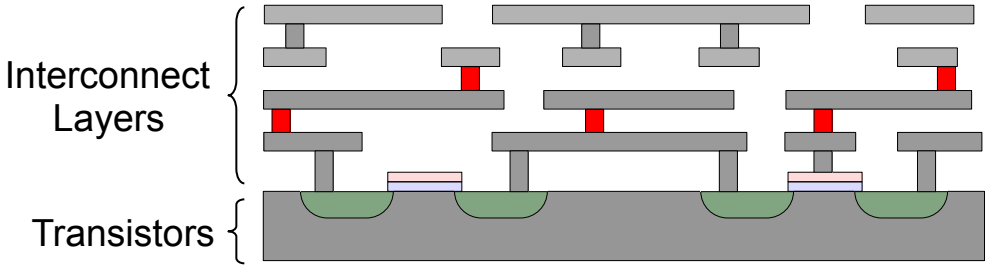
- An FPGA without **re**programmable interconnect
  - Interconnect is mask-programmed



What is a Structured ASIC?

- An FPGA without **re**programmable interconnect
  - Interconnect is mask-programmed
- Two types

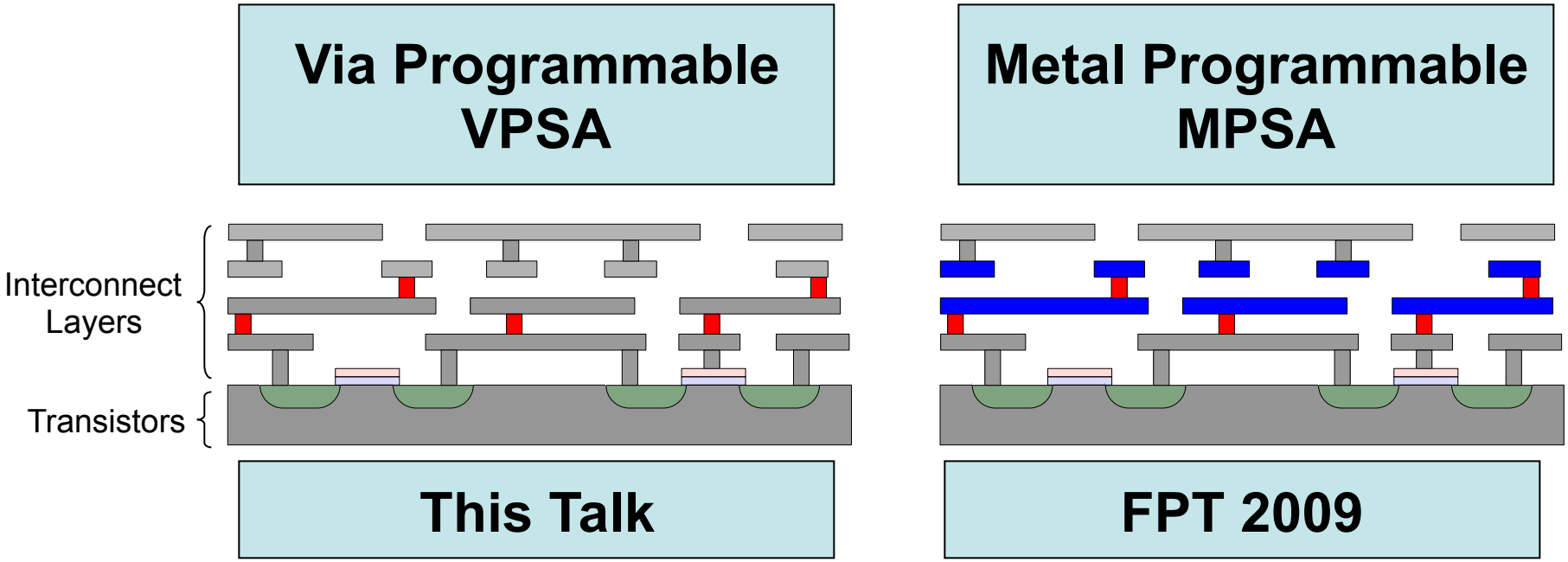
Via Programmable VPSA



This Talk

What is a Structured ASIC?

- An FPGA without **re**programmable interconnect
  - Interconnect is mask-programmed
- Two types



Key Messages

1. Structured ASICs
will be the key technology
of the future.

Key Messages

1. Structured ASICs
will be the key technology
of the future.

Because the **key issues** that
make structured ASICs attractive
have **not been solved**.

They are growing **more prominent**.

Key Messages

1. Structured ASICs
will be the key technology
of the future.

Because the **key issues** that
make structured ASICs attractive
have **not been solved**.

They are growing **more prominent**.

2. Interconnect matters.

MPSAs have better performance,
VPSAs are cheaper.

Motivation for Structured ASICs

- Enormous NRE + Design cost
  limit access to advanced process

Talk Outline

- Cost model
- Experimental methodology
  - Metrics
  - CAD flow
  - Architecture modeling
- Area, cost trends
- Conclusions

Talk Outline

- Cost model
- Experimental methodology
  - Metrics
  - CAD flow
  - Architecture modeling
- Area, cost trends
- Conclusions

VPSA Die-Cost

- Cost is more important than die area
- Primary cost components
  - Die Area
  - Number of configurable layers *(New for structured ASICs)*
- Secondary cost components
  - Die Yield
  - Wafer and processing cost
  - Volume requirements

VPSA Cost Model

$$Cost_{die} = C_{base} +$$

$$C_{custom} +$$

$$C_{proto}$$

VPSA Cost Model

$$Cost_{die} = \textit{Cost of the masks for the base (common portion)} + \textit{Cost of fabricating the base portion} +$$

$$C_{custom} +$$

$$C_{proto}$$

VPSA Cost Model

$$Cost_{die} = \textit{Cost of the masks for the base (common portion)} + \textit{Cost of fabricating the base portion} +$$

$$\textit{Cost of the remaining masks} + \textit{Cost of fabricating the remaining portion} +$$

$$C_{proto}$$

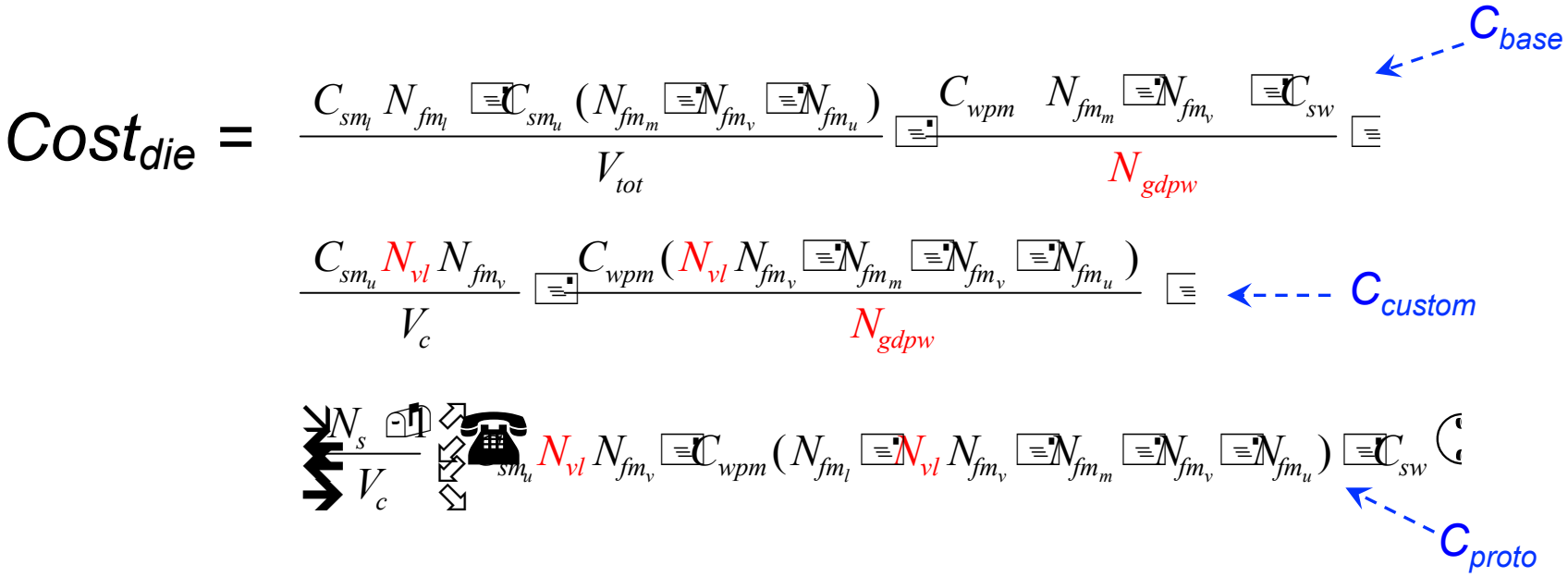
VPSA Cost Model

$Cost_{die}$ = *Cost of the masks for the base (common portion)* + *Cost of fabricating the base portion* +

Cost of the remaining masks + *Cost of fabricating the remaining portion* +

Similar to C_{custom}, but depends on the number of spins

VPSA Cost Model



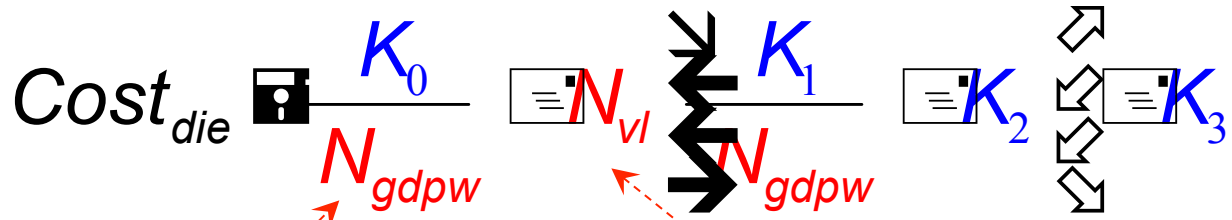
- Die Area and Yield: N_{gdpw}
- Configurable layers: N_{vl}

} Primary Cost Variables

- Fixed layers: N_{fm_l}, N_{fm_m}, N_{fm_v}, N_{fm_u}
- Mask/wafer cost: C_{sml}, C_{smu}, C_{wpm}, N_{mprl}
- Volume requirements: V_{tot}, V_c

} Constants

VPSA Cost Model



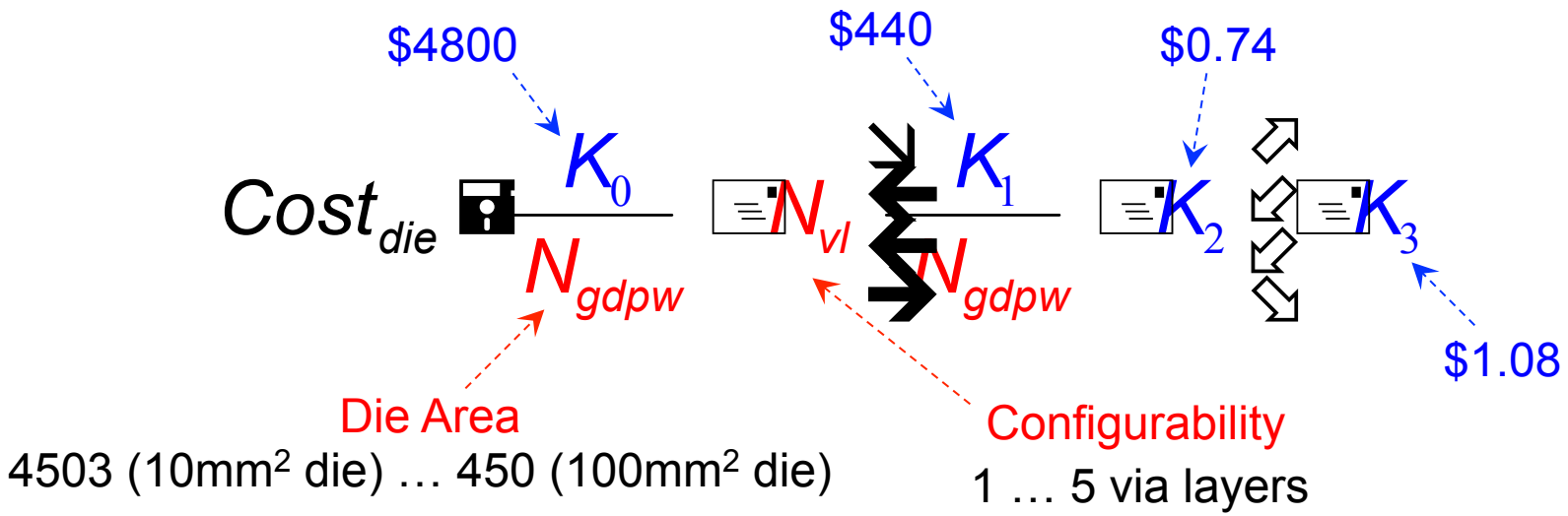
Die Area

4503 (10mm^2 die) … 450 (100mm^2 die)

Configurability

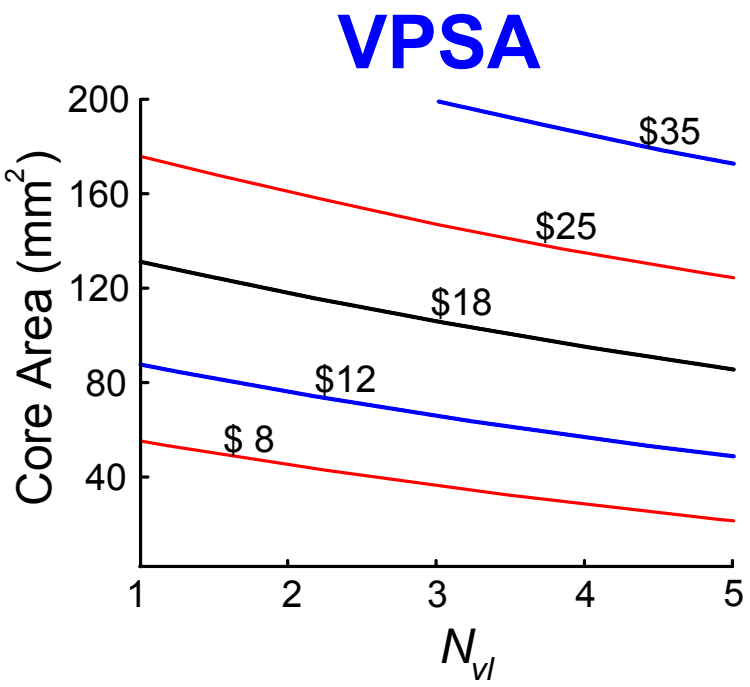
1 … 5 via layers

VPSA Cost Model



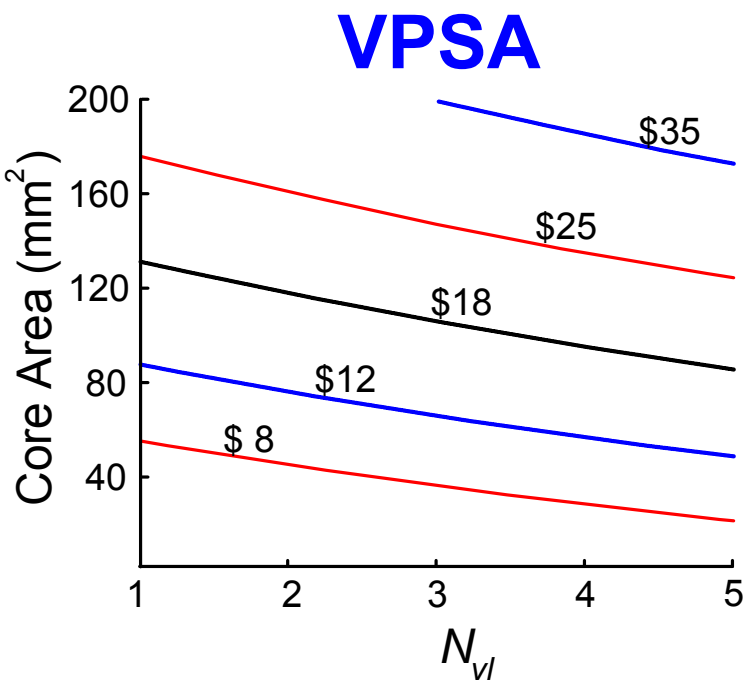
- *Key Assumptions*
  - 45nm Maskset cost: $2.5M
  - Total volume: 2M
  - Per-customer volume: 100k
  - No. of spins: 2

VPSA Cost Model



- At constant cost, area can be traded for number of customizable layers

VPSA Cost Model

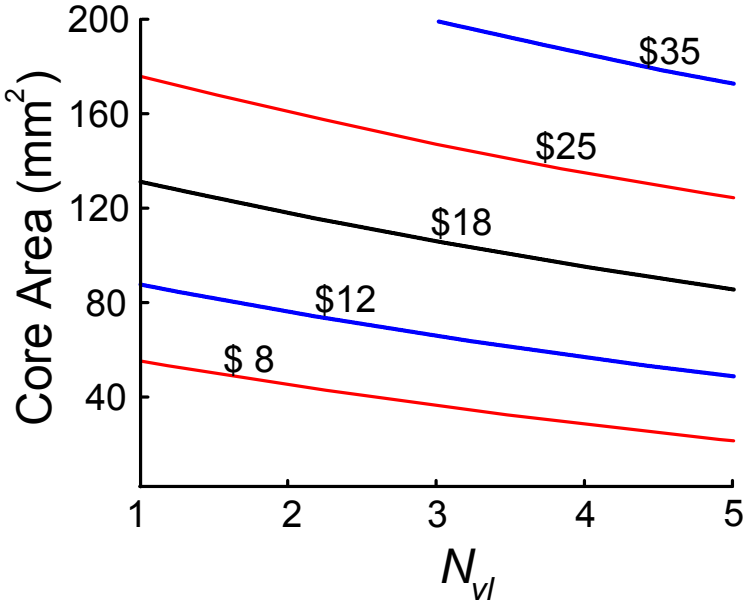


11 mm^2/layer

- At constant cost, area can be traded for number of customizable layers

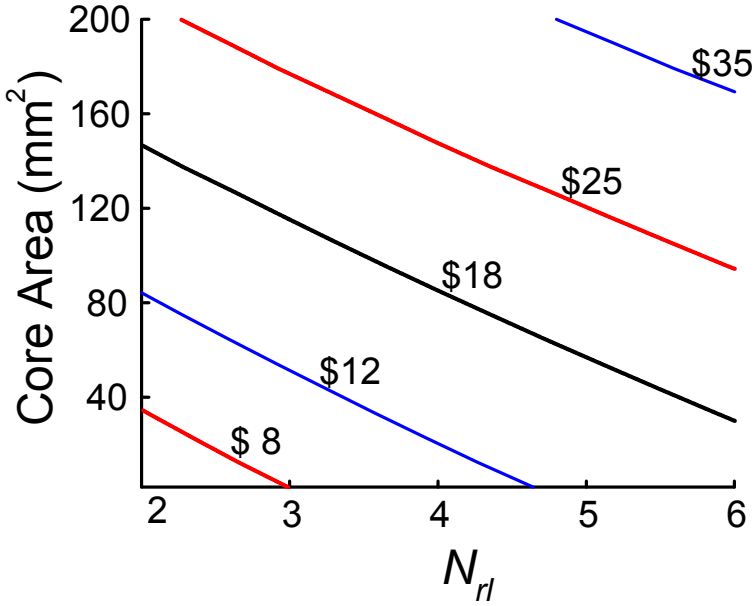
VPSA Cost Model

VPSA



11 mm^2/layer

MPSA



30 mm^2/layer

- At constant cost, area can be traded for number of customizable layers

Talk Outline

- Cost model
- Experimental methodology
  - Metrics
  - CAD flow
  - Architecture modeling
- Area, cost trends
- Conclusions

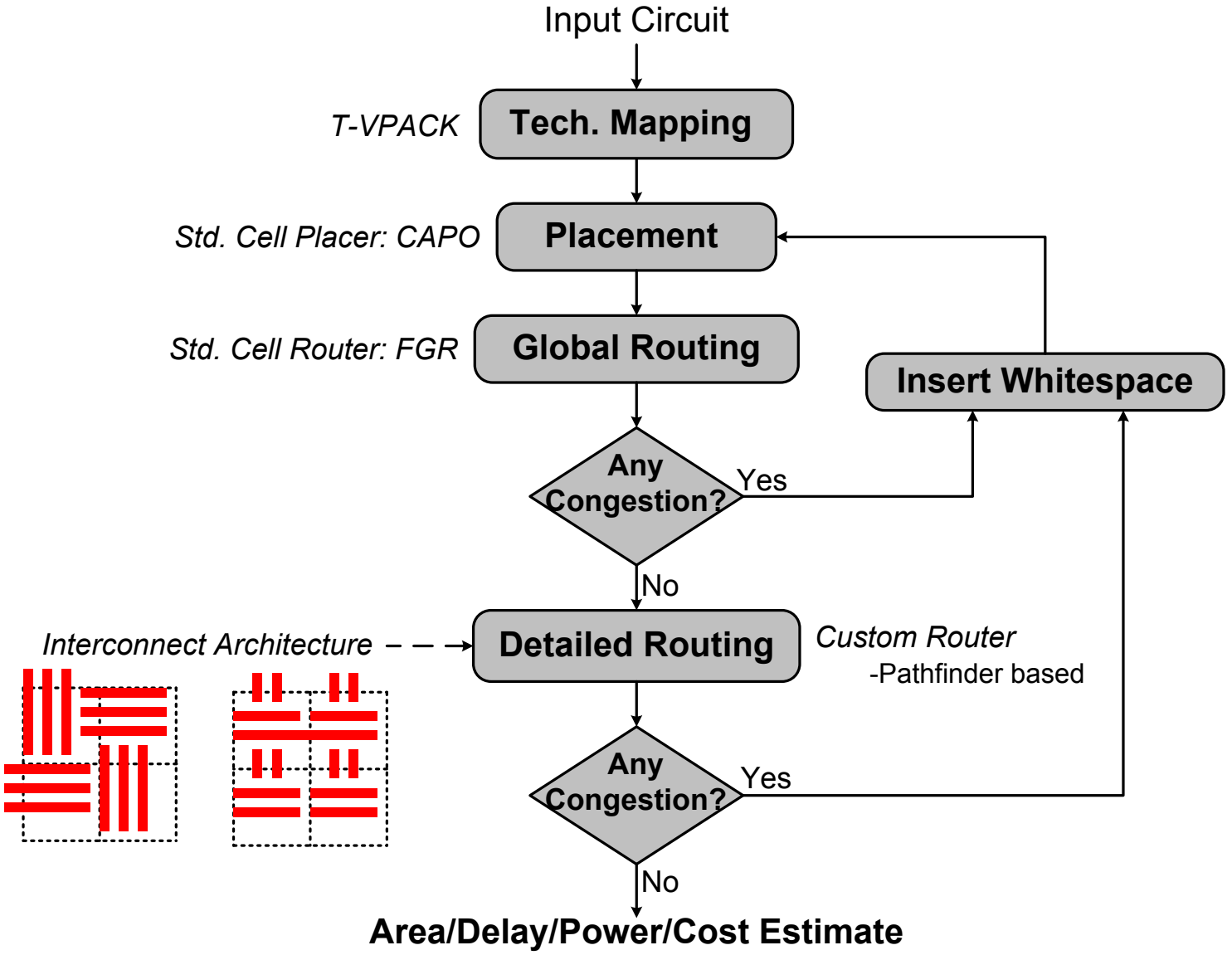
Metrics

- Cost
  - Detailed cost model (just presented)
- Area
  - Placement grid size after whitespace insertion
    - Determined by CAD flow
- Delay and Power
  - Please see paper

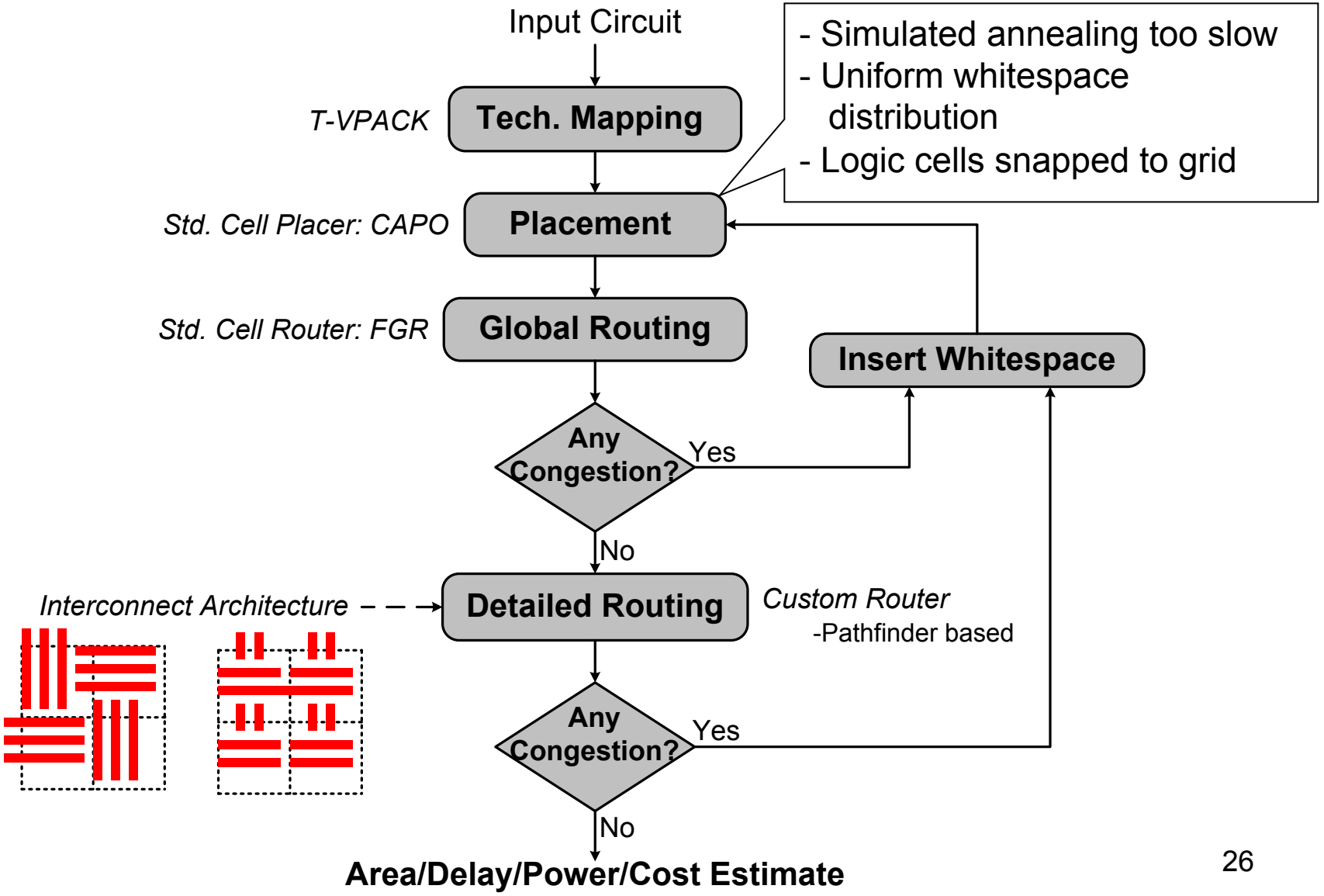
Talk Outline

- Cost model
- Experimental methodology
  - Metrics
  - CAD flow
  - Architecture modeling
- Area, cost trends
- Conclusions

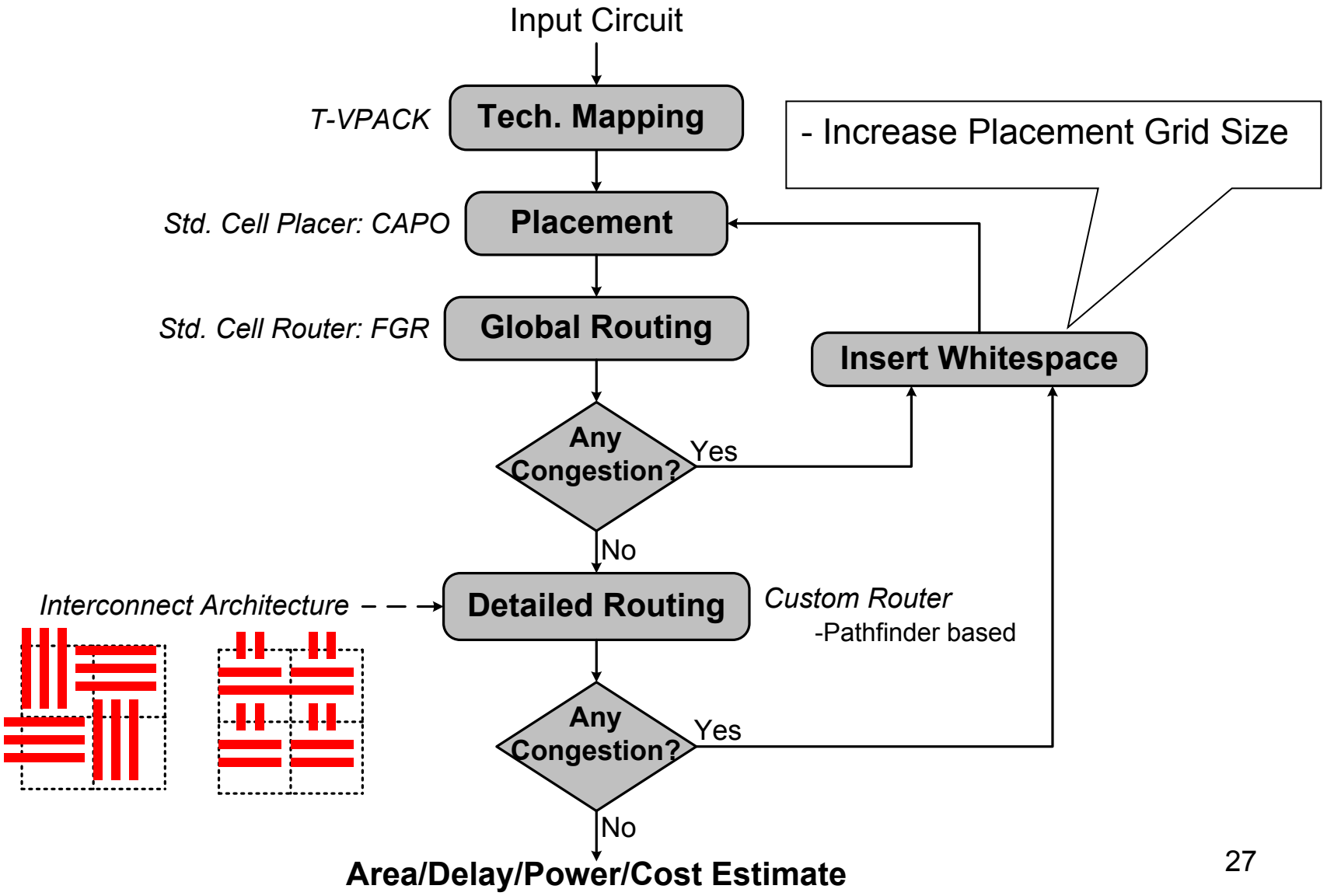
CAD Flow


Input Circuit
T-VPACK
Tech. Mapping
Std. Cell Placer: CAPO
Placement
Std. Cell Router: FGR
Global Routing
Insert Whitespace
Any Congestion?
Yes
No
Interconnect Architecture
Detailed Routing
Custom Router
-Pathfinder based
Any Congestion?
Yes
No
Area/Delay/Power/Cost Estimate

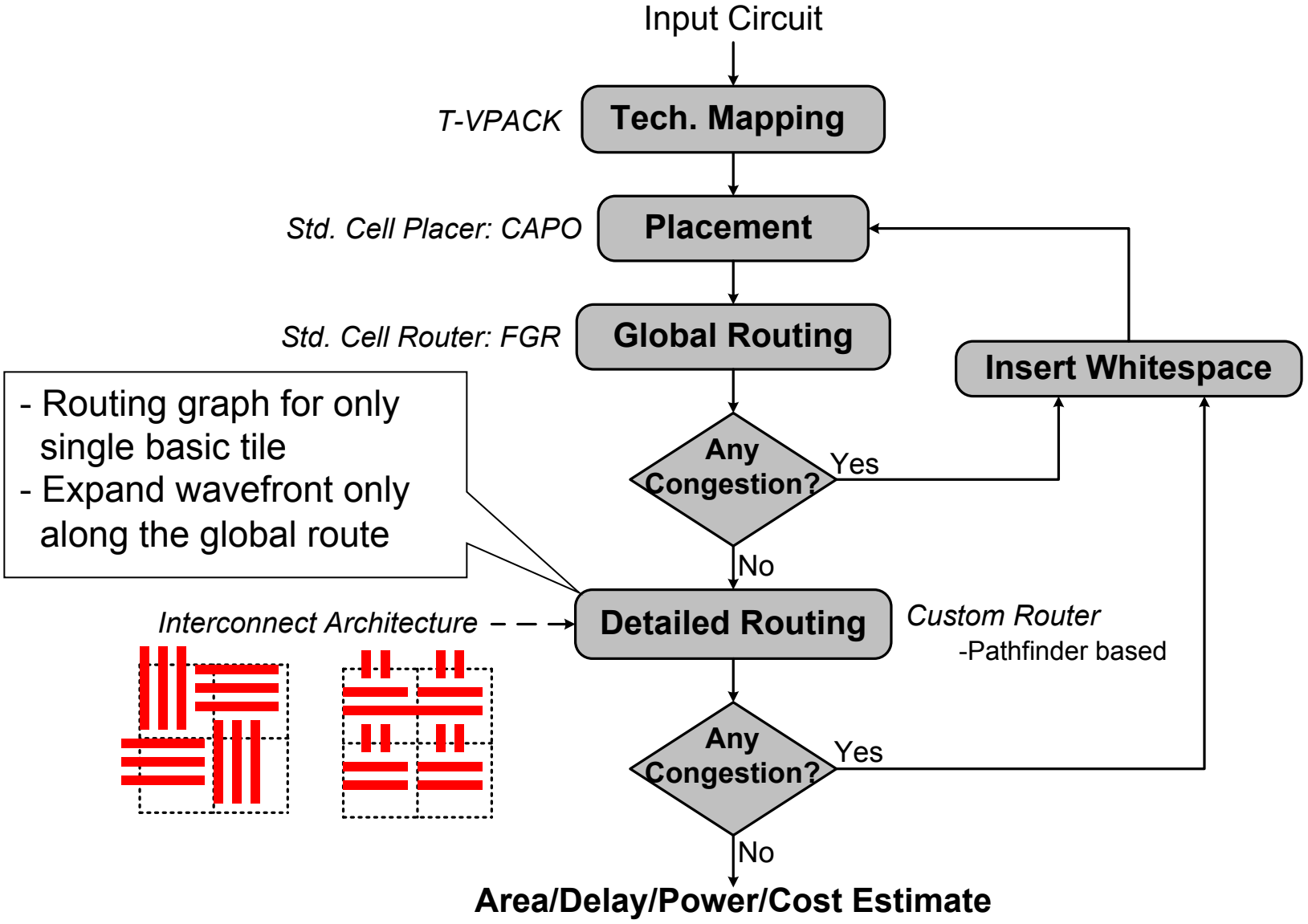
CAD Flow


Input Circuit
T-VPACK
Tech. Mapping
- Simulated annealing too slow
- Uniform whitespace distribution
- Logic cells snapped to grid
Std. Cell Placer: CAPO
Placement
Std. Cell Router: FGR
Global Routing
Insert Whitespace
Any Congestion?
Yes
No
Interconnect Architecture
Detailed Routing
Custom Router
-Pathfinder based
Any Congestion?
Yes
No
Area/Delay/Power/Cost Estimate

CAD Flow


Input Circuit
T-VPACK
Tech. Mapping
- Increase Placement Grid Size
Std. Cell Placer: CAPO
Placement
Std. Cell Router: FGR
Global Routing
Insert Whitespace
Any Congestion?
Yes
No
Interconnect Architecture
Detailed Routing
Custom Router
-Pathfinder based
Any Congestion?
Yes
No
Area/Delay/Power/Cost Estimate

CAD Flow

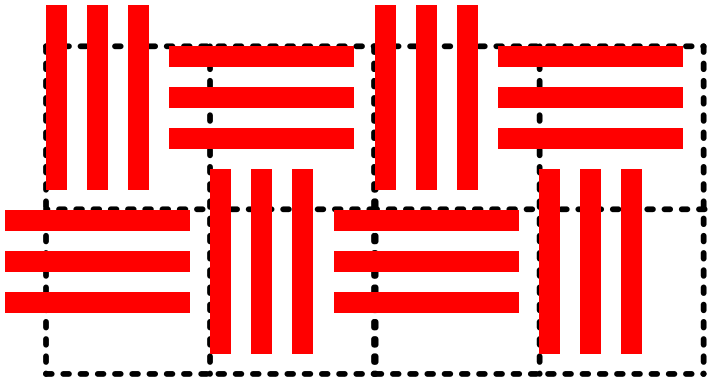

Input Circuit
T-VPACK
Tech. Mapping
Std. Cell Placer: CAPO
Placement
Std. Cell Router: FGR
Global Routing
Insert Whitespace
- Routing graph for only single basic tile
- Expand wavefront only along the global route
Any Congestion?
Yes
No
Interconnect Architecture
Detailed Routing
Custom Router
-Pathfinder based
Any Congestion?
Yes
No
Area/Delay/Power/Cost Estimate

Talk Outline

- Cost model
- Experimental methodology
  - Metrics
  - CAD flow
  - Architecture modeling
- Area, cost trends
- Conclusions

Routing Fabrics

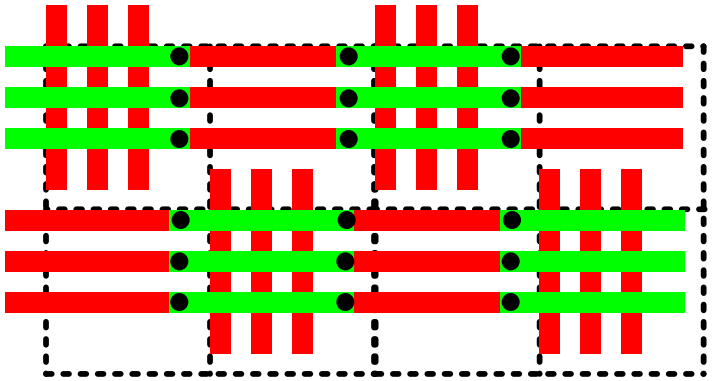
Crossover Fabric



All wires same length!

Routing Fabrics

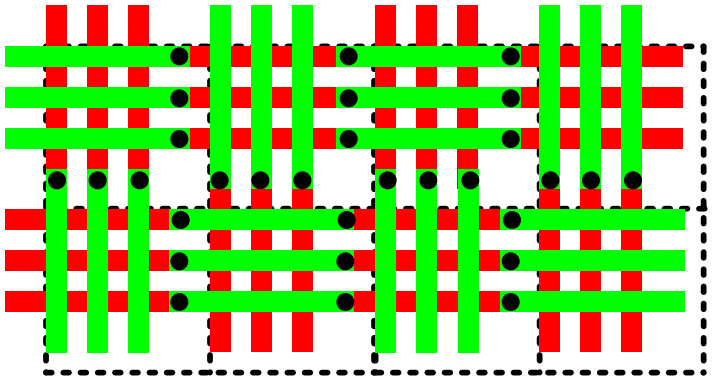
Crossover Fabric



All wires same length!

Routing Fabrics

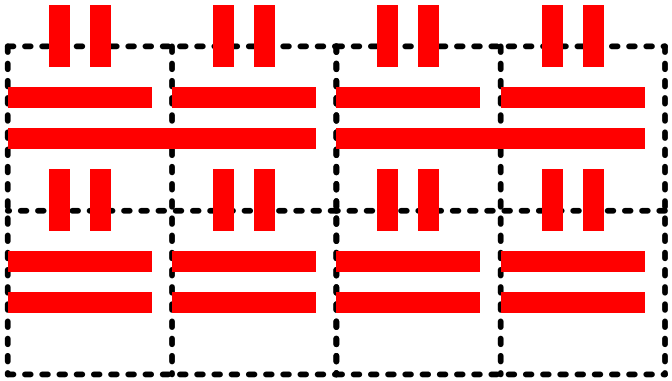
Crossover Fabric



All wires same length!

Routing Fabrics

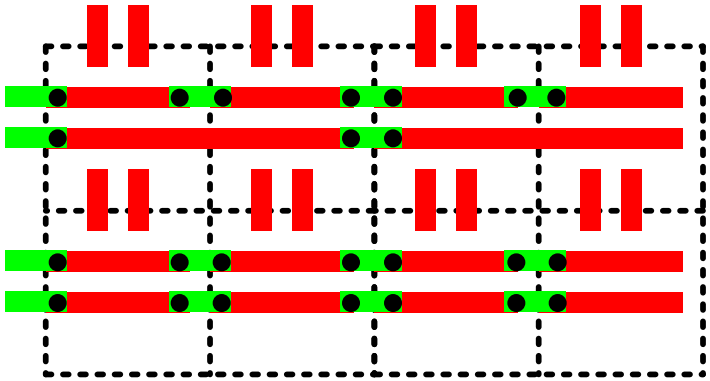
Jumper Fabric



Long wires OK!

Routing Fabrics

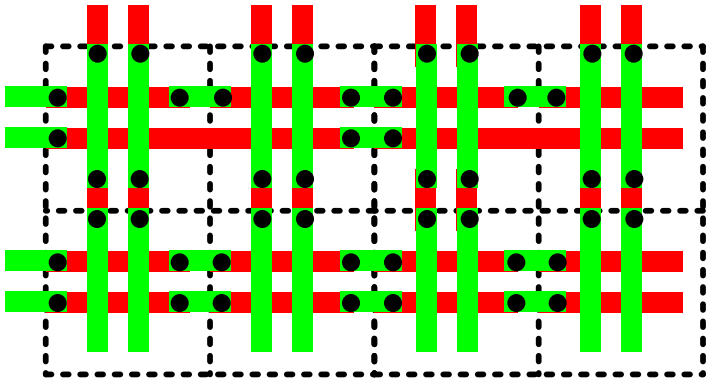
Jumper Fabric



Long wires OK!

Routing Fabrics

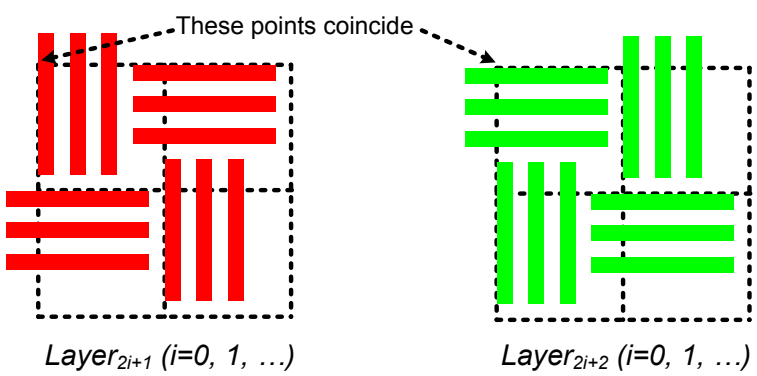
Jumper Fabric



Long wires OK!

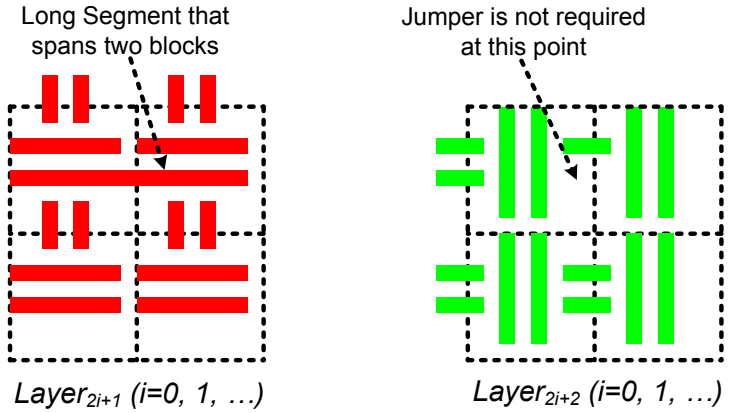
Routing Fabric Comparison

Crossover Fabric



- Single via to extend
- All wires same: length-1

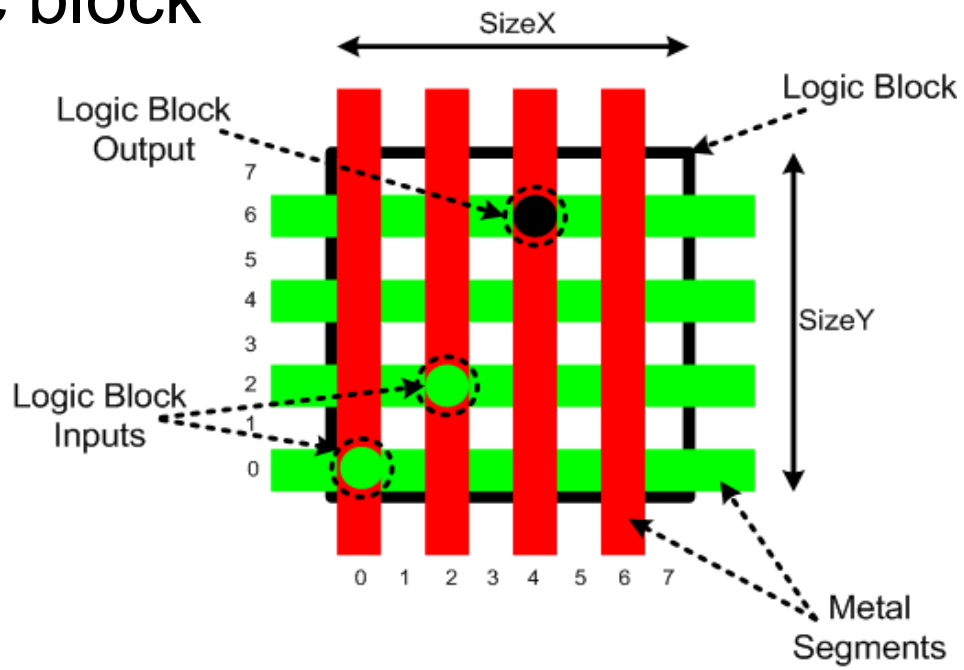
Jumper Fabric



- Two vias to extend
- Short segments: 1 blocks
- Long segments: 4 blocks, staggered
- Two variants
  - Jumper20: 20% Long segments
  - Jumper40: 40% Long segments

Logic Block Model

- Characteristics of logic block
  - Physical dimensions (in wire pitches)
  - Pin locations
- Do not need low-level layout details



Parameterize Logic Block

- Cover wide search space for logic blocks
- Vary layout density
  - **Dense**: Determined by # pins (small layout area)
  - **Sparse**: Determined by Standard Cell implementation
- Vary logic capacity
  - Sweep number of inputs and outputs
    - 2-input, 1-output logic blocks (shown here)
    - 16-input, 8-output logic blocks (also in paper)
  - Use logic clustering (T-VPack) as tech-mapper

Talk Outline

- Cost model
- Experimental methodology
  - Metrics
  - CAD flow
  - Architecture modeling
- Area, cost trends
- Conclusions

Area, Cost Trends

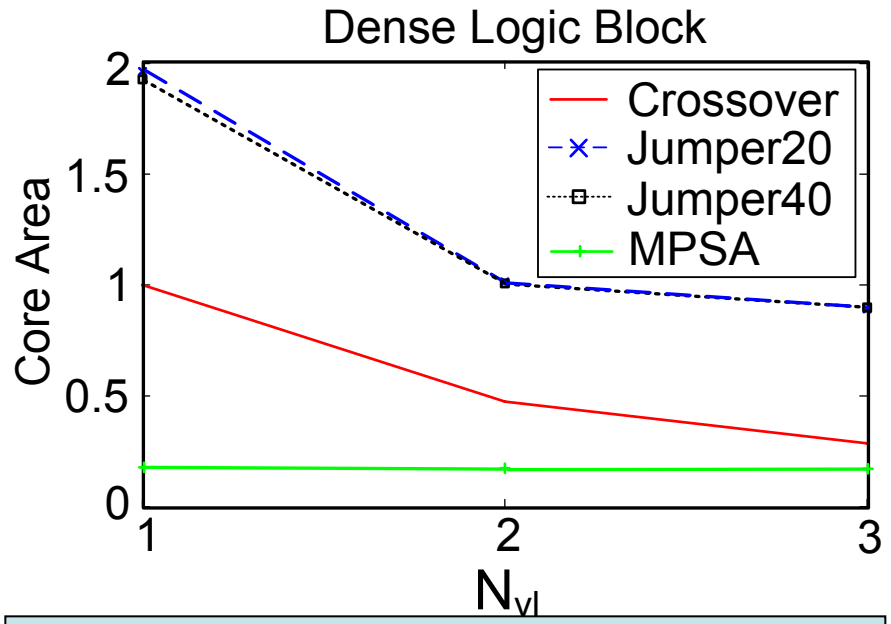
- Experimental results
  - MCNC benchmarks
    - Geometric mean over 19 large circuits
  - Logic block density
    - Dense, medium, and sparse
  - Logic block capacity
    - From 2-input, 1-output to 16-input, 8-outputs
    - Only 2-input, 1-output results shown here

Area and Die-Cost Trends

Area

Cost

Area and Die-Cost Trends



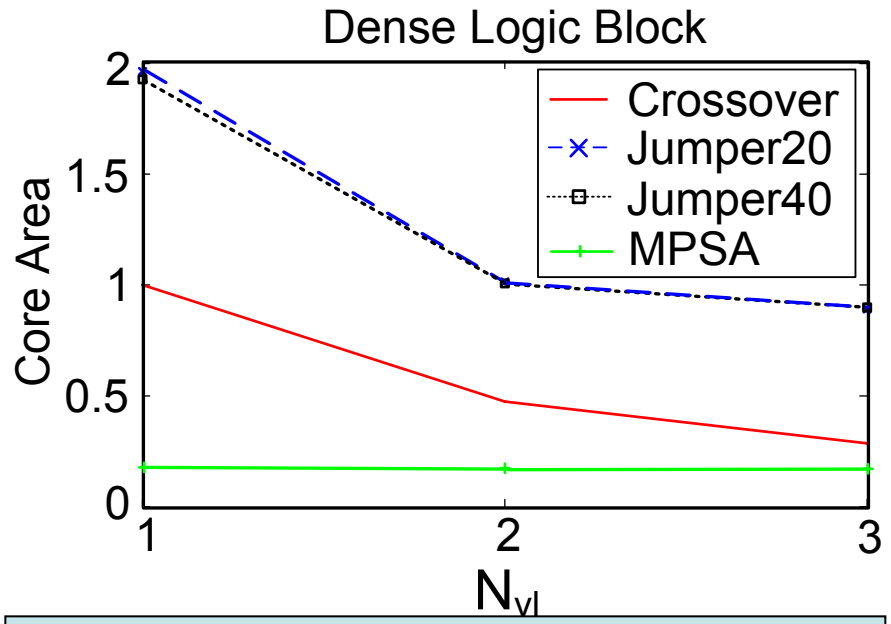
Area

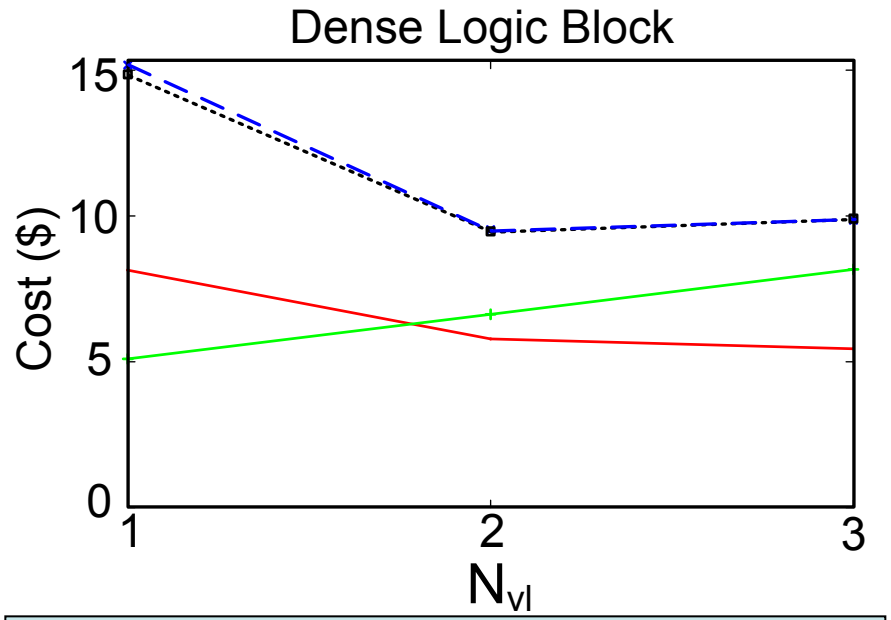
MPSA < Crossover < Jumper

N_{vl} = 1 more area,
needs whitespace to route

Cost

Area and Die-Cost Trends





Area

MPSA < Crossover < Jumper

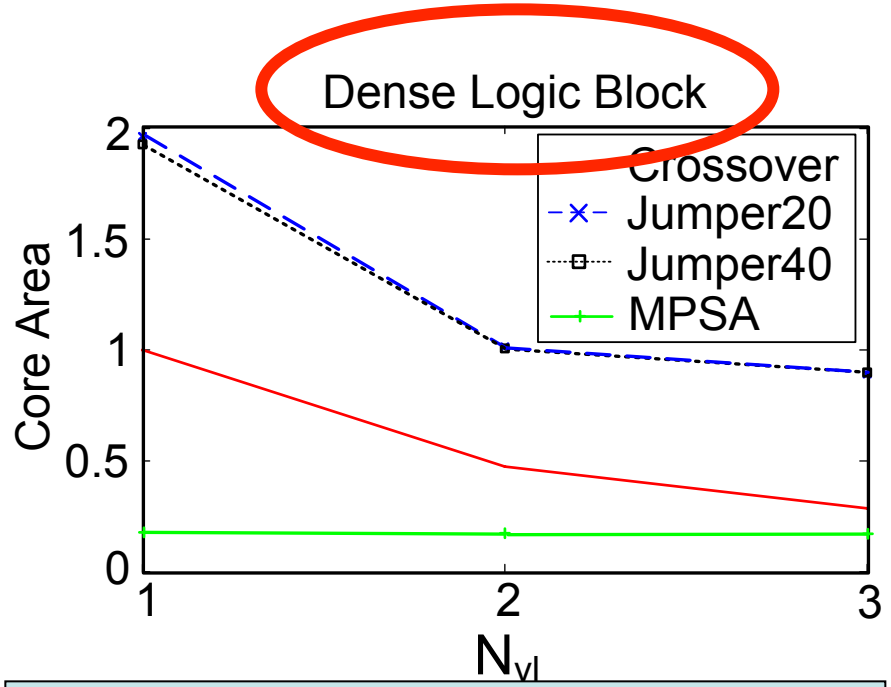
N_{vl} = 1 more area, needs whitespace to route

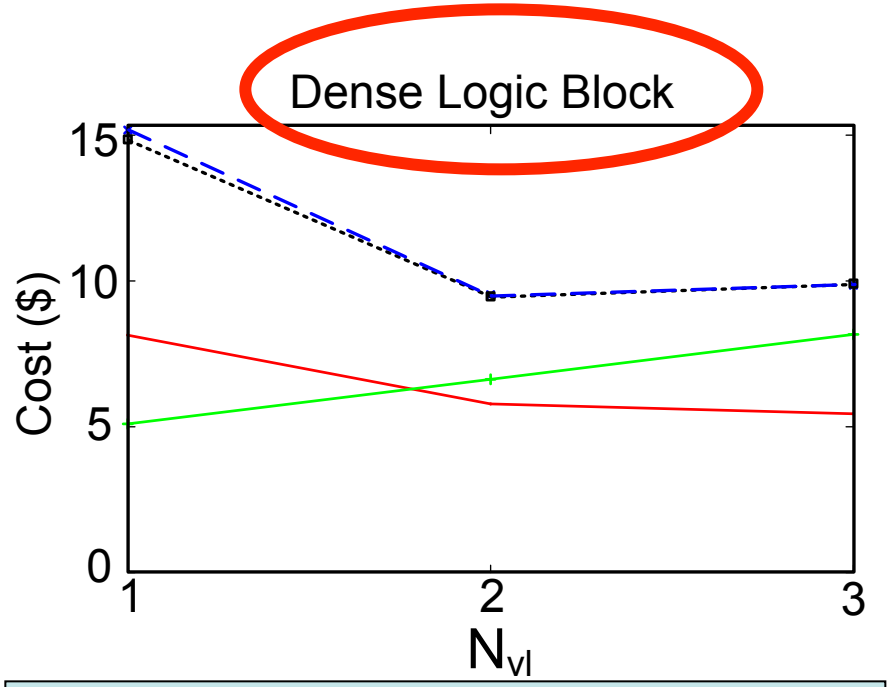
Cost

MPSAs: more layers → higher cost

VPSAs: more layers → lower cost

Area and Die-Cost Trends





Area

MPSA < Crossover < Jumper

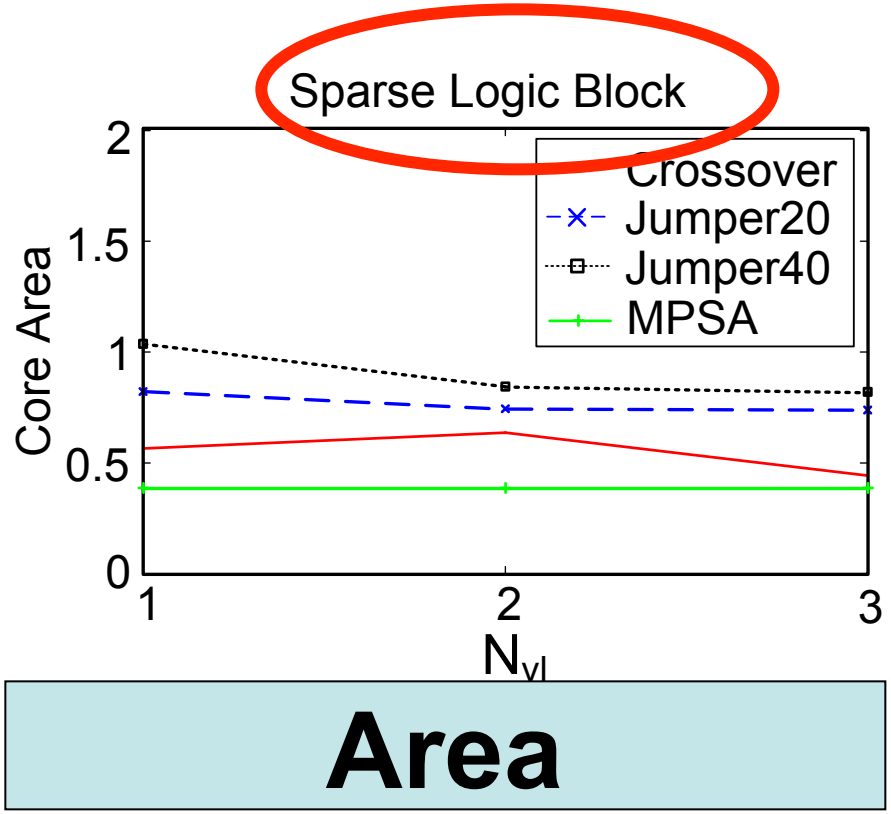
N_{vl} = 1 more area, needs whitespace to route

Cost

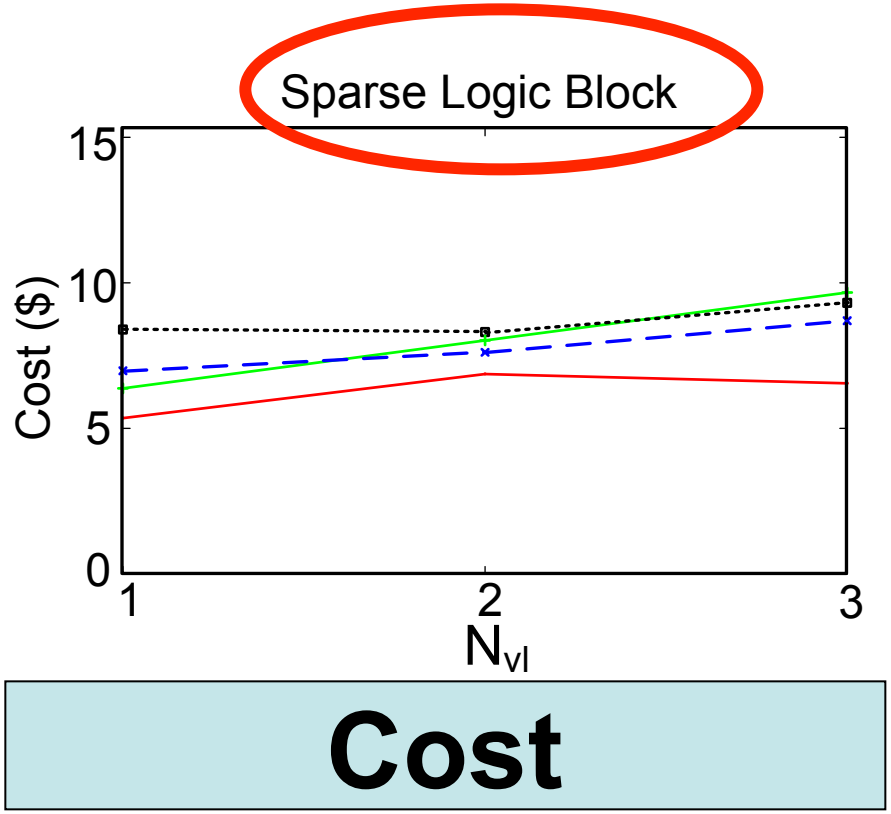
MPSAs: more layers → higher cost

VPSAs: more layers → lower cost

Area and Die-Cost Trends



Area



Cost

- Sparse layout is better! ???
  - Less whitespace needed
- Need to study whitespace allocation

Delay and Power Trends

Key results (in paper):

MPSA is significantly better than VPSA

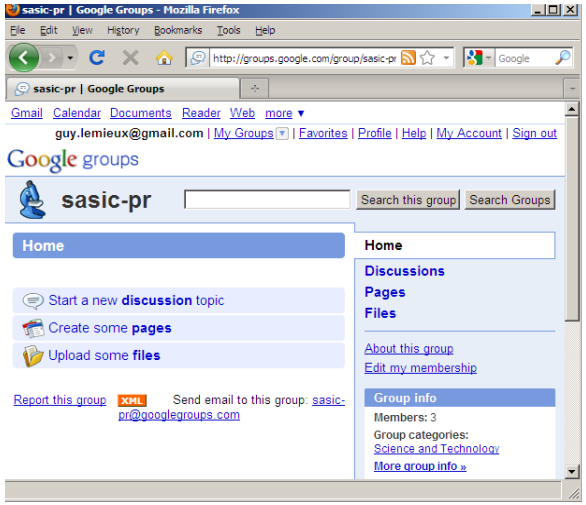
Talk Outline

- Cost model
- Experimental methodology
  - Metrics
  - CAD flow
  - Architecture modeling
- Area, cost trends
- Conclusions

Conclusions

- Trends for VPSAs
  - Die-cost more important than die-area
  - MPSAs better in Area, Delay, and Power
  - VPSAs better in Cost
  - Interconnect Matters
    - Performance varies with different routing fabrics
    - Even significant variation among VPSA structures
- Ongoing research
  - Interconnect architectures
  - Whitespace insertion algorithm

Limitations



- CAD framework available online

  http://groups.google.com/group/sasic-pr

- This is early work … need improvements!
  - Whitespace insertion
  - Buffer insertion

  - Delay/Power of logic blocks
  - Power/clock network area overhead
  - SRAM-configurable logic blocks

Key Message

1. Structured ASICs
will be the key technology
of the future.

Because the **key issues** that
make structured ASICs attractive
have **not been solved**.

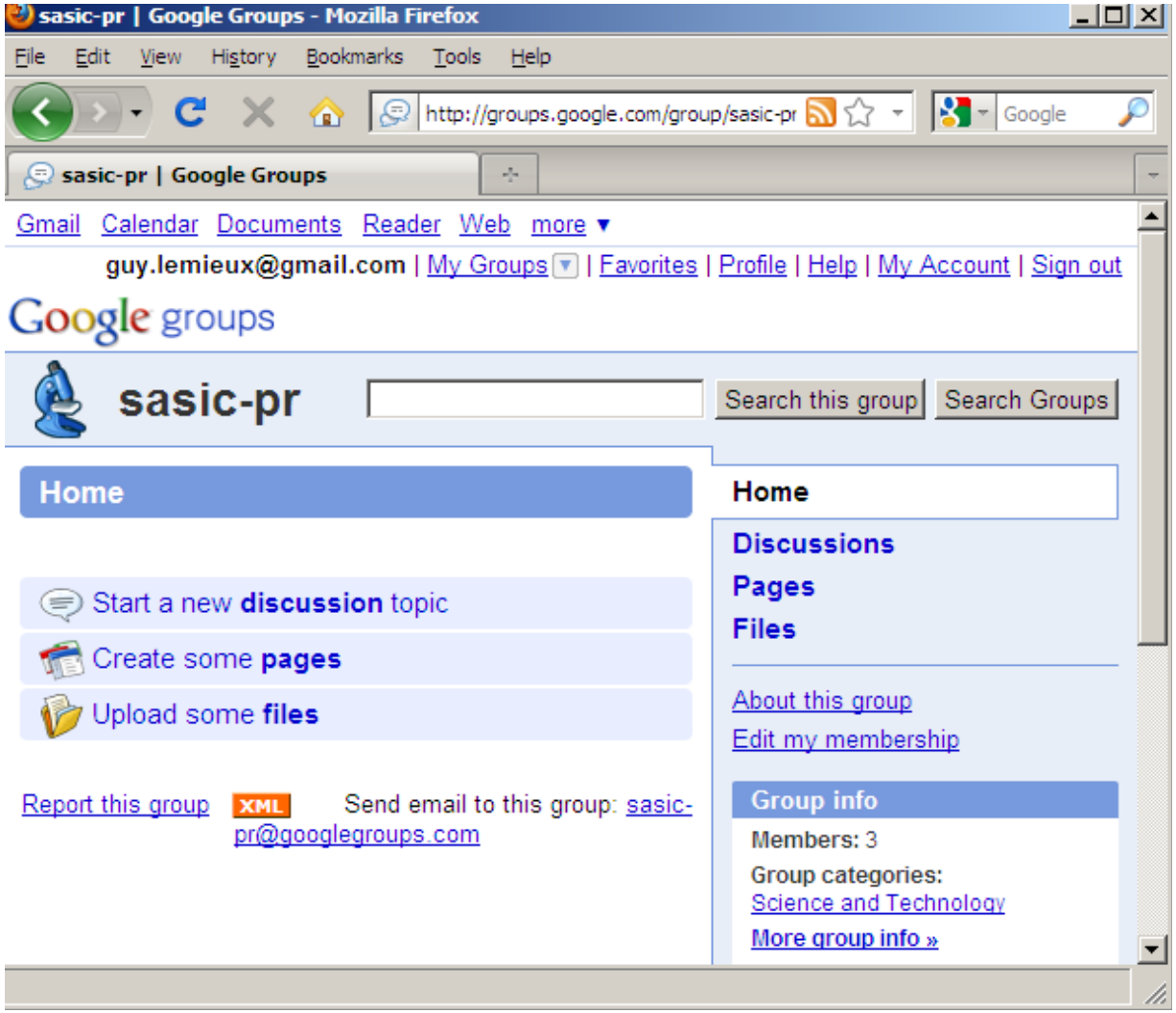
They are growing **more prominent**.

2. Interconnect matters.

MPSAs have better performance,

VPSAs are cheaper.

CAD Framework Available



Power and Delay Trends

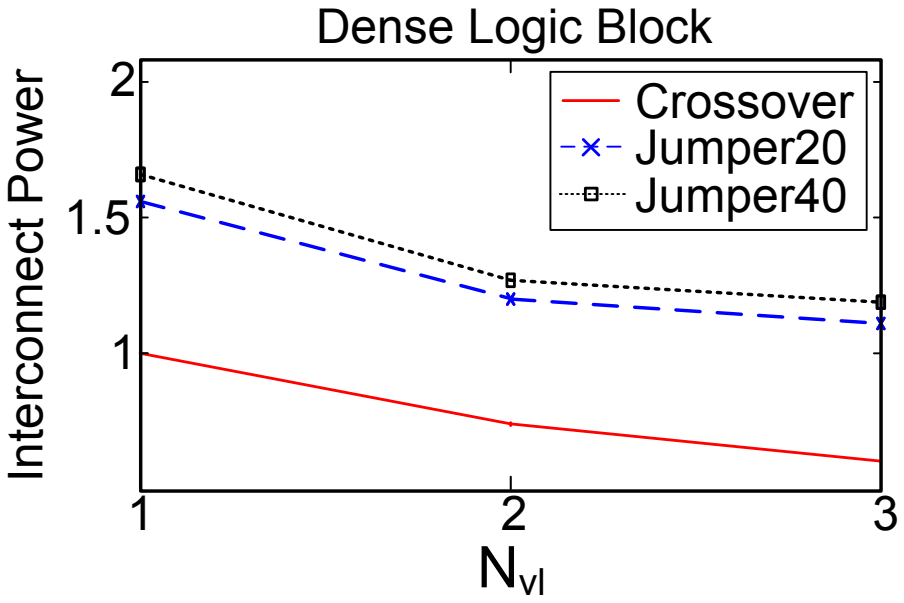
Metrics

- Area
  - Determined from placement grid size
- Delay
  - Average net delay (Elmore model)
    - Register locations unknown; critical path delay calculation is difficult
    - CAD flow is not timing driven
- Power
  - Total metal + via capacitance

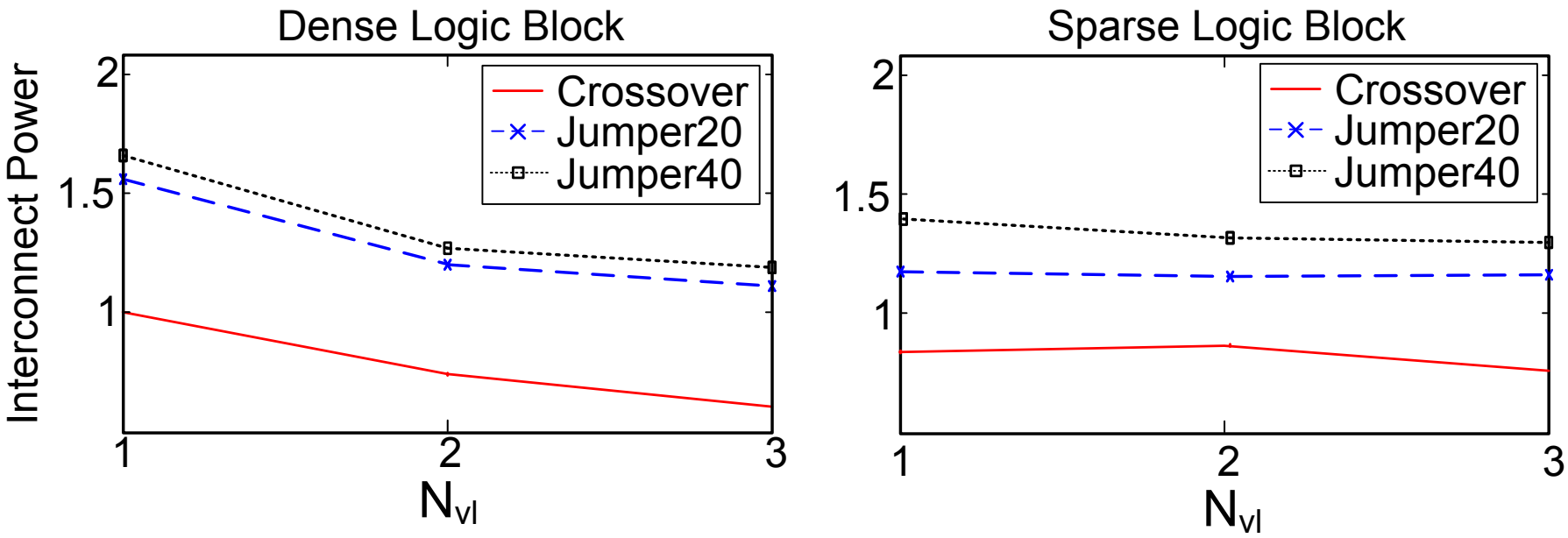
Talk Outline

- Cost model
- Experimental methodology
  - Metrics
  - CAD flow
  - Architecture modeling
- Area, delay, power, cost trends
- Cost model sensitivity
- Conclusions

Power Trends

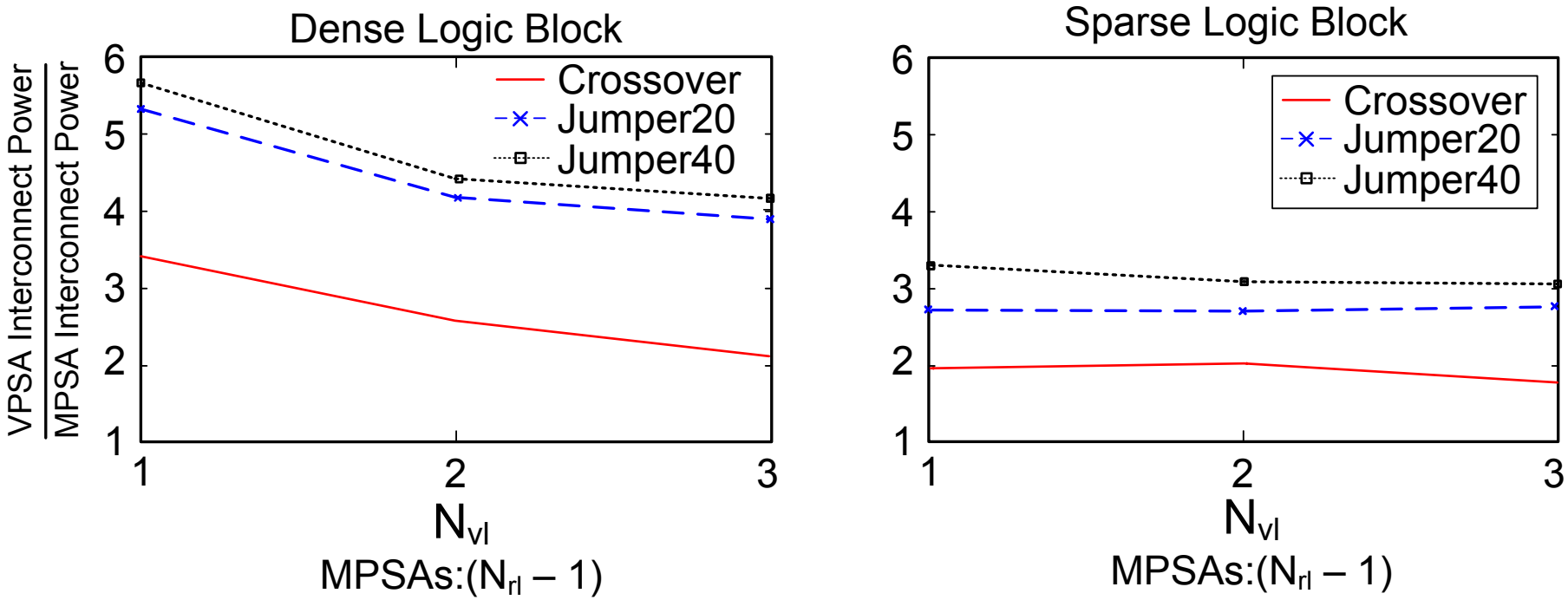


Power Trends



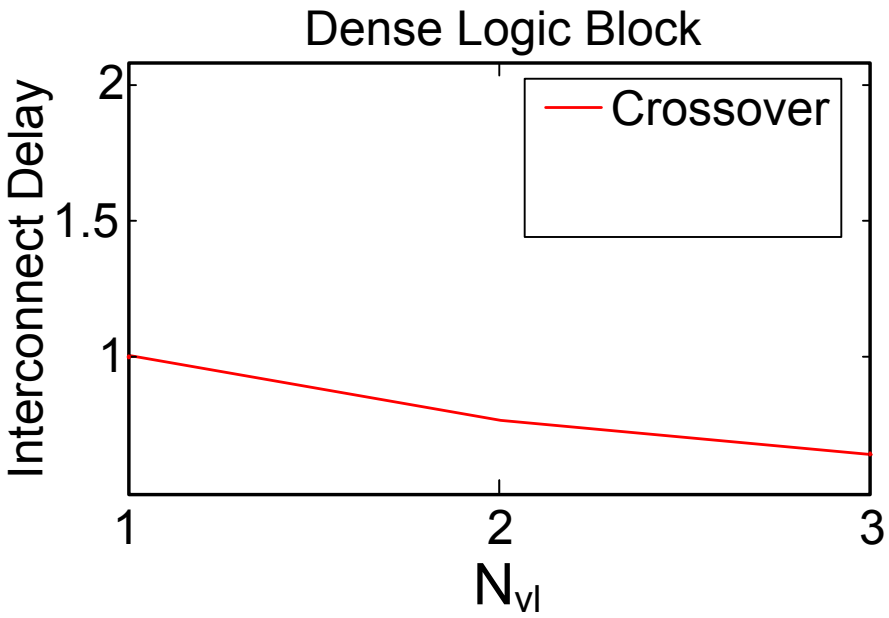
- Significant range for different routing fabrics
- More custom via layers → Lower Power
  - Especially for dense layouts

Power Trends

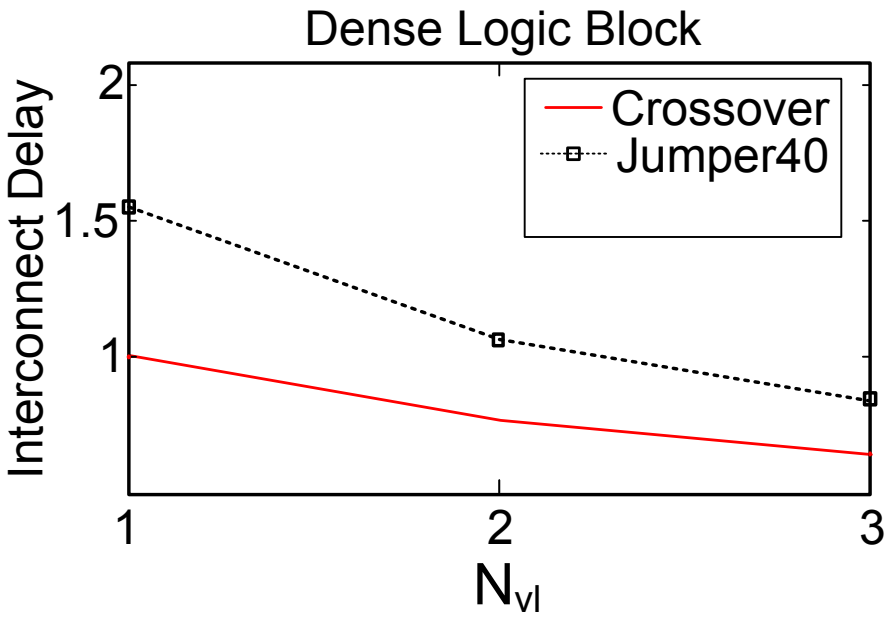


- **Re-Normalized to MPSAs**
- VPSAs use more power
  - 2x (sparse) to 6x (dense) more than MPSAs

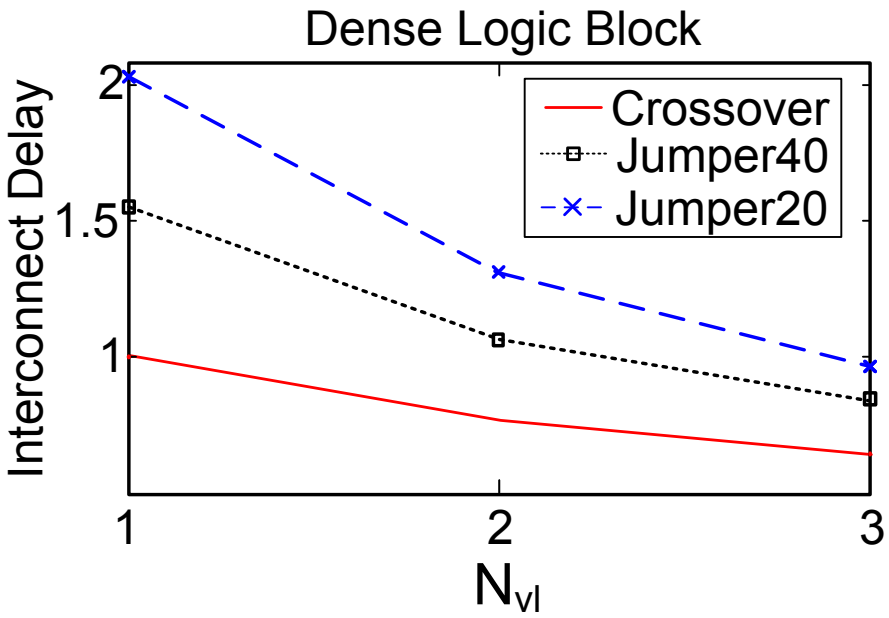
Delay Trends



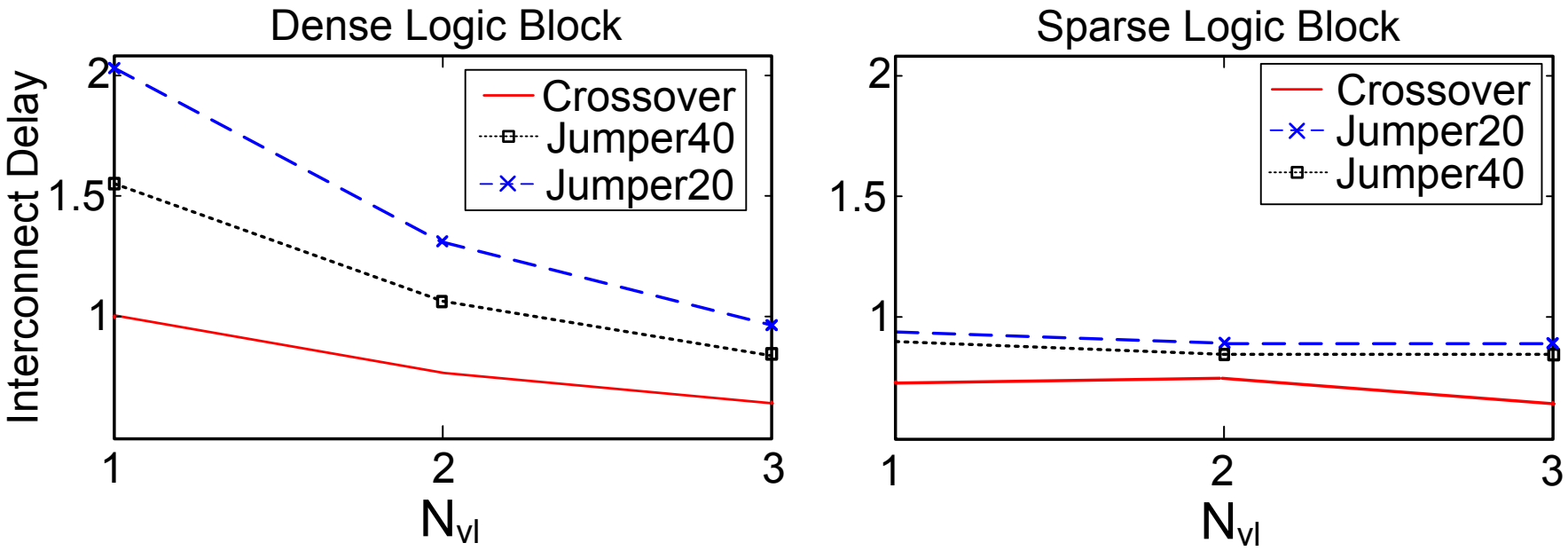
Delay Trends



Delay Trends



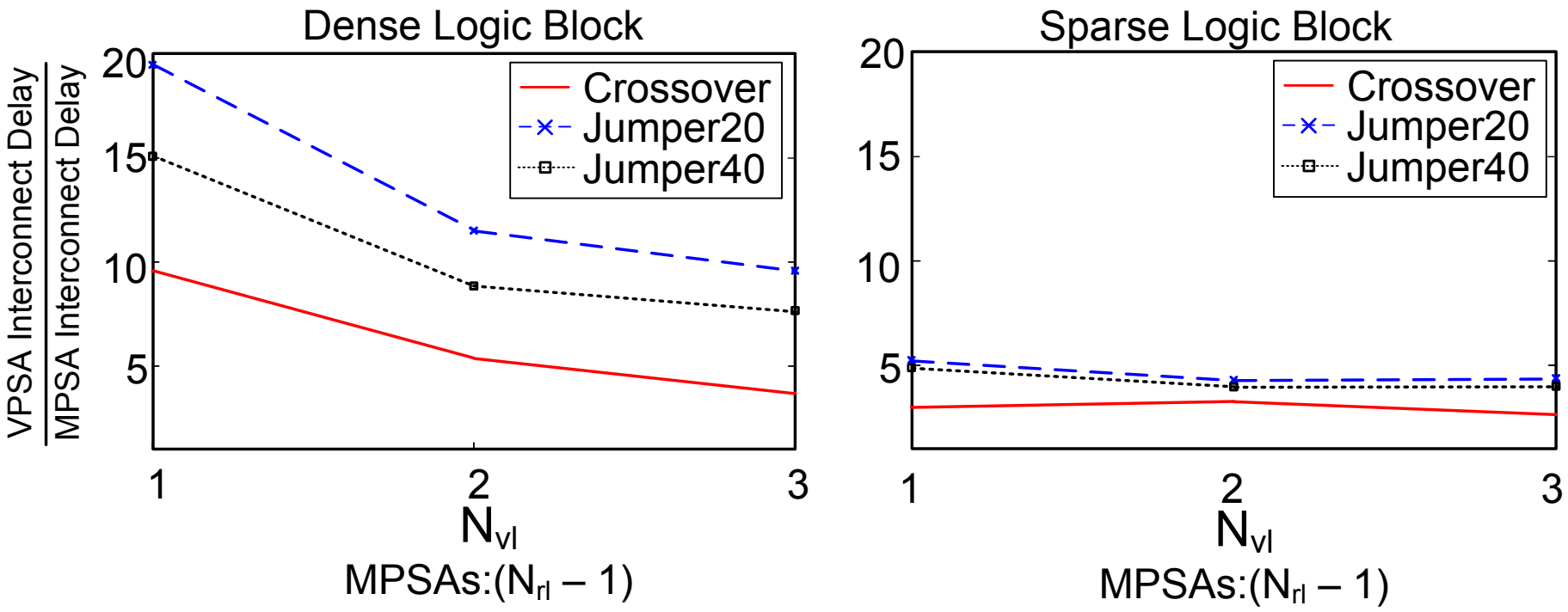
Delay Trends



- Significant range for different fabrics
  - Delay improves with more custom via layers

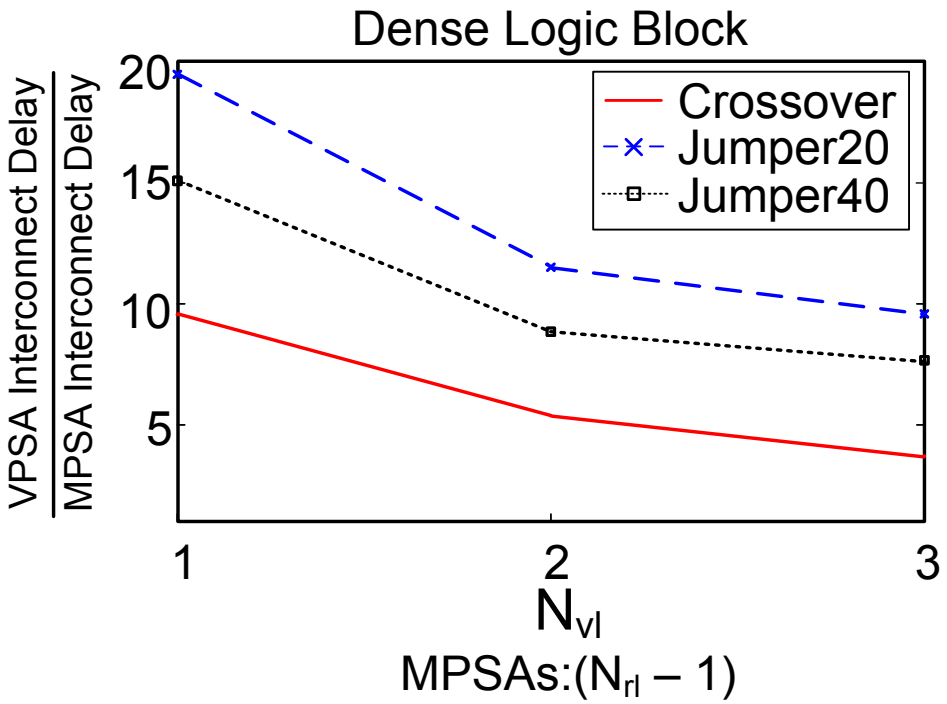
- Jumper Fabric: Long segments improve delay (but higher power)

Delay Trends



- **Re-Normalized to MPSAs**
- VPSA delay up to 20x worse

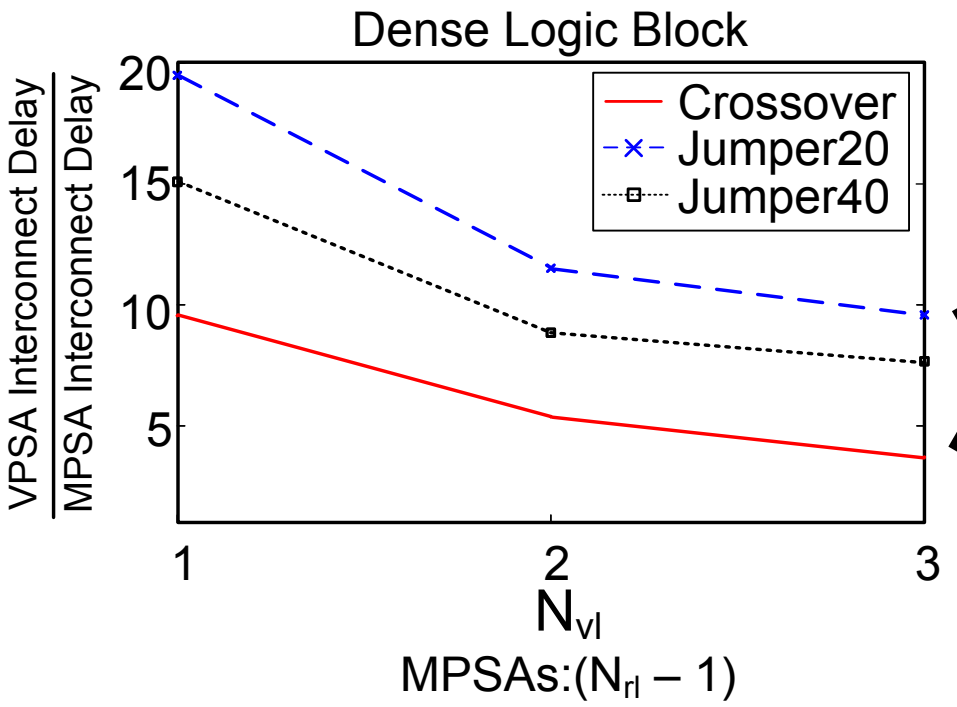
Delay Trends



Why is VPSA delay worse than MPSA delay?

- **Re-Normalized to MPSAs**
- VPSA delay up to 20x worse

Delay Trends

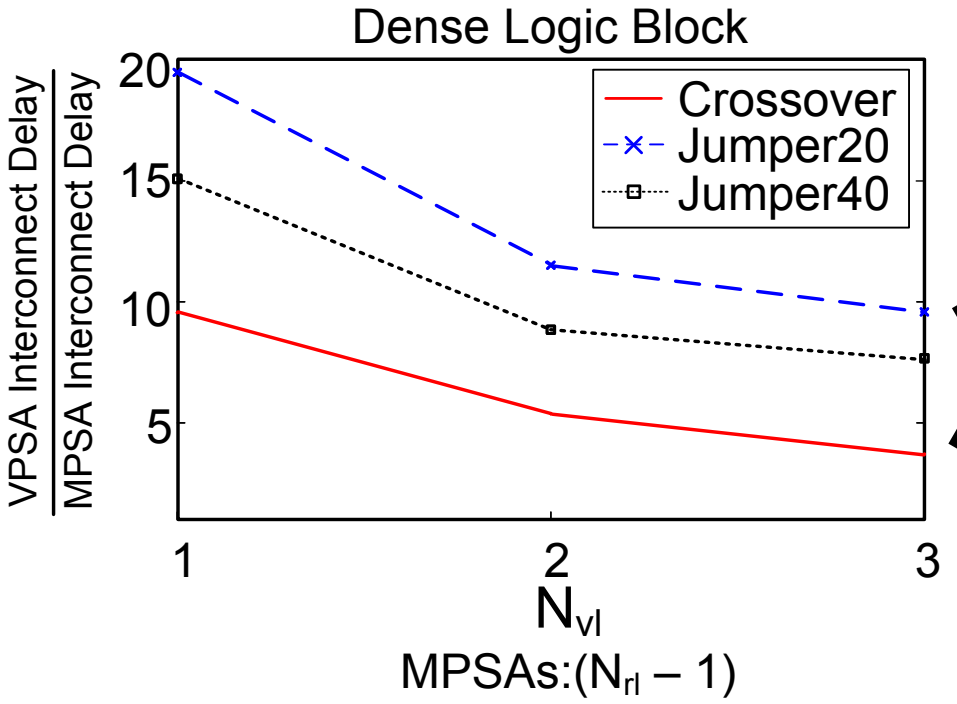


- **Re-Normalized to MPSAs**
- VPSA delay up to 20x worse

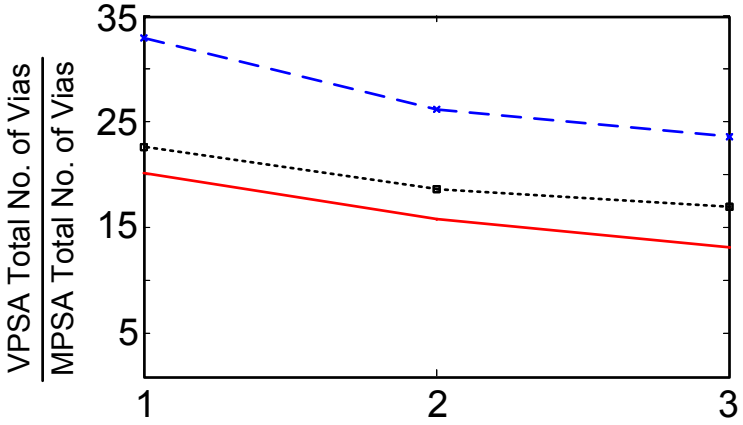
more vias

more wirelength

Delay Tre



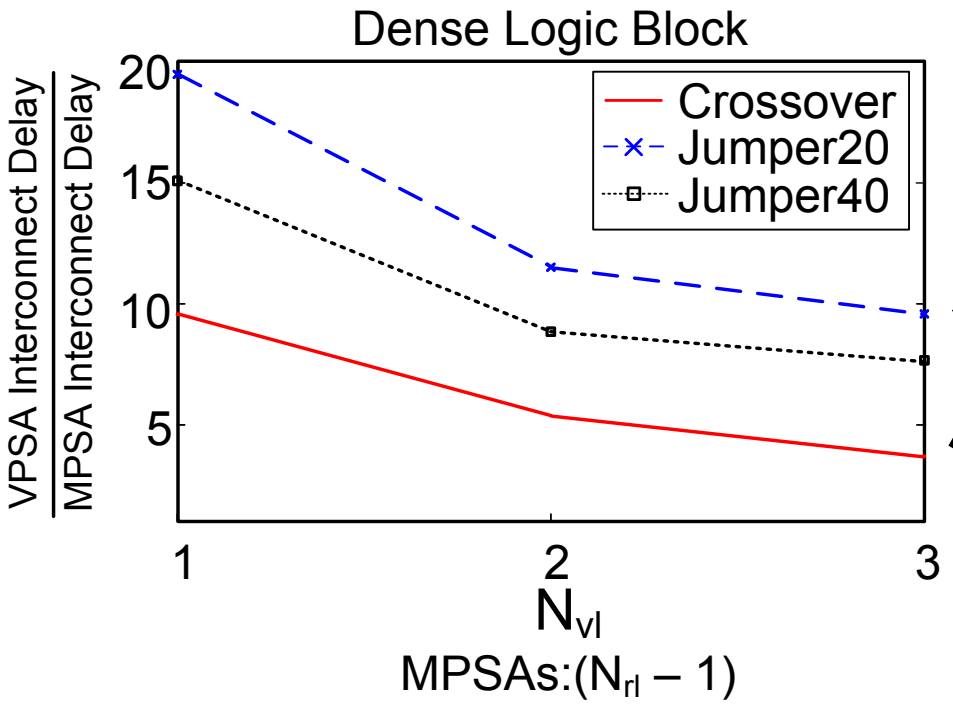
more vias



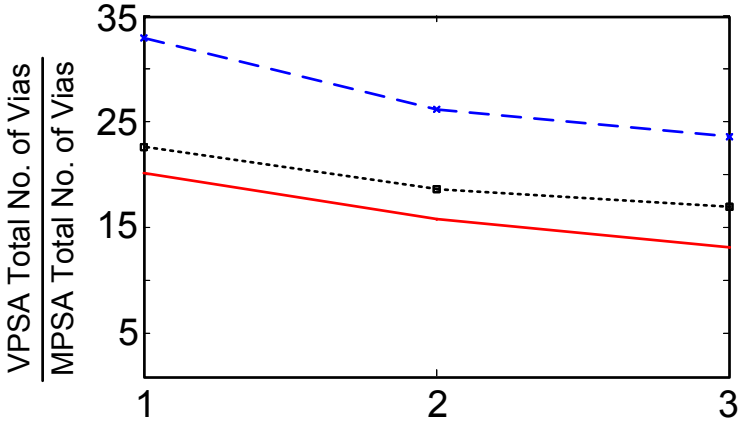
more wirelength

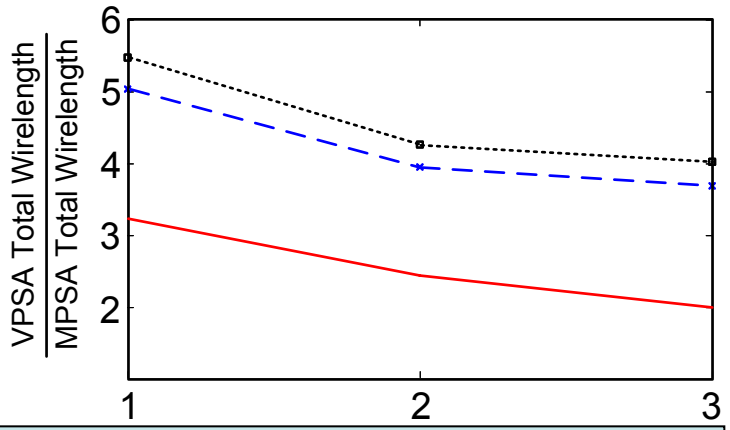
- **Re-Normalized to MPSAs**
- VPSA delay up to 20x worse

Delay Tre



more vias





more wirelength

- **Re-Normalized to MPSAs**
- VPSA delay up to 20x worse

Cost Model Sensitivity

Talk Outline

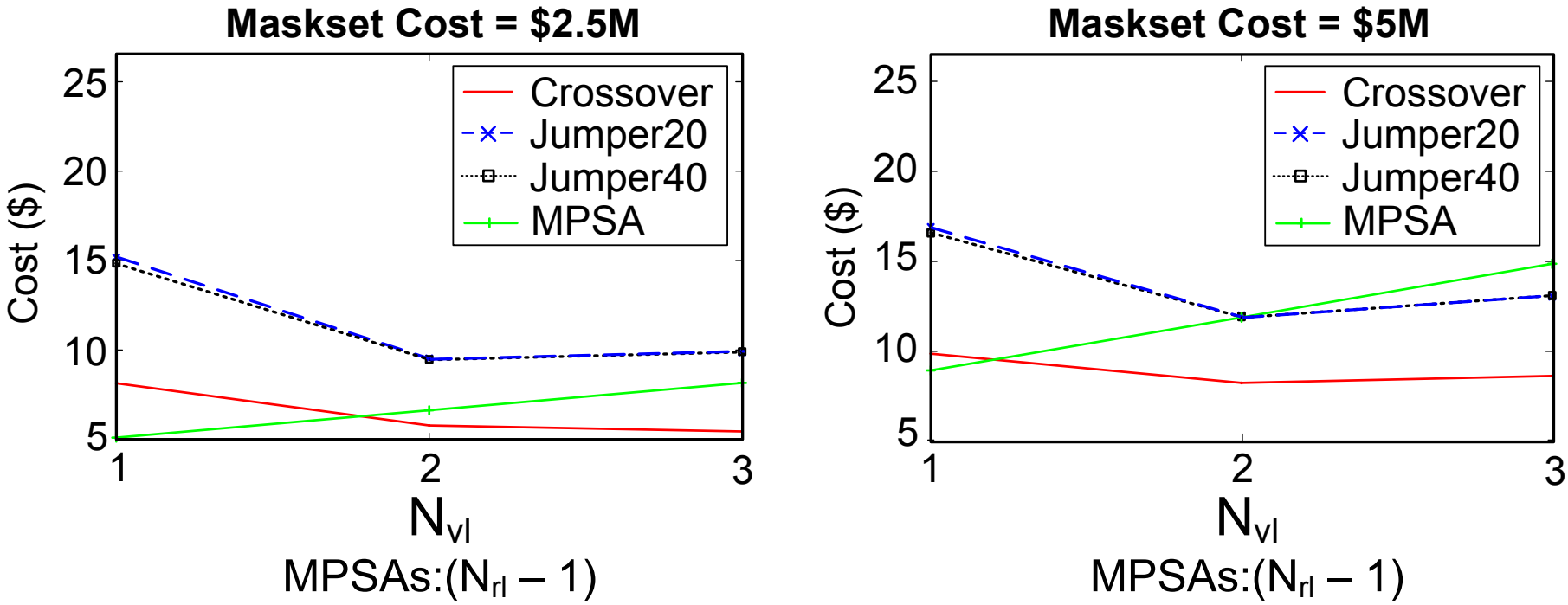
- Cost model
- Experimental methodology
  - Metrics
  - CAD flow
  - Architecture modeling
- Area, delay, power, cost trends
- Cost model sensitivity
- Conclusions

Cost Model Sensitivity

- How sensitive is the die-cost to various factors?
- Primary factors
  - Die area
  - Number of customizable layers
- Secondary factors
  - Maskset cost
  - Volume requirements
  - Number of fixed lower masks

Cost Model Sensitivity

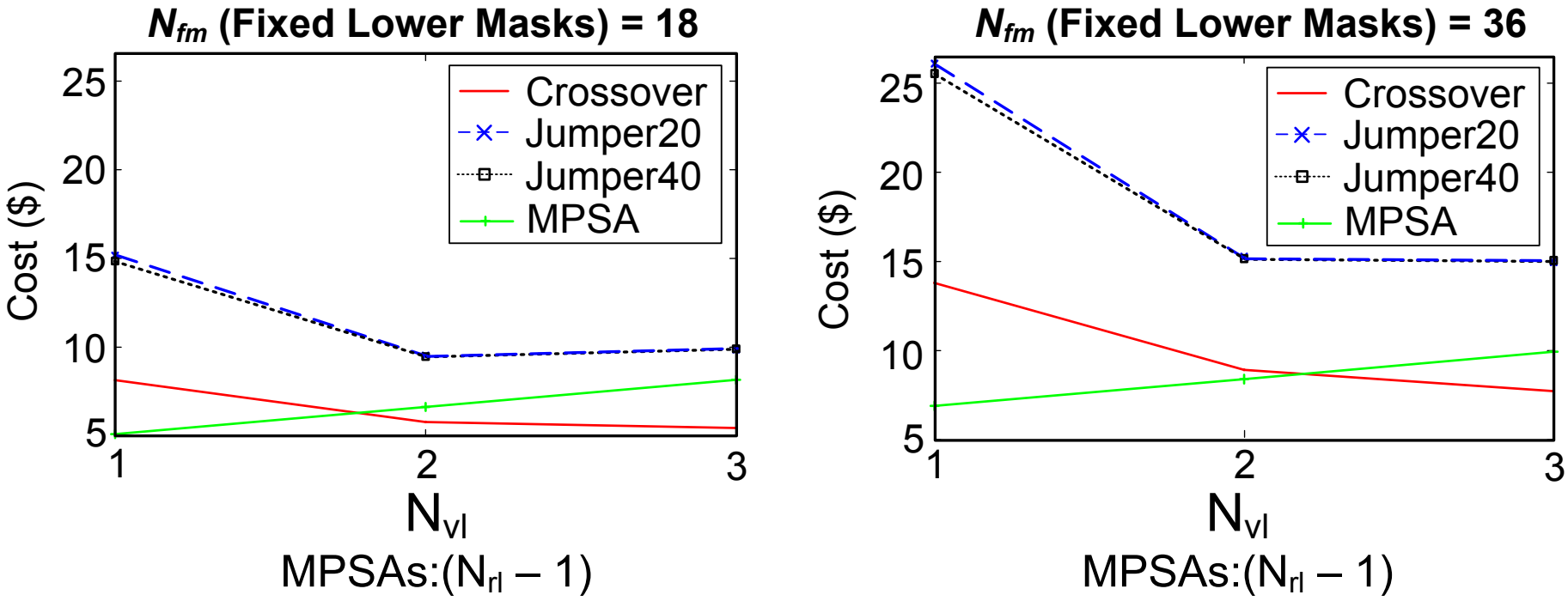
– Sensitivity to Maskset Cost



- VPSAs less sensitive to maskset cost

Cost Model Sensitivity

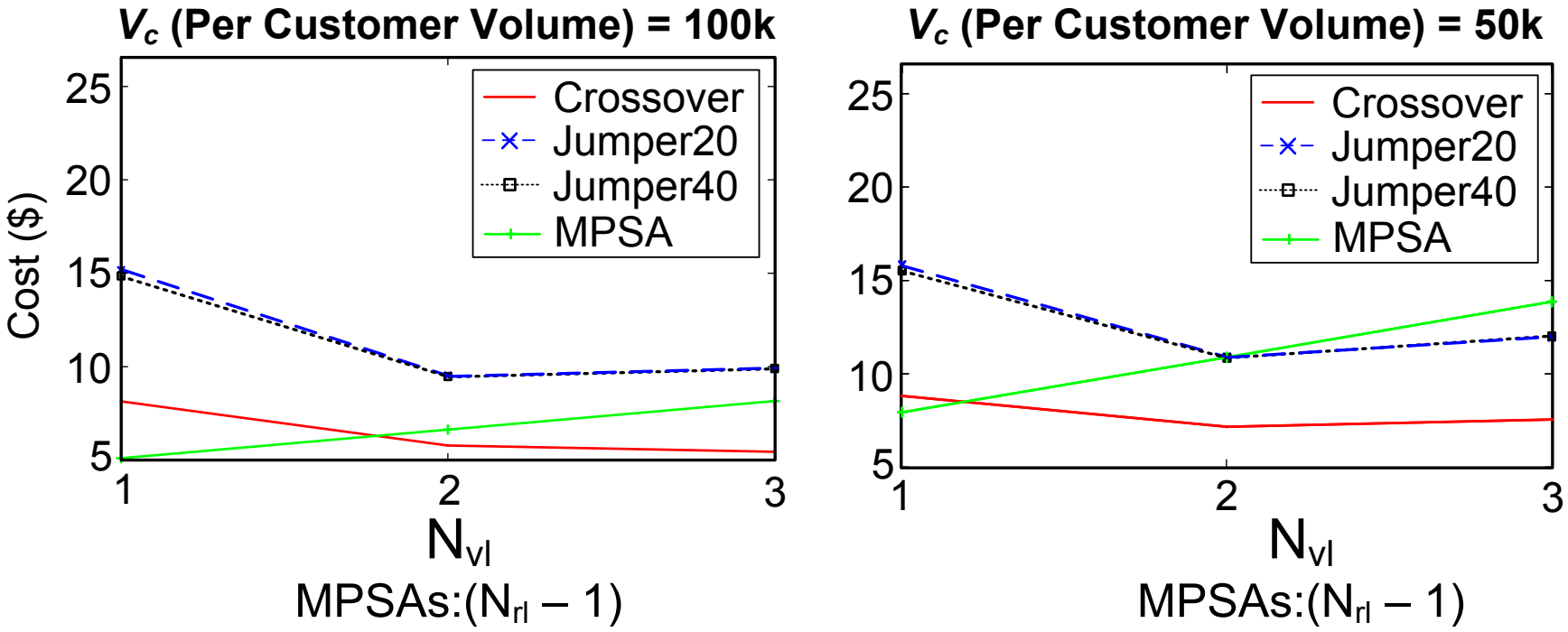
– Sensitivity to Number of Fixed Lower Masks (N_{fm_l})



- VPSA cost increases more rapidly than MPSAs
  - Large area of VPSAs

Cost Model Sensitivity

– Sensitivity to Per Customer Volume (V_c)



- VPSAs less sensitive to customer volume than MPSAs