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Foreword

Programmable Logic Devices (PLDs) have become the key implementation medium for the vast majority of digital circuits designed today. While the highest-volume devices are still built with full-fabrication rather than field-programmability, the trend towards ever fewer ASICs and more FPGAs is clear. This makes the field of PLD architecture ever more important, as there is stronger demand for faster, smaller, cheaper and lower-power programmable logic.

PLDs are 90% routing and 10% logic. This book focuses on that 90% that is the programmable routing: the manner in which the programmable wires are connected and the circuit design of the programmable switches themselves. Anyone seeking to understand the design of an FPGA needs to become literate in the complexities of programmable routing architecture. This book builds on the state-of-the-art of programmable interconnect by providing new methods of investigating and measuring interconnect structures, as well as new programmable switch basic circuits.

The early portion of this book provides an excellent survey of interconnection structures and circuits as they exist today. Lemieux and Lewis then provide a new way to design sparse crossbars as they are used in PLDs, and show that the method works with an empirical validation. This is one of a few routing architecture works that employ analytical methods to deal with the routing architecture design. The analysis permits interesting insights not typically possible with the standard empirical approach.

The authors show how the sparse crossbar can be effectively used as the interconnect network within a clustered logic block in an FPGA. They give some very surprising results of their effect on the choice of the logic function in the logic block.

An exciting portion of this book marries the issue of programmable switch circuit design with the design of the routing architecture. The authors suggest some new and important circuits and show that they are more effective than

current designs. They give a clever method of replacing expensive buffers with cheaper alternatives that also reduce overall critical path delay in FPGAs.

To achieve all of this, the book also makes important contributions to the software (an enhanced router) and modeling (of area and delay) used in the empirical FPGA architecture development approach.

This book is a must-read for the aspiring FPGA architect, or for anyone who would like to gain a good comprehension of the most important IC technology of our time.

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