Altium II

(PCB Layout)

ELEC391 – WT2 2015

PCB Design support for ELEC391:

Altium 2014, 150 licenses

Lecture talks:

- Jan 22 Altium I (Circuit Design + Simulation)
- Feb 1 Altium II (PCB Layout)
- TBA Guest Lecture – PCB Production
- Support & submission instructions posted here

Mechanical and PCB design support available 2hrs per lab session MCLD315,306

Mon: 16:00-18:00
Tue : 09:00-11:00 / 14:00-16:00 / 16:00-18:00
Wed: 09:00-11:00 / 16:00-18:00
Thu : 09:00-11:00 / 14:00-16:00 / 16:00-18:00
Fri : 09:00-11:00

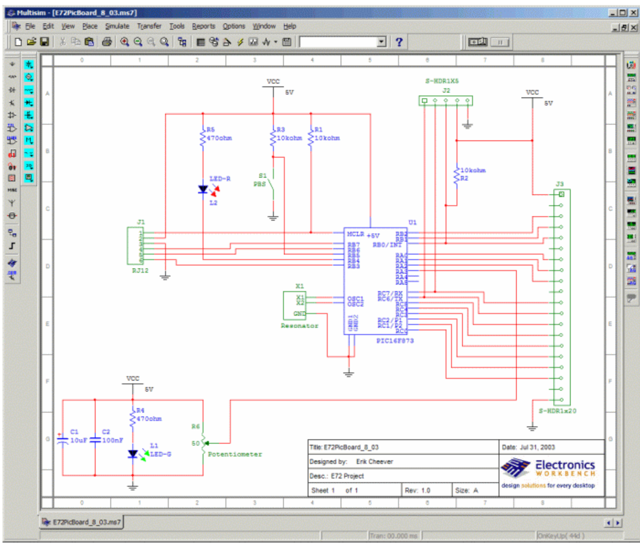
Contents

- Walk-through Tutorial, simple PCB
  - Altium tips
  - Advanced example
- Instructions for elec391 design submissions
- Anatomy of a PCB
  - Traces, pads, vias, layers etc.
- PCB Design Best practices

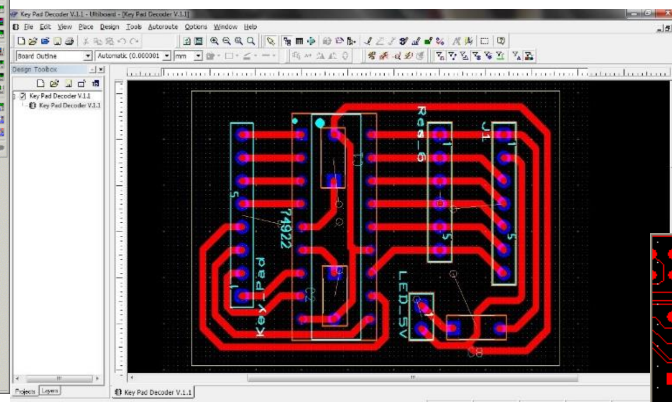
PCB Basic Design Flow

- Gerber: 274X
  - Top, Bottom Cu
  - Top, Bottom Solder
  - Silkscreen
  - Mechanical 1
- Drill files (tool list)

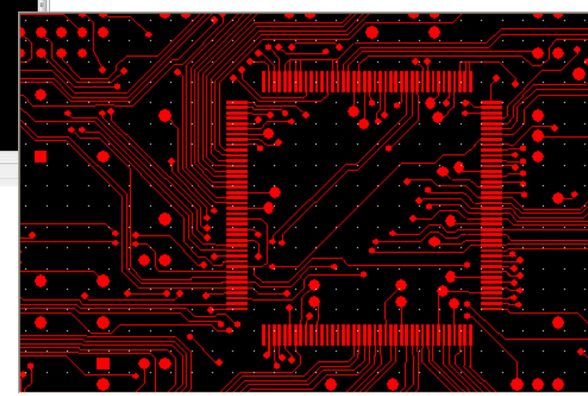
Schematic entry



PCB Layout



CAM files



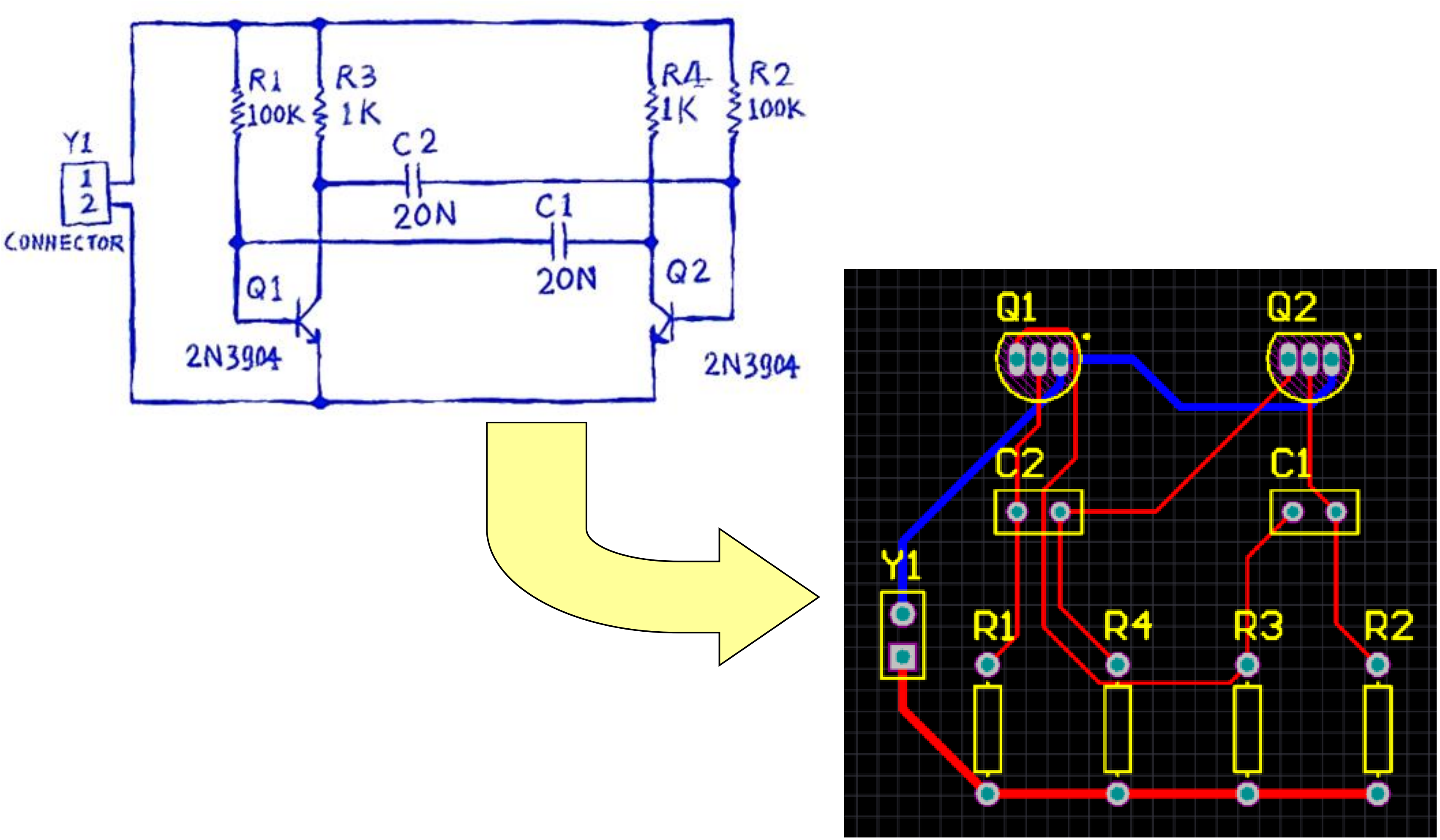
- Symbol and Footprint creation
- Auto place
- Auto route …

2 starting points for PCB design

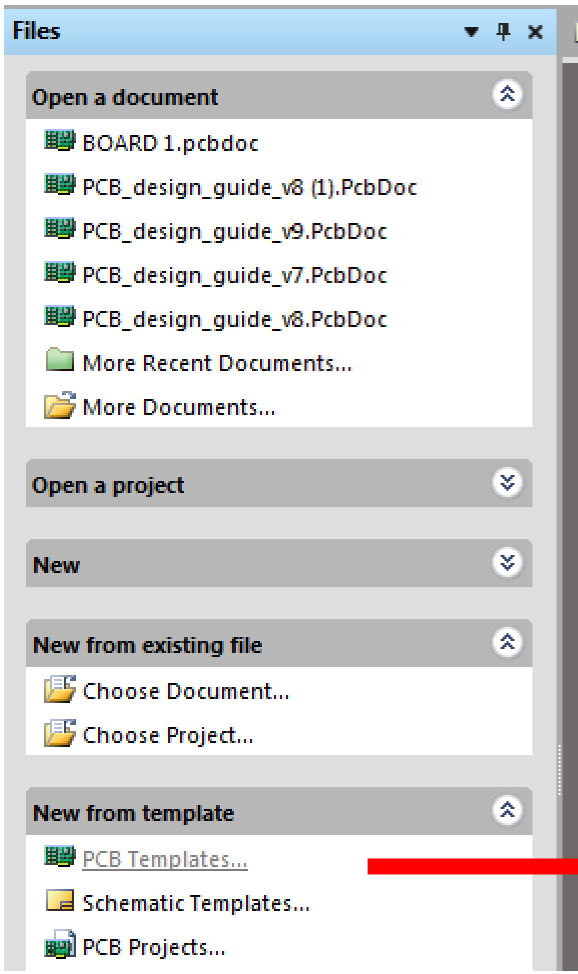
1. <u>From a companion schematic package</u>
   - Prepare project schematics
   - Import schematic design
   - Component footprints are added automatically
   - Connectivity is indicated with rats nests
   - Net names are imported from the schematic
2. Directly from the PCB editor
   - You need to select and place manually each component footprint from a library
   - No rats nest – connectivity
   - You must assign nets manually (at least GND)

Board Implementation
Tutorial - Getting Started with PCB Design

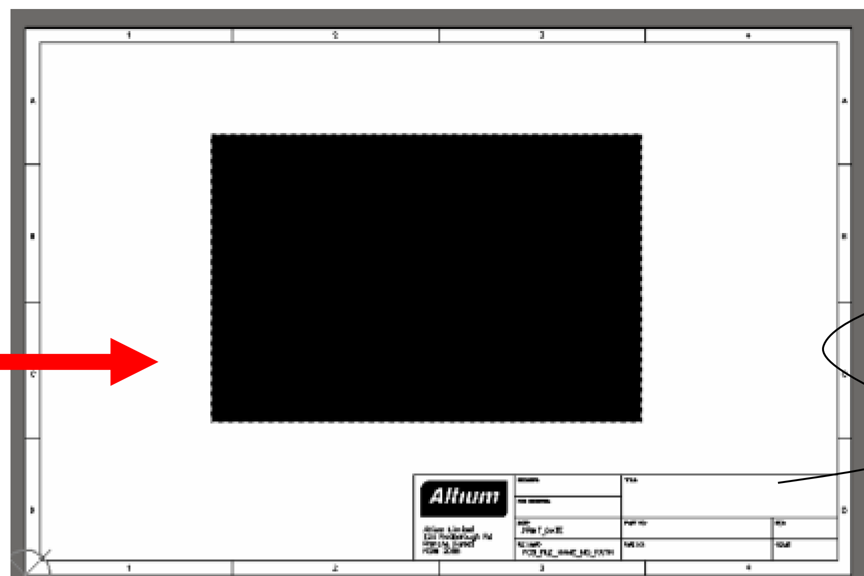
http://techdocs.altium.com/display/ADOH/Board+Implementation



Creating a New Board from a template

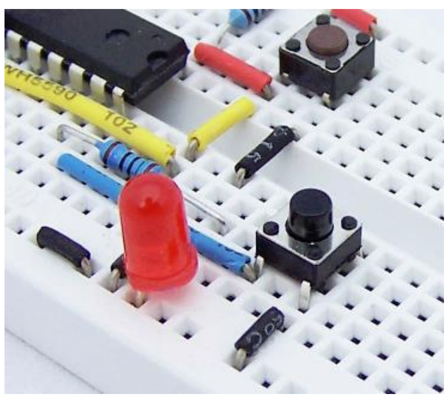


- Files Panel:
  - New from template
  - select the A4.PcbDoc template
  - Save as … same name as SchDoc file (but it may end in another directory)

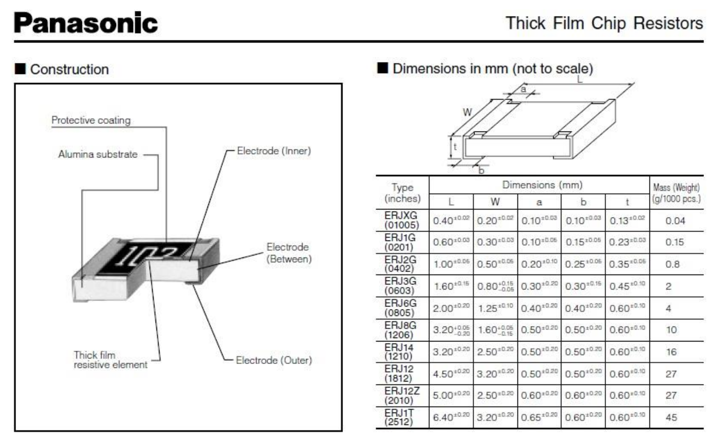


First things first … choosing working units

- Imperial (inches)
  - 1/1000th of an inch = 1 mil = 1thou
  - 100mils (0.1”) is a common dimension



- Metric (mm)
  - 1 mm ≠ 1mil !
  - Common unit in SM parts



Panasonic Thick Film Chip Resistors

■ Construction

■ Dimensions in mm (not to scale)

Type (inches)	Dimensions (mm) L	W	a	b	t	Mass (Weight) (g/1000 pcs.)
ERJXG (01005)	$0.40^{\pm0.02}$	$0.20^{\pm0.02}$	$0.10^{\pm0.03}$	$0.10^{\pm0.03}$	$0.13^{\pm0.02}$	0.04
ERJ1G (0201)	$0.60^{\pm0.03}$	$0.30^{\pm0.03}$	$0.10^{\pm0.05}$	$0.15^{\pm0.05}$	$0.23^{\pm0.03}$	0.15
ERJ2G (0402)	$1.00^{\pm0.05}$	$0.50^{\pm0.05}$	$0.20^{\pm0.10}$	$0.25^{\pm0.05}$	$0.35^{\pm0.05}$	0.8
ERJ3G (0603)	$1.60^{\pm0.15}$	$0.80^{+0.15}_{-0.05}$	$0.30^{\pm0.20}$	$0.30^{\pm0.15}$	$0.45^{\pm0.10}$	2
ERJ6G (0805)	$2.00^{\pm0.20}$	$1.25^{\pm0.10}$	$0.40^{\pm0.20}$	$0.40^{\pm0.20}$	$0.60^{\pm0.10}$	4
ERJ8G (1206)	$3.20^{+0.05}_{-0.20}$	$1.60^{+0.05}_{-0.15}$	$0.50^{\pm0.20}$	$0.50^{\pm0.20}$	$0.60^{\pm0.10}$	10
ERJ14 (1210)	$3.20^{\pm0.20}$	$2.50^{\pm0.20}$	$0.50^{\pm0.20}$	$0.50^{\pm0.20}$	$0.60^{\pm0.10}$	16
ERJ12 (1812)	$4.50^{\pm0.20}$	$3.20^{\pm0.20}$	$0.50^{\pm0.20}$	$0.50^{\pm0.20}$	$0.60^{\pm0.10}$	27
ERJ12Z (2010)	$5.00^{\pm0.20}$	$2.50^{\pm0.20}$	$0.60^{\pm0.20}$	$0.60^{\pm0.20}$	$0.60^{\pm0.10}$	27
ERJ1T (2512)	$6.40^{\pm0.20}$	$3.20^{\pm0.20}$	$0.65^{\pm0.20}$	$0.60^{\pm0.20}$	$0.60^{\pm0.10}$	45

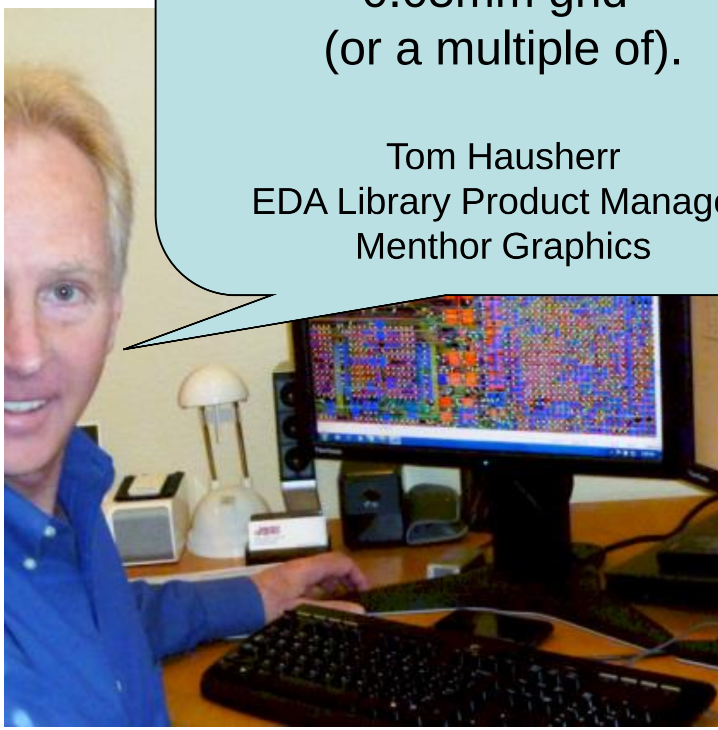
- Remember: 100mils = 2.54mm
- To switch units in Altium Press <Q>

Metric or Imperial?

"every element in a PCB design should reside on a 0.05mm grid"
(or a multiple of).

Tom Hausherr
EDA Library Product Manager,
Menthor Graphics

Old PCB wisdom:
“thou shall use thous”
David L. Jones
EEV blog

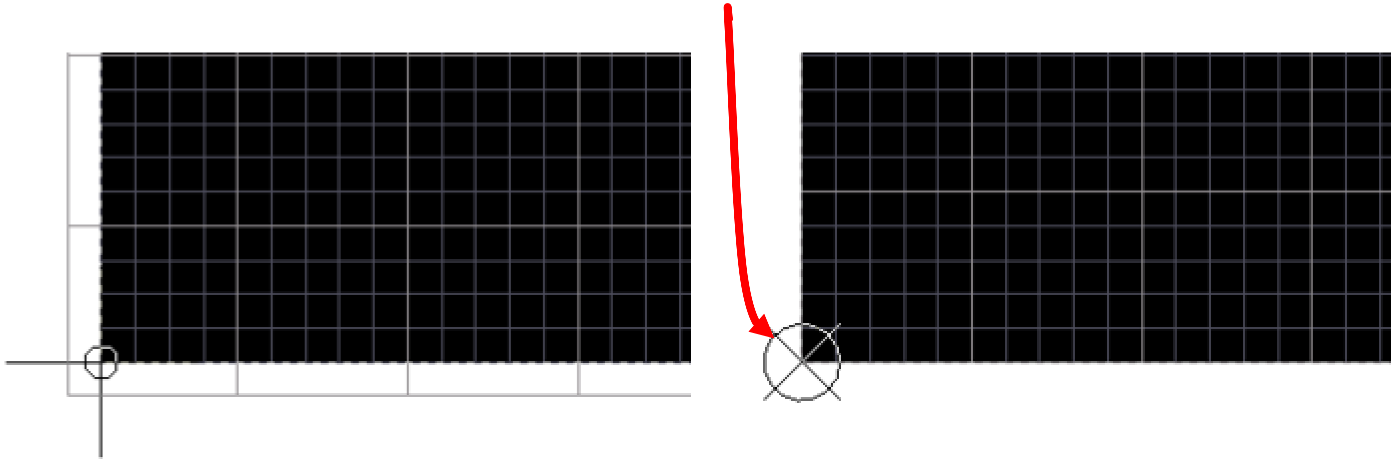


Comment driven by high density & modern surface mount technology

Comment driven by traditional 0.1” spacing between pins

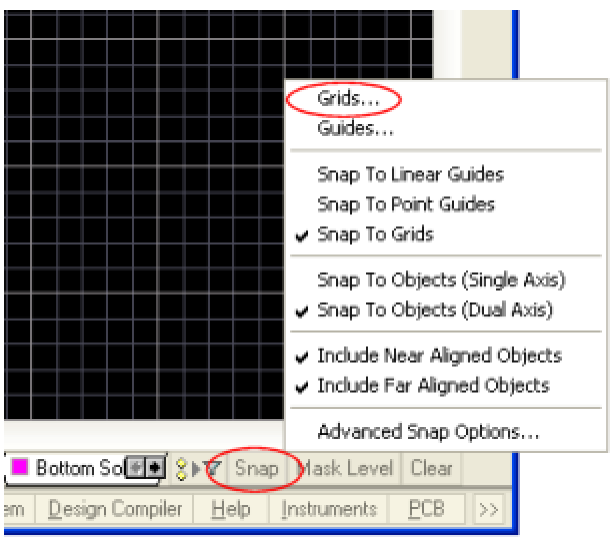
First things first … setting the board origin

- Absolute origin (lower left corner)
- User-defined relative origin
    - Edit >> Origin >> Set



First things first … setting the snap grid

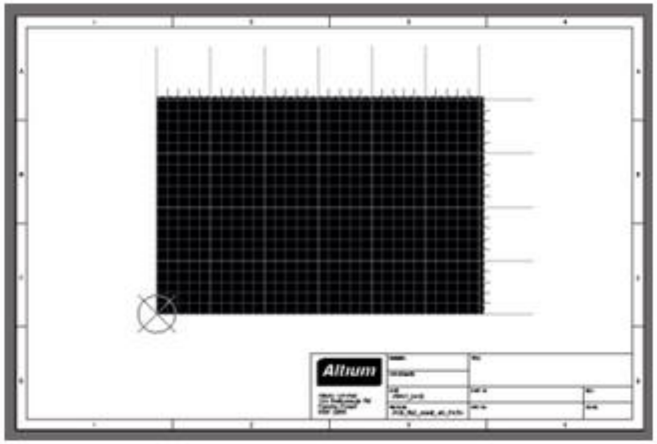
- PCBs are grid based objects
- Recent past: … there were several grids
  - visible grid
  - snap grid: controls mouse movement
  - component grid: controls placement of components
  - electrical grid: range of attraction

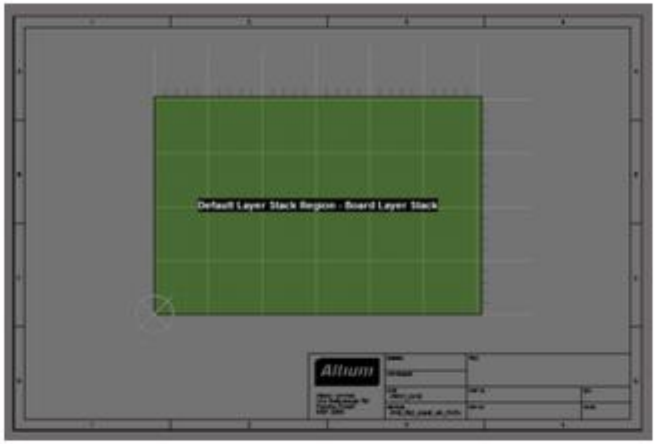


- Now: **Unified Cursor-Snap System**
- Selecting a suitable snap grid:
  - <Ctrl>+<G>
  - Start with a coarse grid to define board size

First things first … redefining the board shape

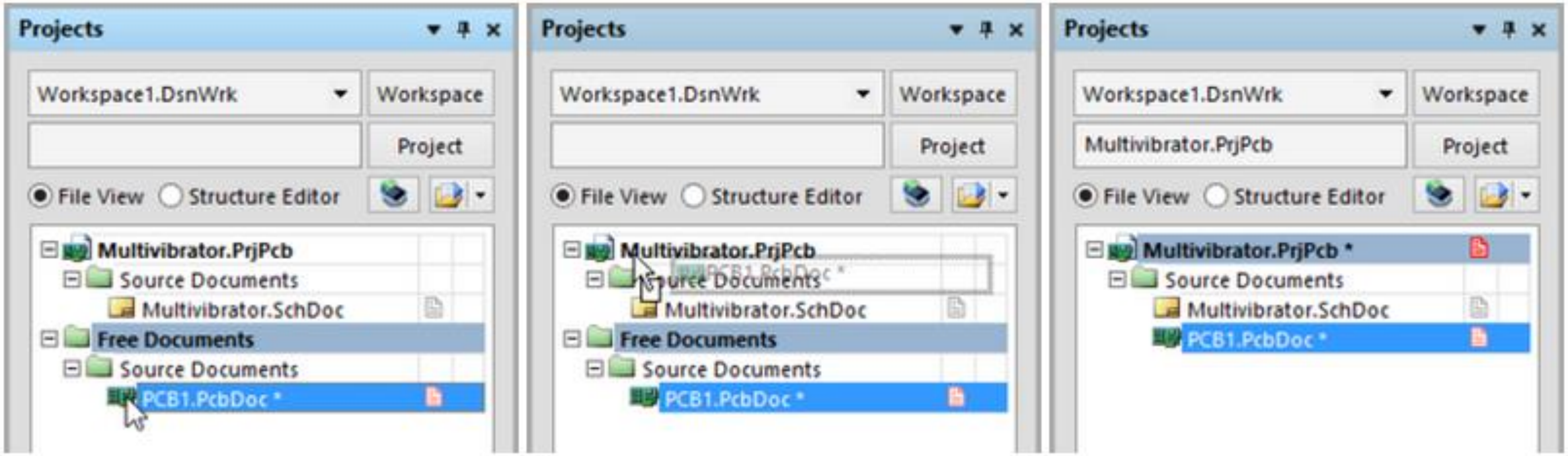
- Viewing modes:
  - Board Planning Mode (**1**)
    - **Design » Edit Board Shape**
    - **Design >> Move Board Shape** (Relocate the origin)
  - 2D Layout Mode (**2**)
  - 3D Layout Mode (**3**).





Design transfer

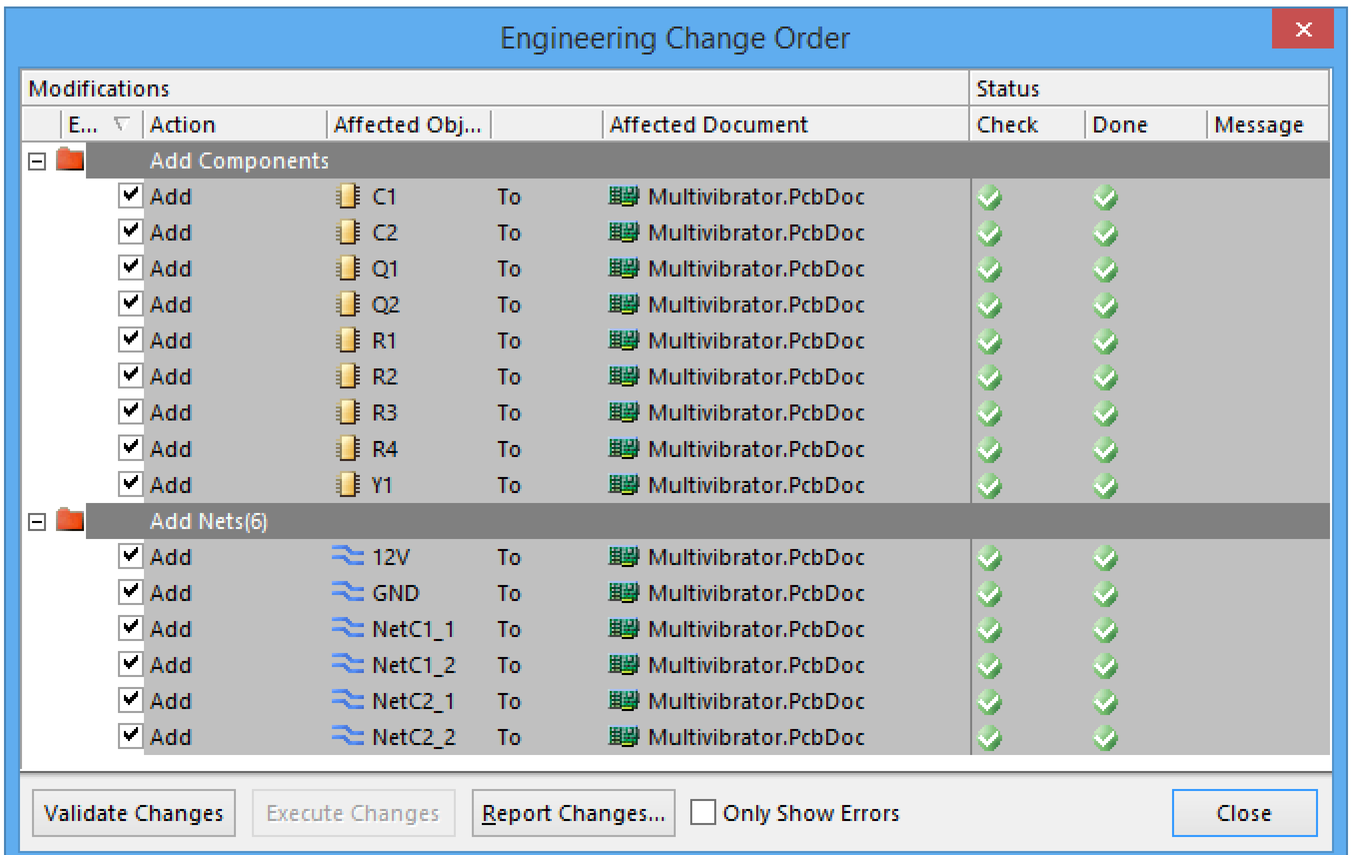
- Make the PCB board part of the project



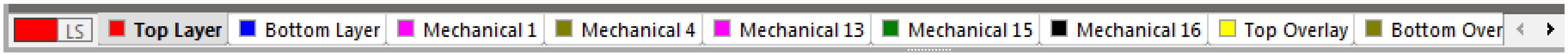
- Rename the file
- Save the PcBDoc file and the project

Design transfer

- Design transfer
  - On Schematic file
    - Design >> Update PCB Document …



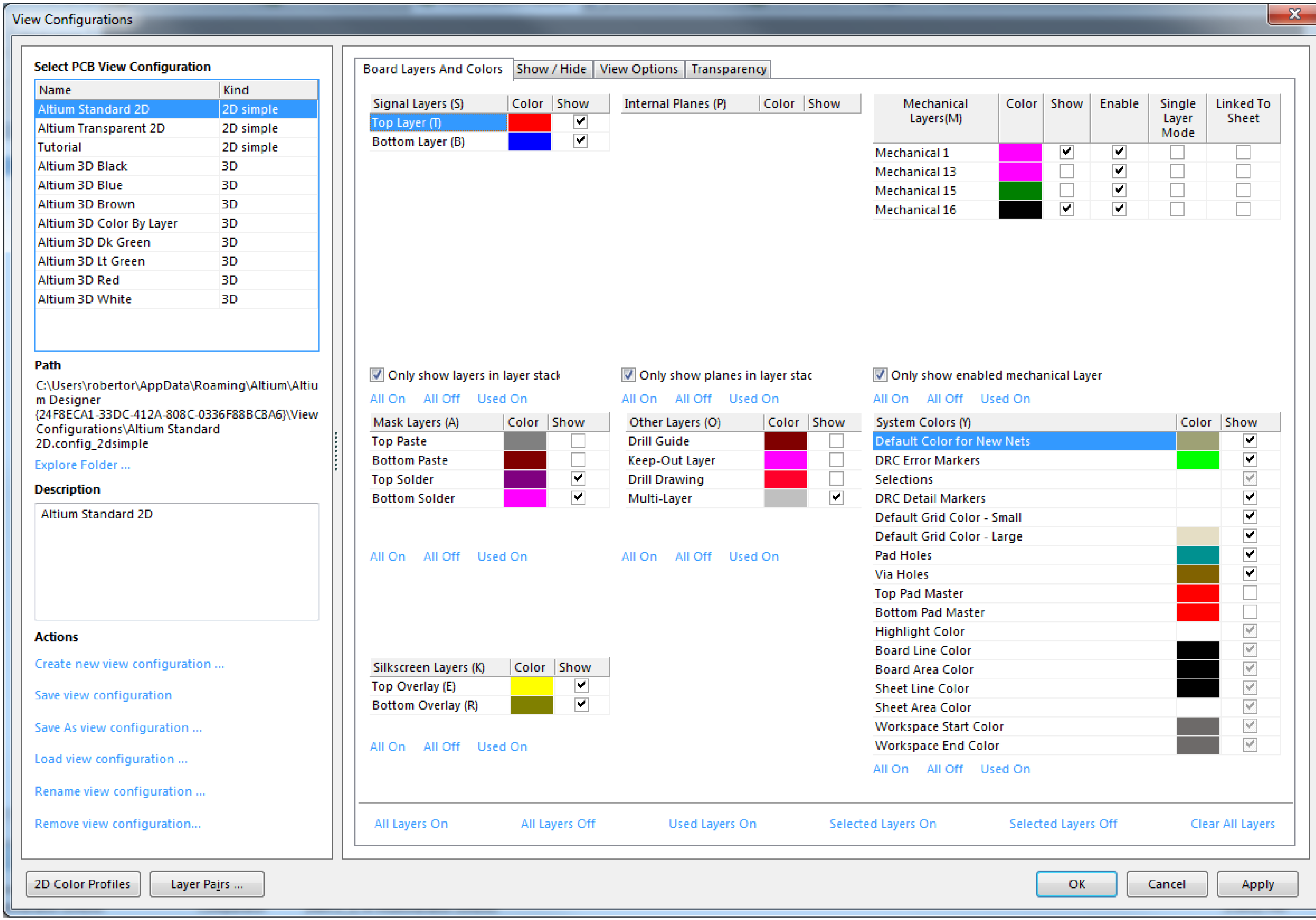
Configuring the Display Layers



- Electrical layers
  32 signal layers and 16 internal power plane layers.
- Mechanical layers
  32 general purpose mechanical layers, used for design tasks such as dimensions, fabrication details, assembly instructions, or special purpose tasks such as glue dot layers. These layers can be selectively included in print and Gerber output generation. They can also be paired, meaning that objects placed on one of the paired layers in the library editor, will flip to the other layer in the pair when the component is flipped to the bottom side of the board.
- Special layers
  these include the top and bottom silkscreen layers, the solder and paste mask layers, drill layers, the Keep-Out layer (used to define the electrical boundaries), the multilayer (used for multilayer pads and vias), the connection layer, DRC error layer, grid layers, hole layers, and other display-type layers.

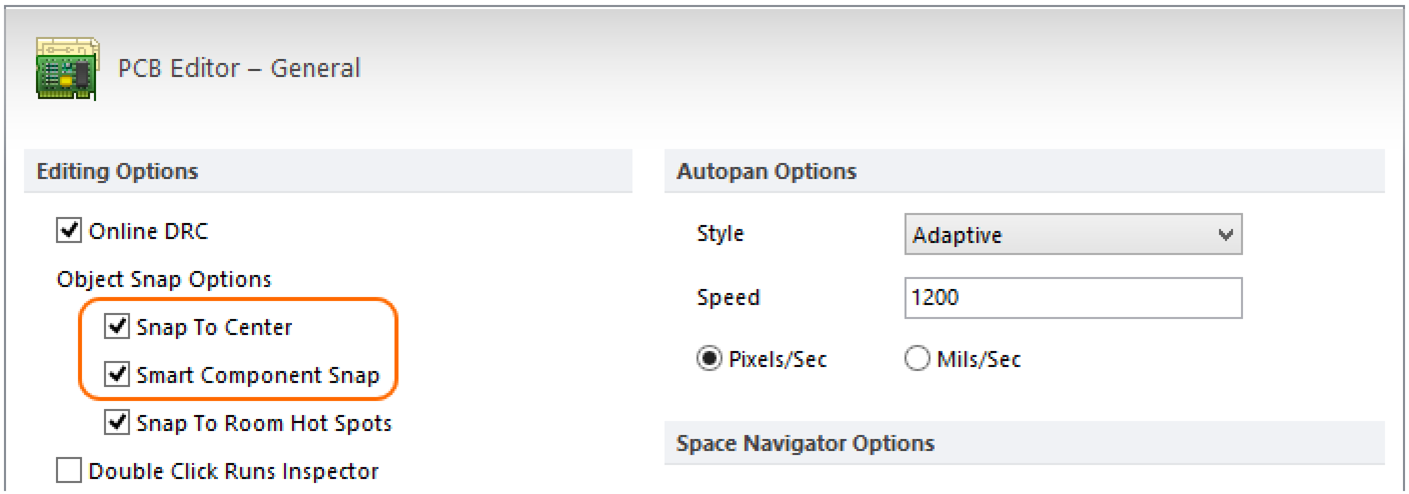
Configuring the Display Layers

- Design » Board Layers and Colors



Component positioning and placement options

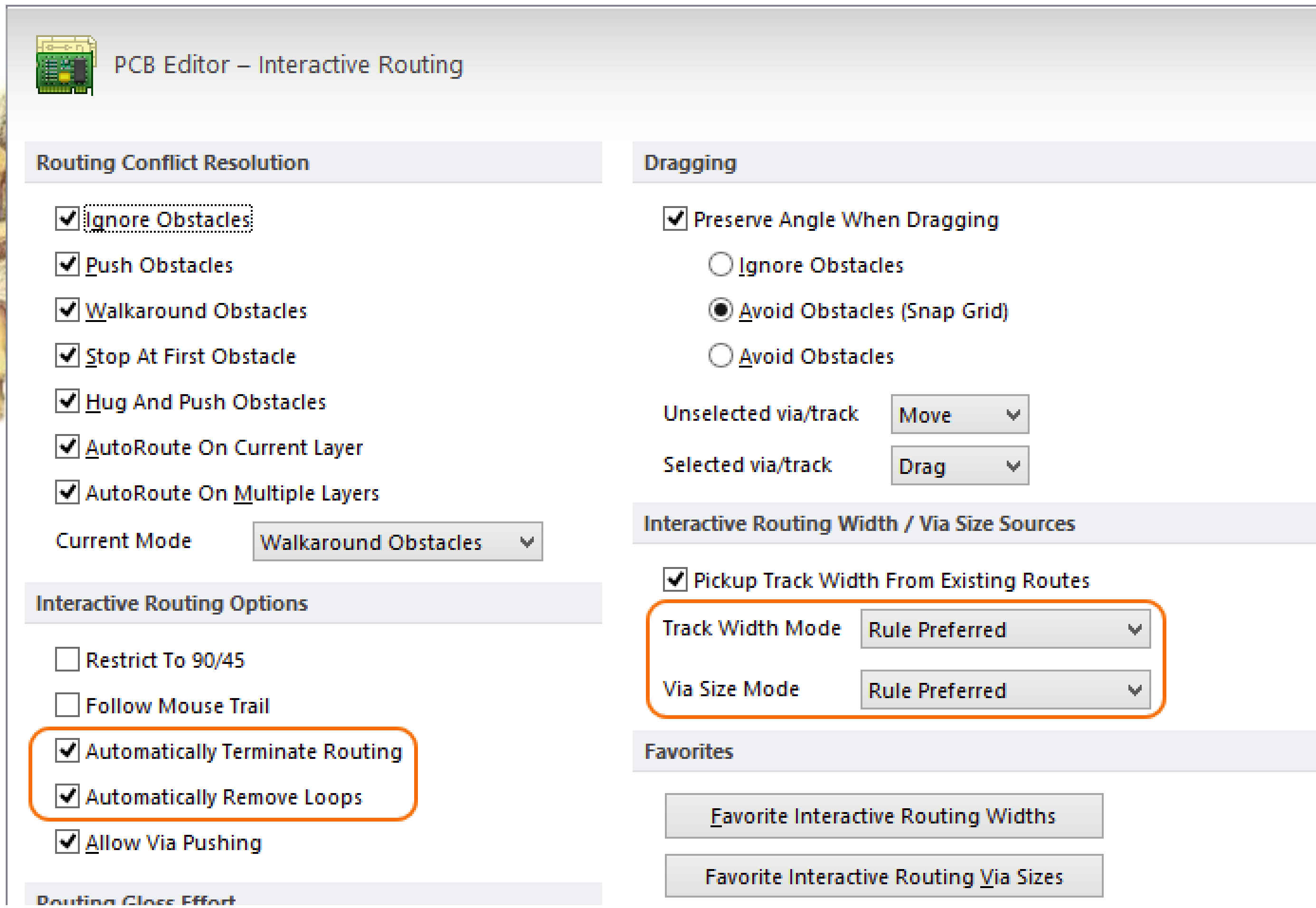
- Tools >> Preferences



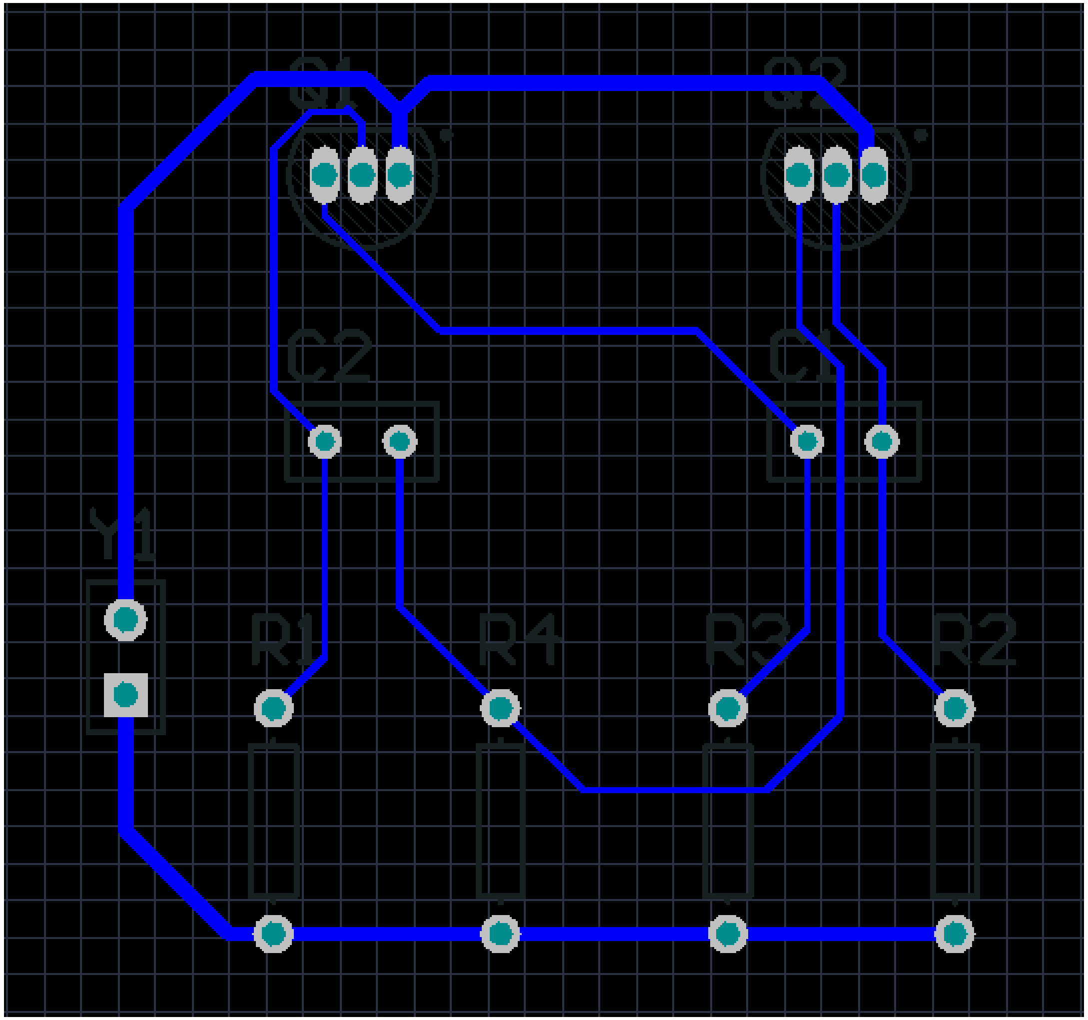
Words of wisdom:
These are very useful!

Component positioning and placement options

- Tools >> Preferences



Positioning components & routing



Design Rules

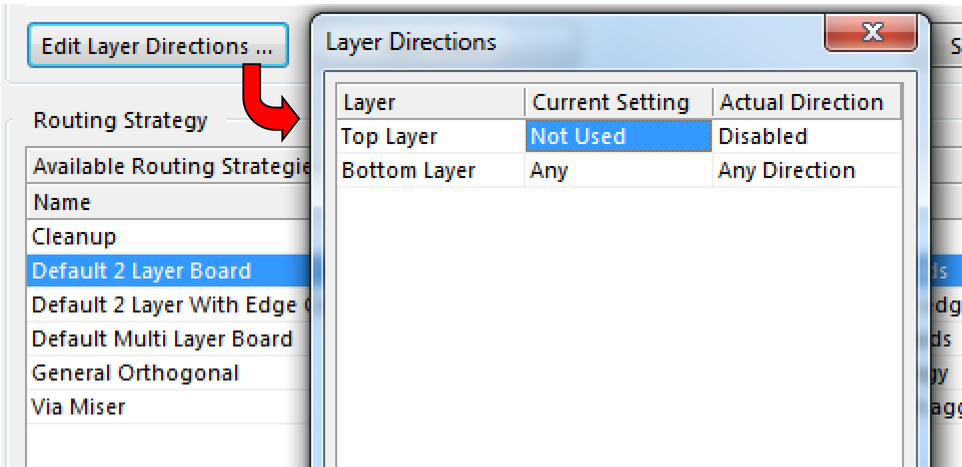
- Design >> Rules

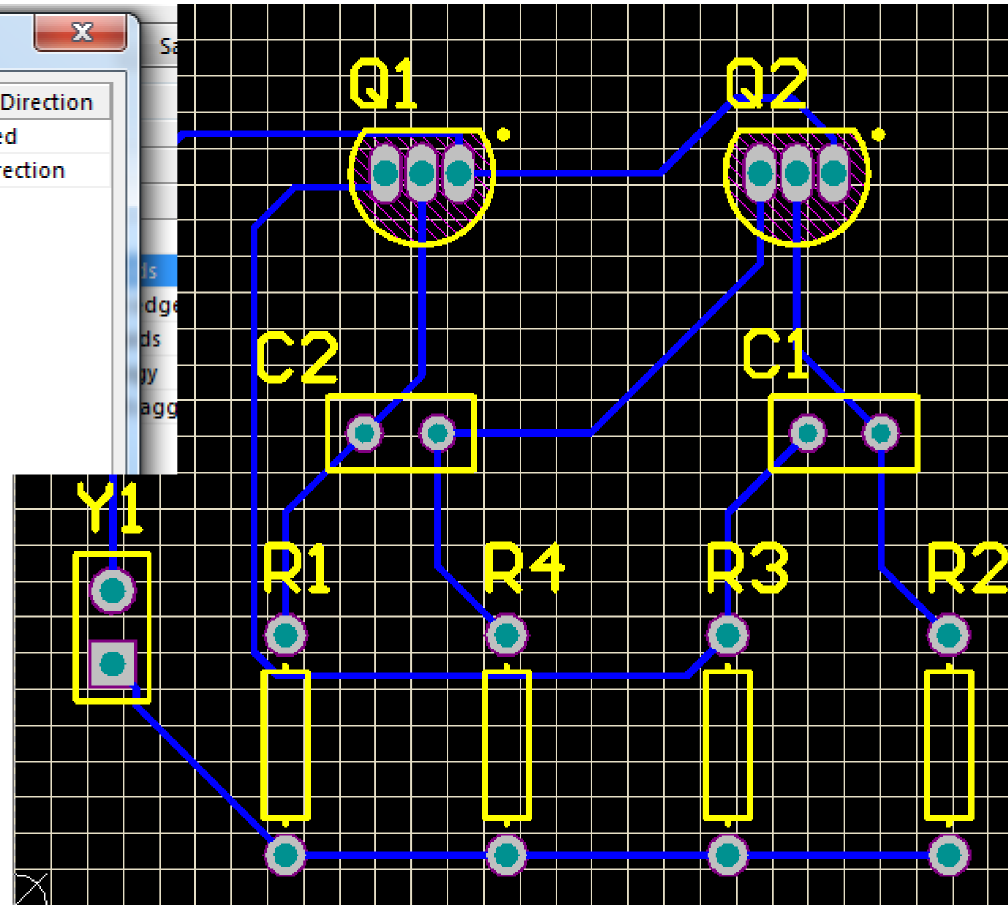
Rule	Constrain	Query
Routing, Width*	Min width = 7mils Max width =50mils Preferred =10mils	All
Routing, Width_Power	Min width = 7mils Max width =60mils Preferred =40mils	Advanced (Query) (InNet('12V') **OR** InNet('GND'))
Electrical, Clearance	Min clearance = 10mil (1)	All

(1) We can use 7mils for your projects

Auto route

- Tools » Un-Route » All
- Auto Route » All





- You can set single layer routing

Handy shortcuts for routing

- Press ***** on the numeric keypad while routing to cycle through the available signal layers. A via will automatically be added, in accordance with the applicable Routing Via Style design rule. Alternatively, use **Ctrl+Shift+Roll** shortcuts to move back and forth through the available signal layers.

- **Shift**+**R** to cycle through the enabled conflict resolution modes, including Push, Walkaround, Hug and Push, and Ignore. Enable the required modes in the **PCB Editor - Interactive Routing** page of the *Preferences* dialog.

- **Shift**+**S** to cycle single layer mode on and off, ideal when there are many objects on multiple layers.

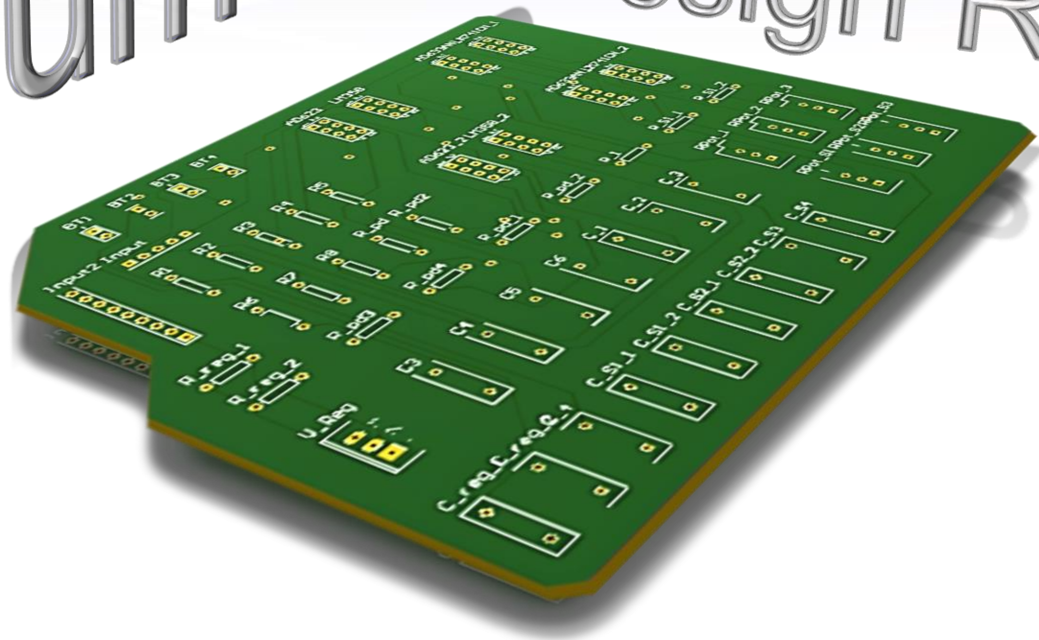
- **Spacebar** to toggle the corner direction (for all but any angle mode).

- **Shift**+**Spacebar** to cycle through the various track corner modes. The styles are: any angle, 45°, 45° with arc, 90° and 90° with arc. There is an option to limit this to 45° and 90° in the **PCB Editor - Interactive Routing** page of the *Preferences* dialog.

ELEC 391

Altium PCB

Design Rules



Andy

Submission Instructions

- Every group is entitled to **three** submissions
- Cost: \$25 + \$10/ sq-in
- Submission dates:

  Midnight, every Monday until March 21
  we will check submissions and accept fixes
  until Tuesday 5PM
- Turn around: 6 business days
- Work within the listed guidelines
- Verify PCB layout and design - prior to design submission
- <u>Add your group number on the top overlay – make it visible</u>

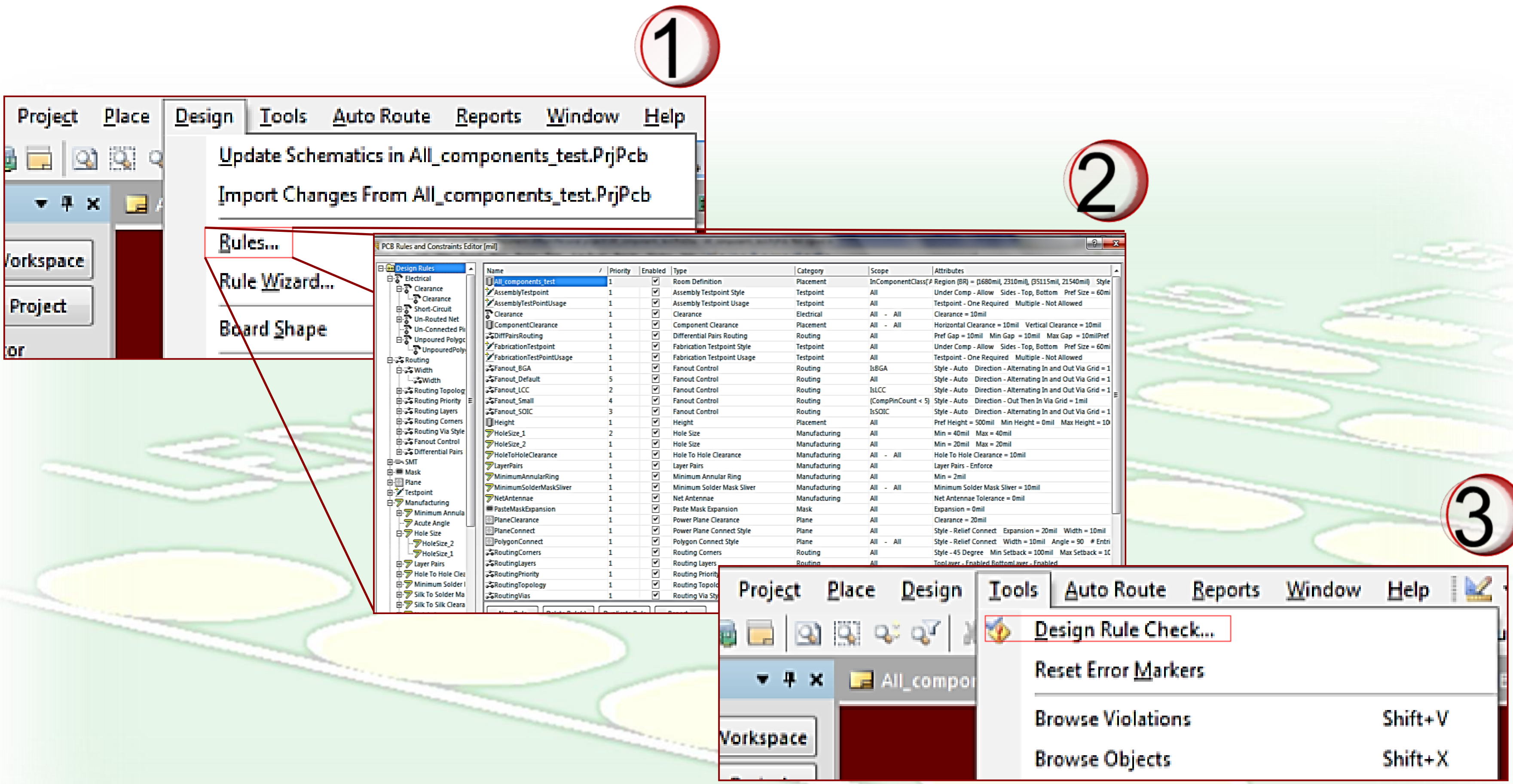
Submission Instructions

- Email pcb@ece.ubc.ca
  Subject: [PCB] ELEC391, Group Section #, submission# (out of 3)
- Attach: Zipped file with your PCB Project file (*.PrjPcb) and all associated files, also include the latest DRC report. (make sure all files are under the same directory)

  Body:
  Total number of boards to fabricate:
  Name of boards to fabricate and number of copies for each:

  Do not forget to:
  - include your group number on the top overlay layer
  - draw a board outline on Mechanical 1

Rules and Checks

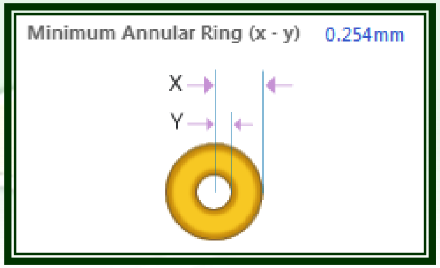


Rules – design rules

- DRC file available here:
  http://www.ece.ubc.ca/~eng-services/files/courses/elec391/pcb-design/Notes_PCB_Layout.txt
- Download and save as ".RUL" file
- On your PCB design select:
  Design >> Rules
- On the 'PCB Rules and Constrains Editor', Right click anywhere on the left column
  - Select: Import Rules
  - Select all rules in window (using shift) → OK
  - Choose .RUL file
  - Clear existing rules prior to import? → NO

Rules – design rules

- Component clearance and (electrical) clearance:
  - Minimum distance = 7 mil
- (Routing) width:
  - Minimum trace width = 7 mil
- Layer:
  - Maximum number of layers = 2
- Annular ring size:
  - (create as new rule in Design -> Rules -> Manufacturing -> MinimumAnnularRing -> New Rule)
  - Minimum annular ring size = 8 mil

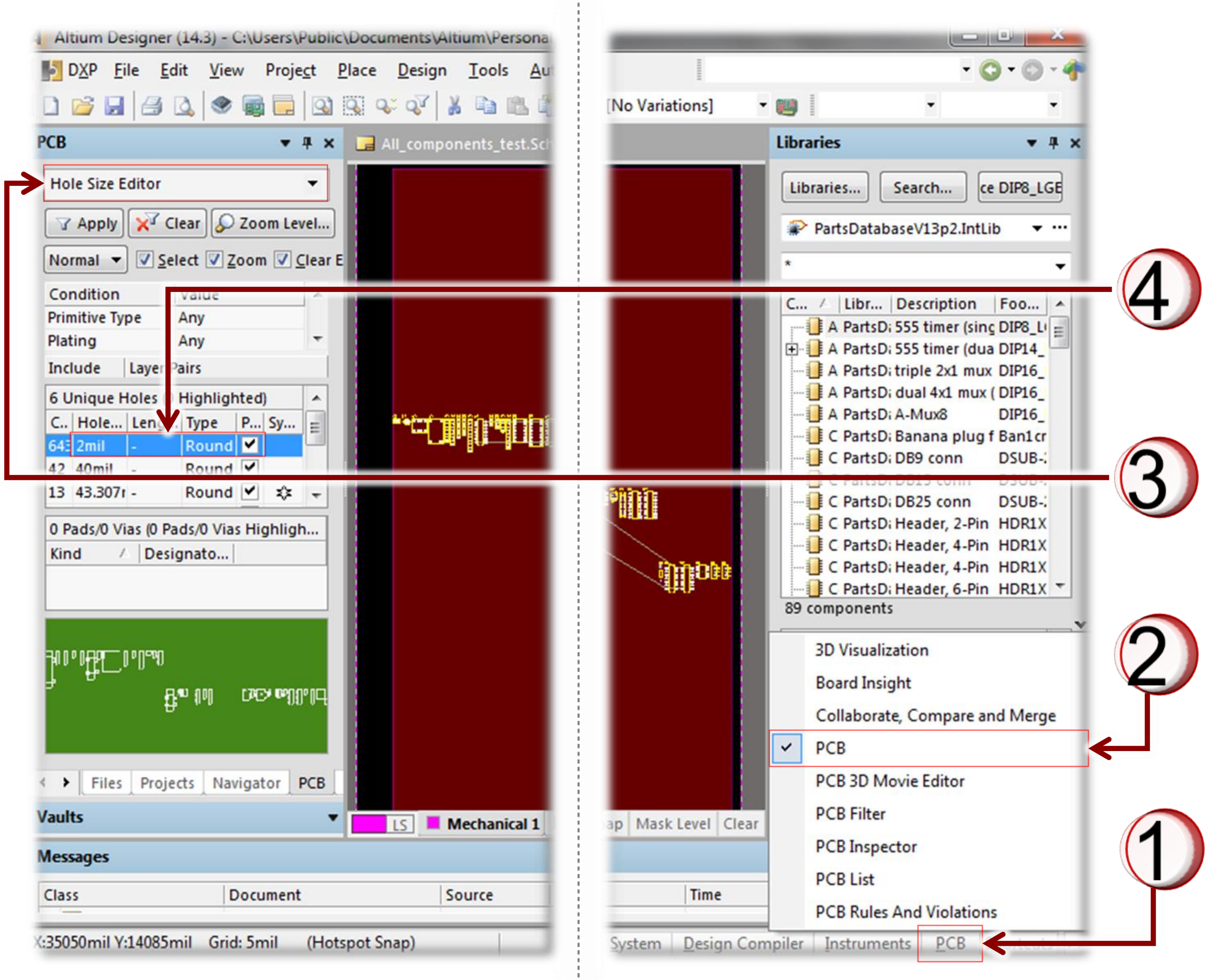


Rules – hole sizes

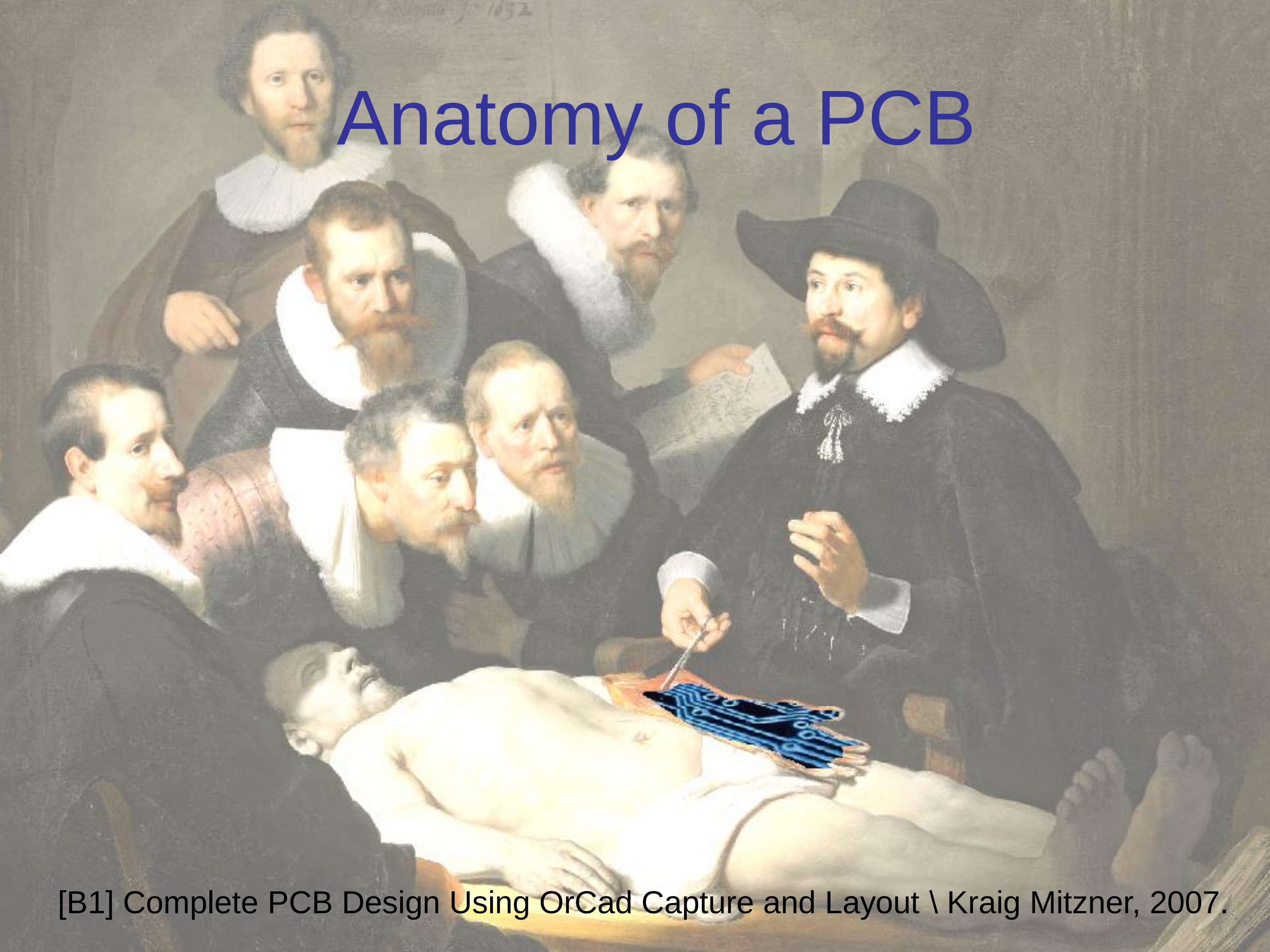
- Pre-selected hole and drill sizes: [plated vs. non-plated sizes]

Drill Number Set	Drill Size	Finished Size	Approximate Use
#76	.020"	.017"	via holes
#70	.028"	.025"	via holes, fine lead devices such as trim pots etc.
#65	.035"	.032"	IC's, 1/4 watt resistors, small diodes, ripple caps etc.
#62	.038"	.035"	Square posted pins that measure .025" on the flat.
#58	.042"	.039"	TO-220 packages, IDC type square posted headers, 1/2 watt resistors, 1N9000 series diodes, IC chip carriers, etc.
#55	.052"	.049"	larger connectors, transformer leads, etc.
#53	.060"	.057"	similar to .052" above
#44	.086"	.083"	TO-220 mounting holes, screw holes, general mounting
1/8 in.	.125"	.122"	mounting holes
#24	.152"	.149"	mounting holes

PCB Hole Size Editor



Anatomy of a PCB



[B1] Complete PCB Design Using OrCad Capture and Layout \ Kraig Mitzner, 2007.

PCB Anatomy: Substrate

Ref [B1]

- Substrate (laminate)
  - Rigid board of insulating material
  - Provides structural support to the circuit components
  - Most commonly used material type is FR4, 62-63mils thick
  - Laminates are available in different thicknesses

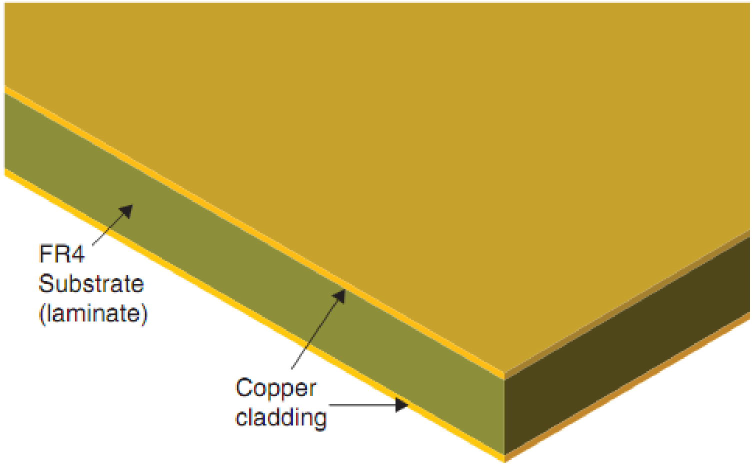


Figure 1-2 A double-sided copper clad FR4 substrate.

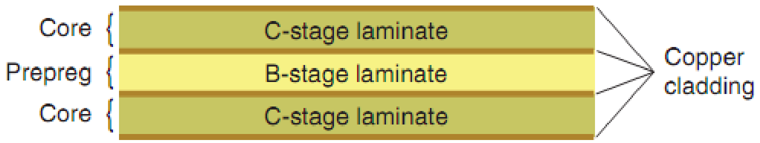


Figure 1-3 Cores and prepreg.

Cu thickness measured in weight oz/ft^2

½ oz → 0.7mils

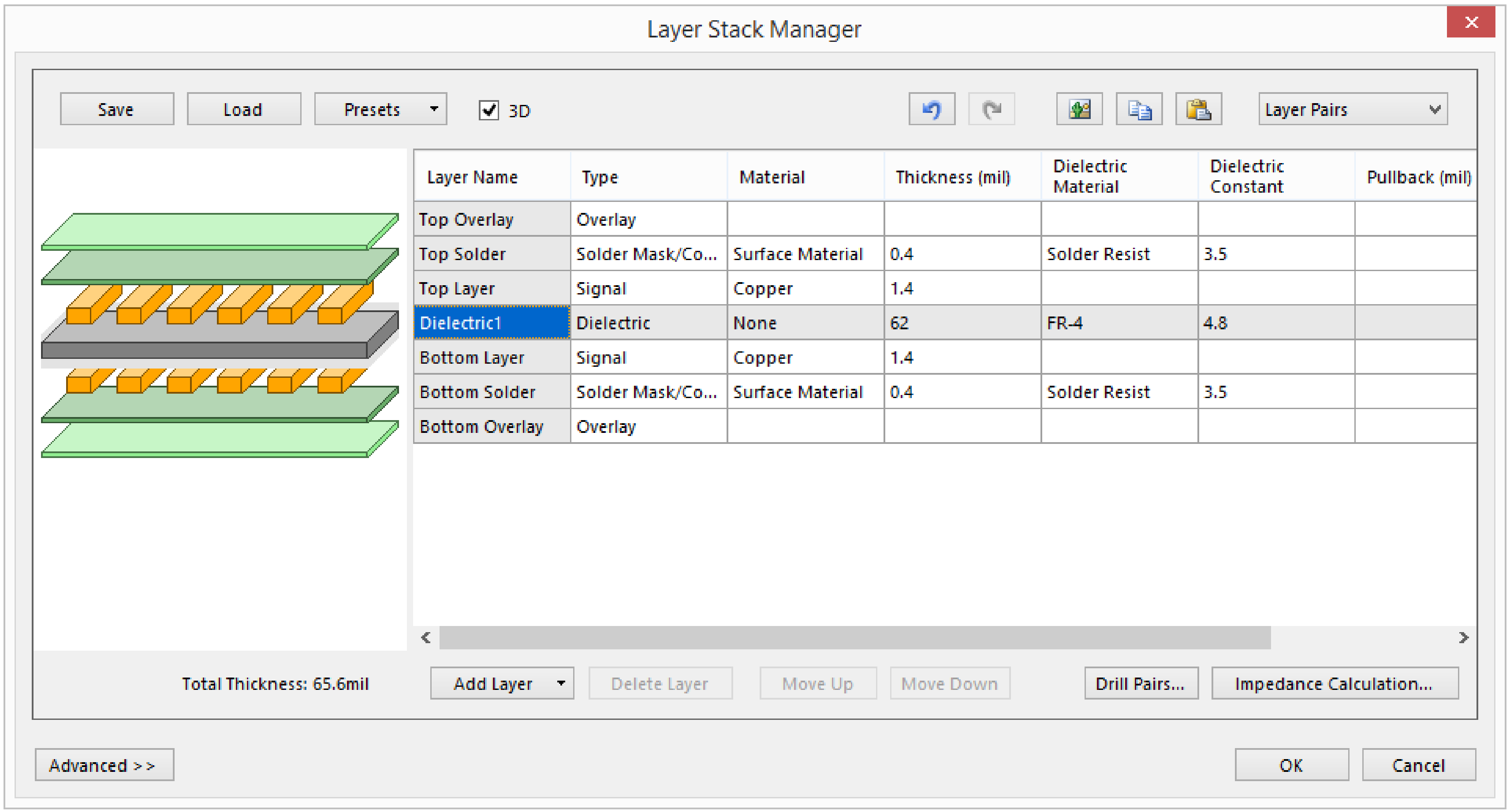
1 oz → 1.4mils

2 oz → 2.8mils

1mil = 25µm

PCB Anatomy: Layer Stackup

Design >> Layer Stack Manager …



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)
Top Overlay	Overlay					
Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5	
Top Layer	Signal	Copper	1.4			
Dielectric1	Dielectric	None	62	FR-4	4.8	
Bottom Layer	Signal	Copper	1.4			
Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5	
Bottom Overlay	Overlay					

Ref [B1]

PCB Anatomy: Traces / Tracks

- Copper traces are patterned either by:
  - Photolithography: requires photomasks
  - Laser: used to draw patterns on photoresist
  - Mechanical milling: Cu is removed to isolate the traces.
- Trace width and thickness determines:
  - Ampacity (current carrying capacity)
  - Characteristic impedance for RF designs
- Practical limitations:
  - Minimum trace width and gap

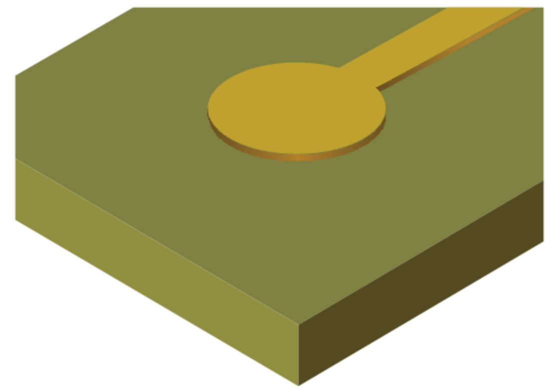


Figure 1-11 Copper pad and trace after etching and resist stripping.

Negative view: Copper planes, Drill holes, Solder Masks

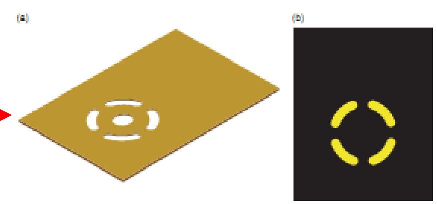


Figure 1-18 Copper in a plane layer (negative view without drill info). (a) Copper plane with thermal relief. (b) Negative view in Layout.

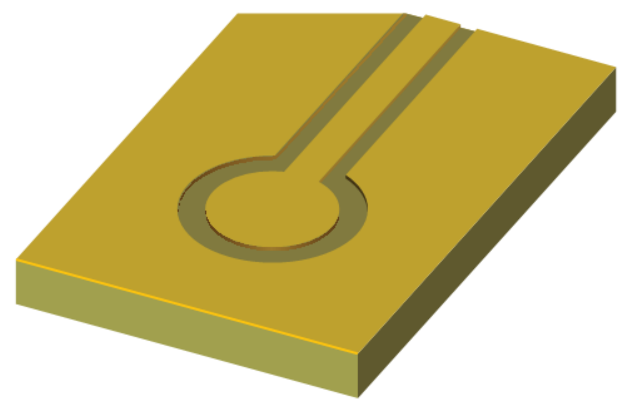
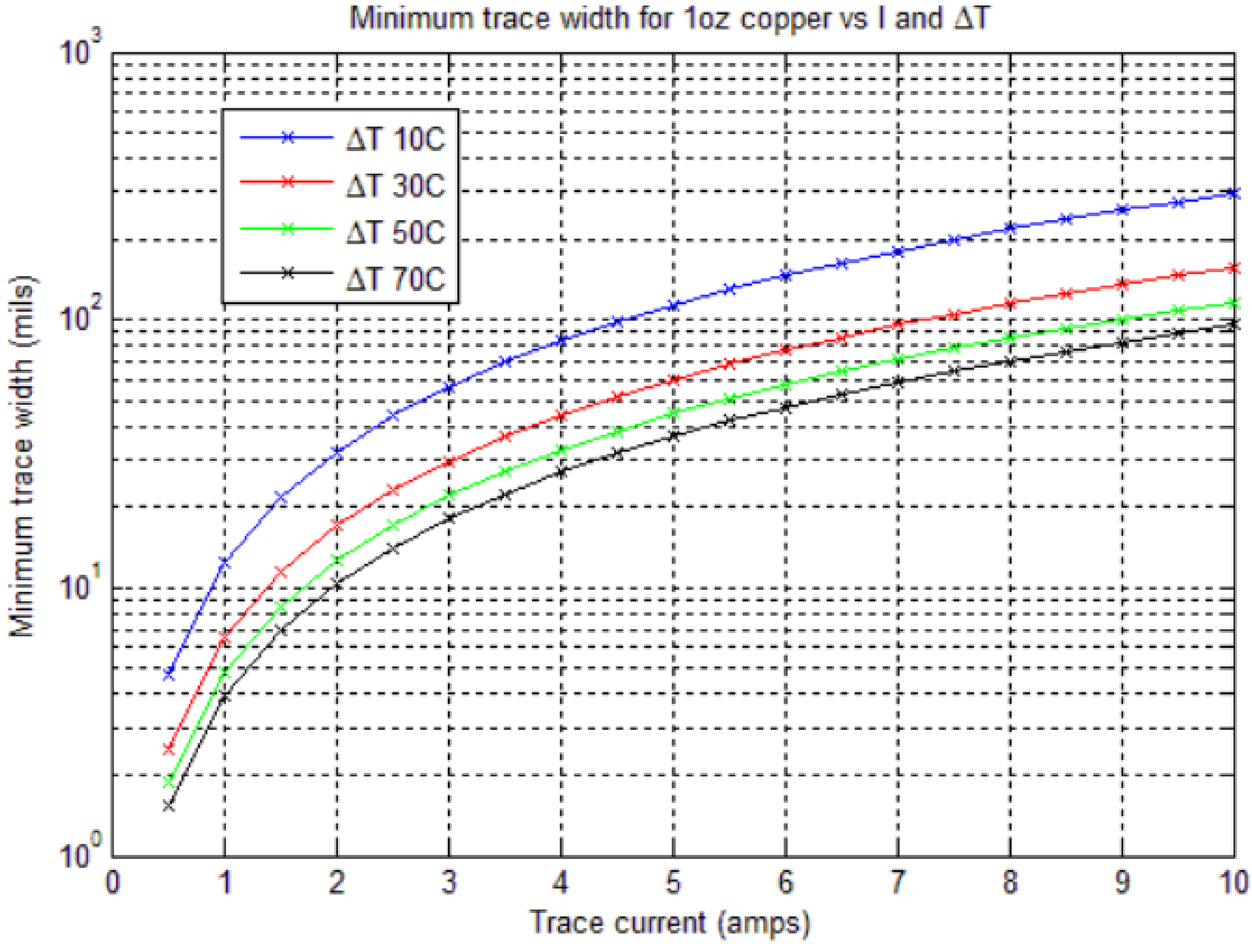


Figure 1-12 A mechanically milled trace.

PCB Anatomy: Trace width

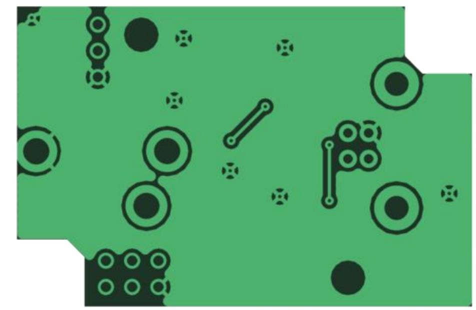


Use the following online trace width calculator:
http://circuitcalculator.com/wordpress/2006/01/31/pcb-trace-width-calculator

Ref [B1]

PCB Anatomy: Vias

- Connection between layers is accomplished with via holes
- After the holes are drilled, their inner walls are plated
- Top and bottom traces are patterned after plating



Source: wikipedia.org: Thermal pad

Thermal relief is needed when connecting a via to a copper plane

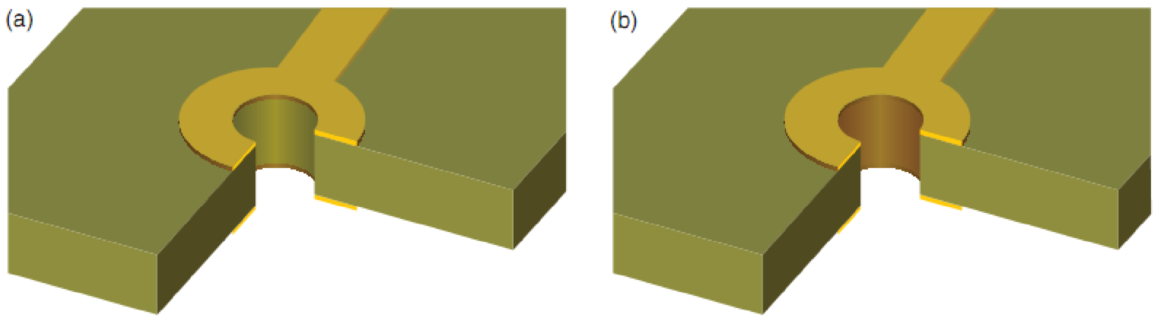


Figure 1-13 Holes are drilled into the board and then copper plated. (a) A nonplated through-hole. (b) A plated through-hole.

PWR and GND planes are commonly inner layers

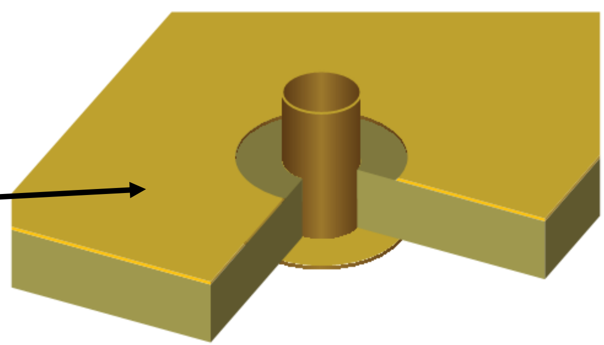


Figure 1-15 A clearance area provides isolation between a plated hole and a plane.

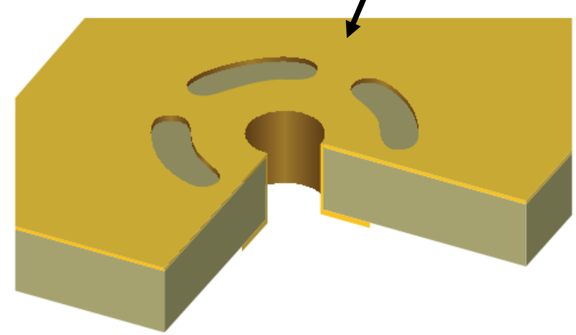
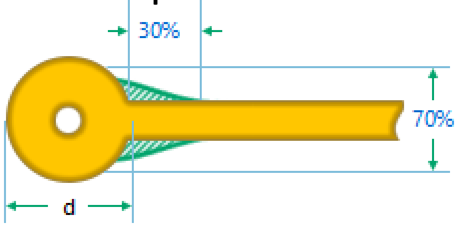


Figure 1-14 A connection to a plane layer through a thermal relief.

Teardrops:



PCB Anatomy: Vias

- Types of via holes:
  - Plated and un-plated through-hole, blind, buried

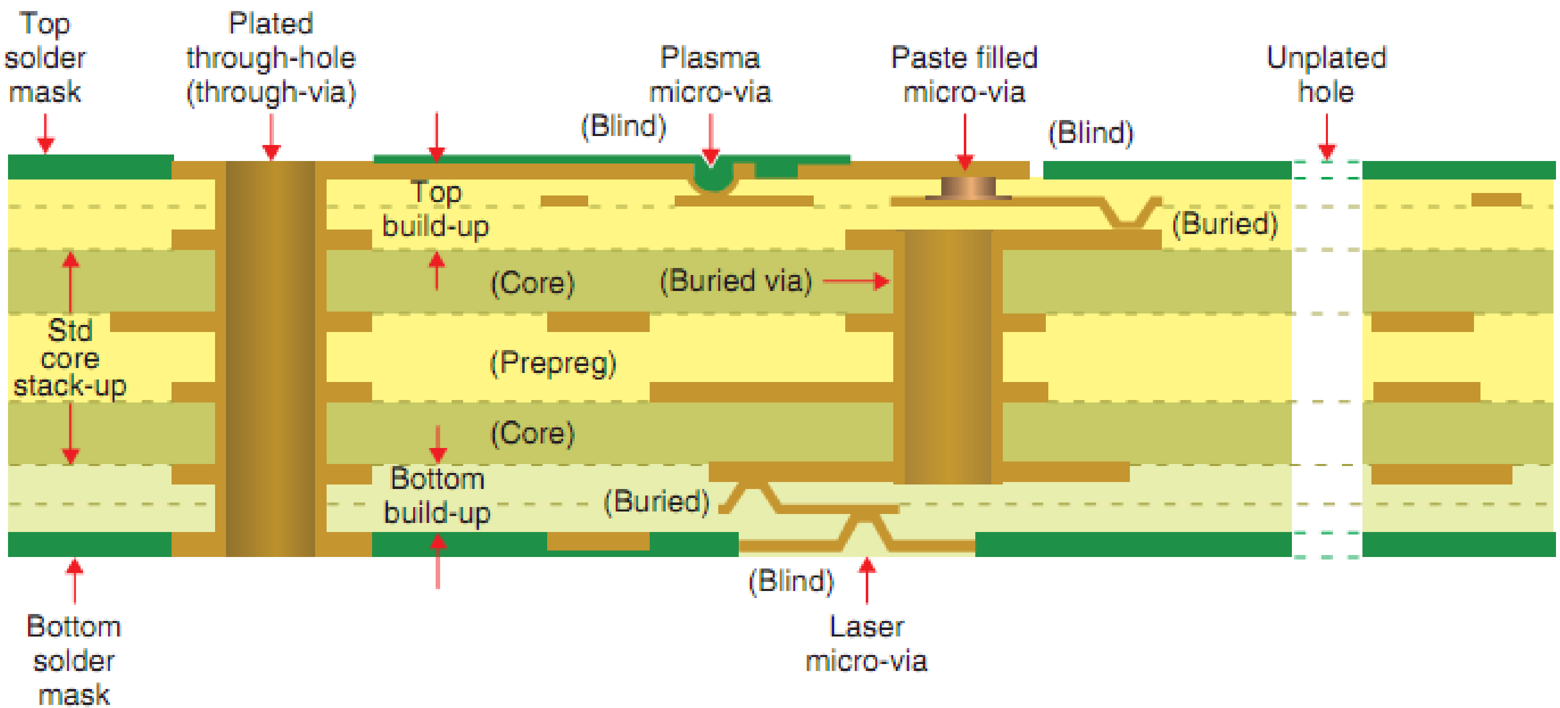


Figure 1-5 A built-up, multitechnology, PCB stack-up.

Ref [B1]

PCB Anatomy: Holes

Holes can be:

- Vias, multi-layer pads, mounting holes, or cuts
- Plated or non plated

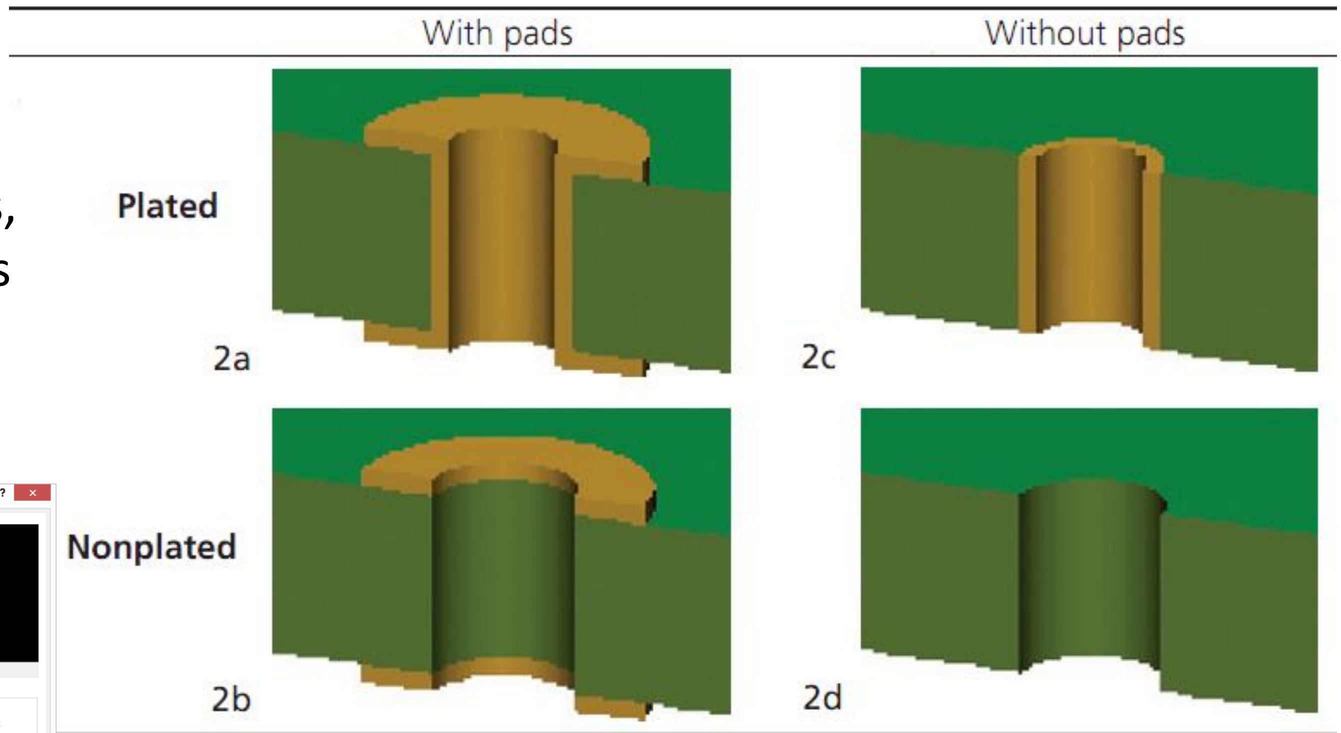
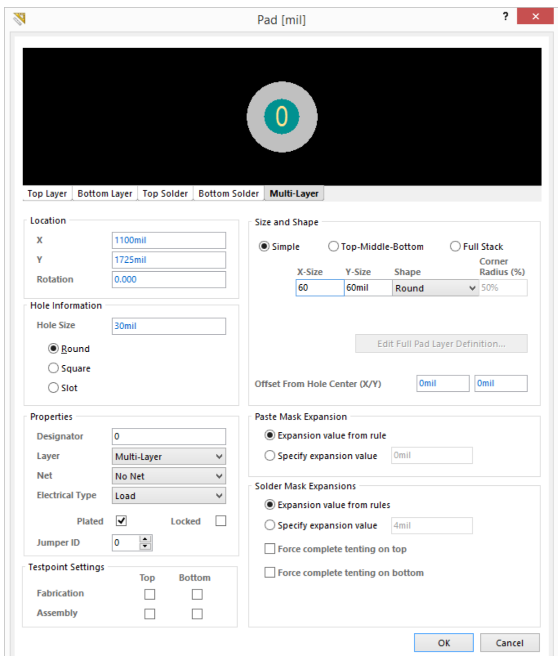


Table 8-2 Basic hole types

Altium pad properties dialog



You must specify whether a hole is plated or non plated during the design process

PCB Anatomy: Pads

- Pads: contact areas for soldering components, test points, and solder traps
- Pads can have any shape
- Single layer pads: Top/bottom layer, common for SMT, end launch connectors
- Multi-layer pads: for through hole components
- Footprints are a collection of pads

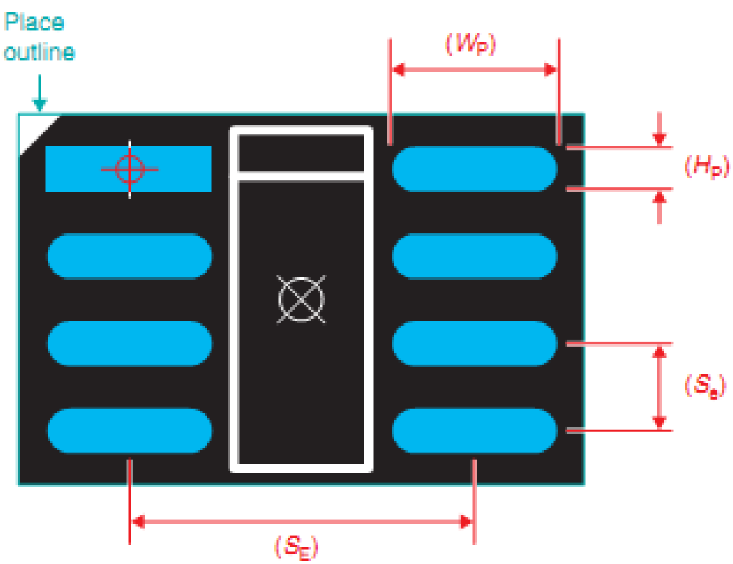


Figure 5-7 Footprint dimensions (typical convention).

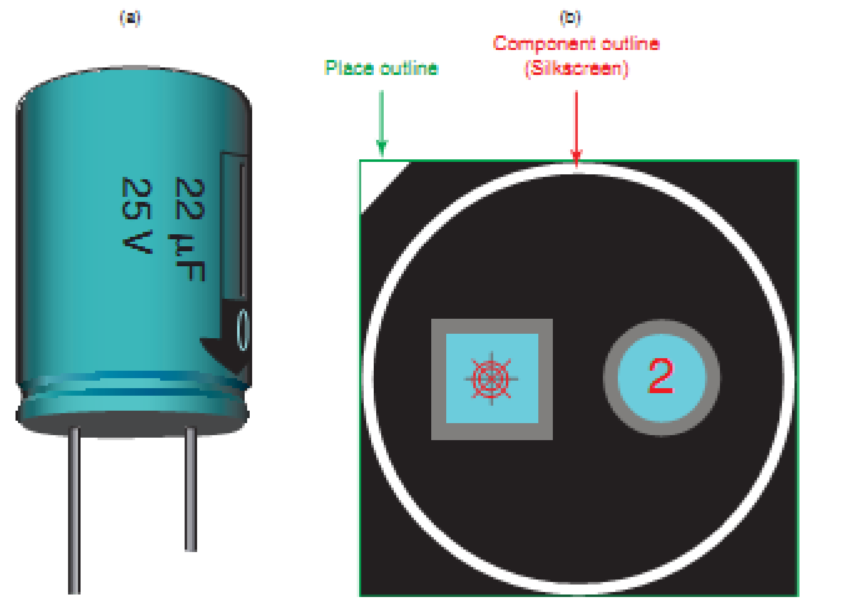


Figure 5-12 Radial-leaded through-hole device. (a) Axial-leaded capacitor. (b) Layout axial footprint

PCB Anatomy: Solder mask

- Solder mask or solder resist:
  - Thin polymer layer deposited on top and bottom layers
  - Protects outer layers from oxidation and prevents solder bridges
  - Allows for wave or reflow soldering of components
  - Holes are opened with photolithography wherever components will be soldered
  - Default color is green, but any other color is possible

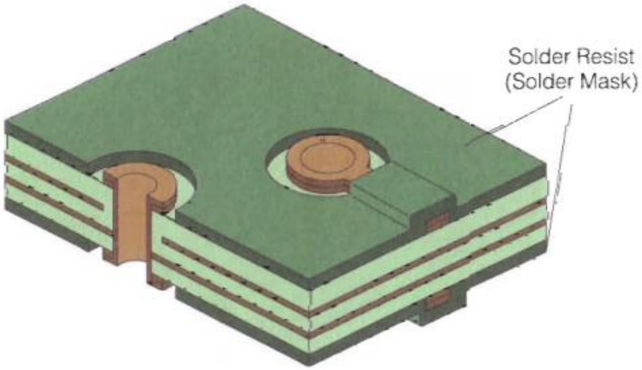


Illustration ML-14. *Apply solder resist.* The specified resist (either dry film, liquid photoimageable, or screen printed) is applied to the surfaces of the PCB or panel.

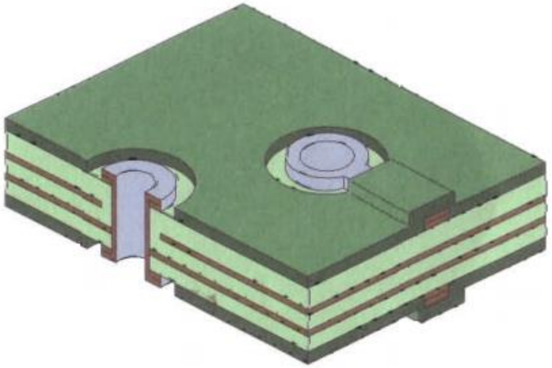
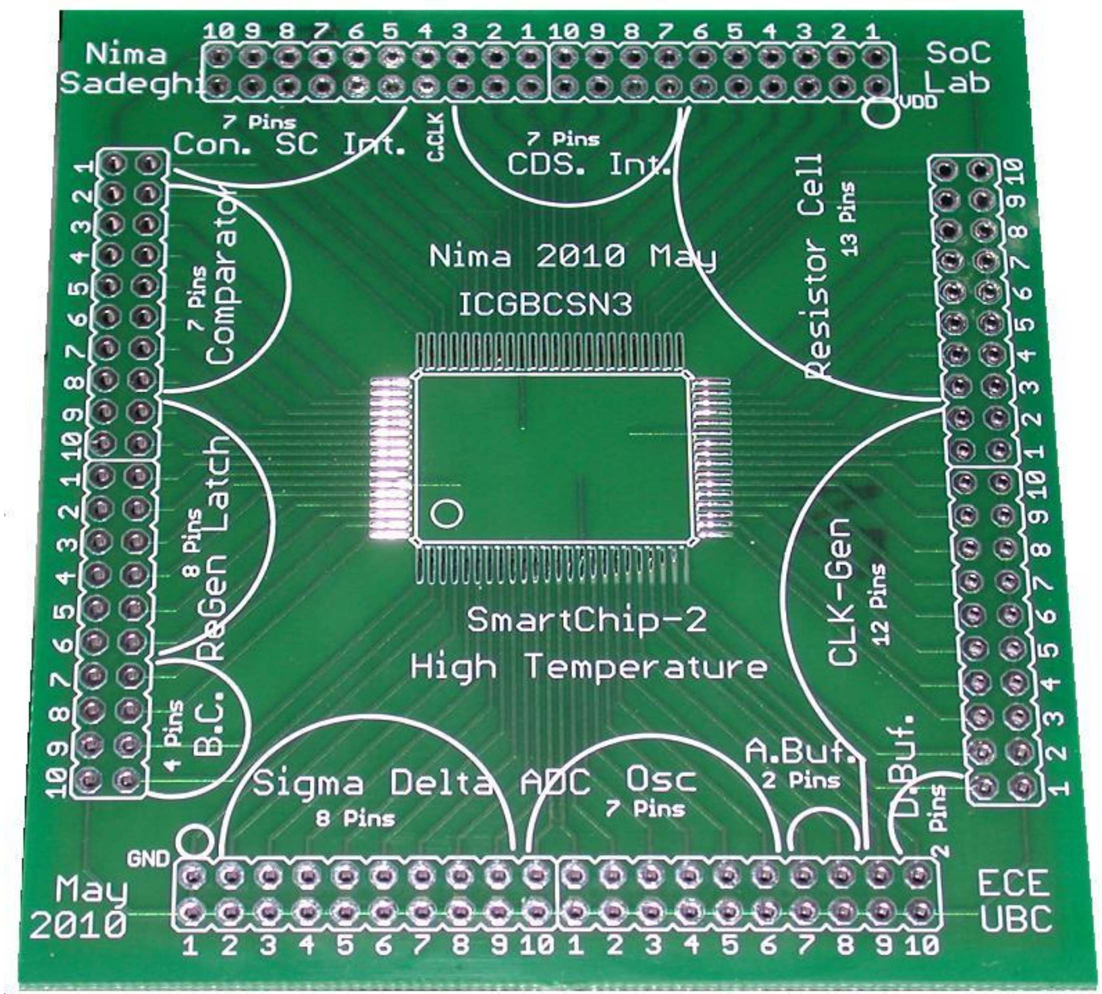


Illustration ML-15. *Solder coat.* Solder (tin/lead) is applied to the exposed copper areas, and the excess solder is removed.

Source: Printed Circuit Board Basics: An Introduction to the PCB Industry, by: Michael Flatt

PCB Anatomy: Legend / Silkscreen / Overlay



- Legend or silkscreen:
  - Applied on top of the solder resist
  - Can be applied to one or both outer layers
  - Default color is white but any other color is possible

Tip: add (Top) and (Bottom)

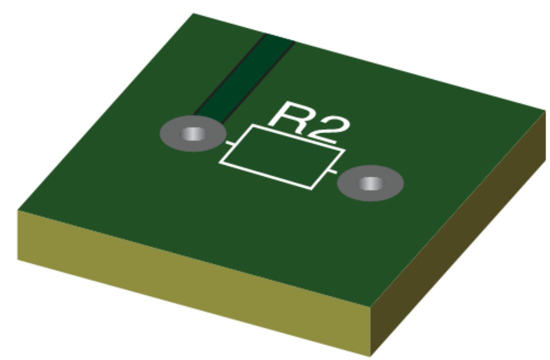
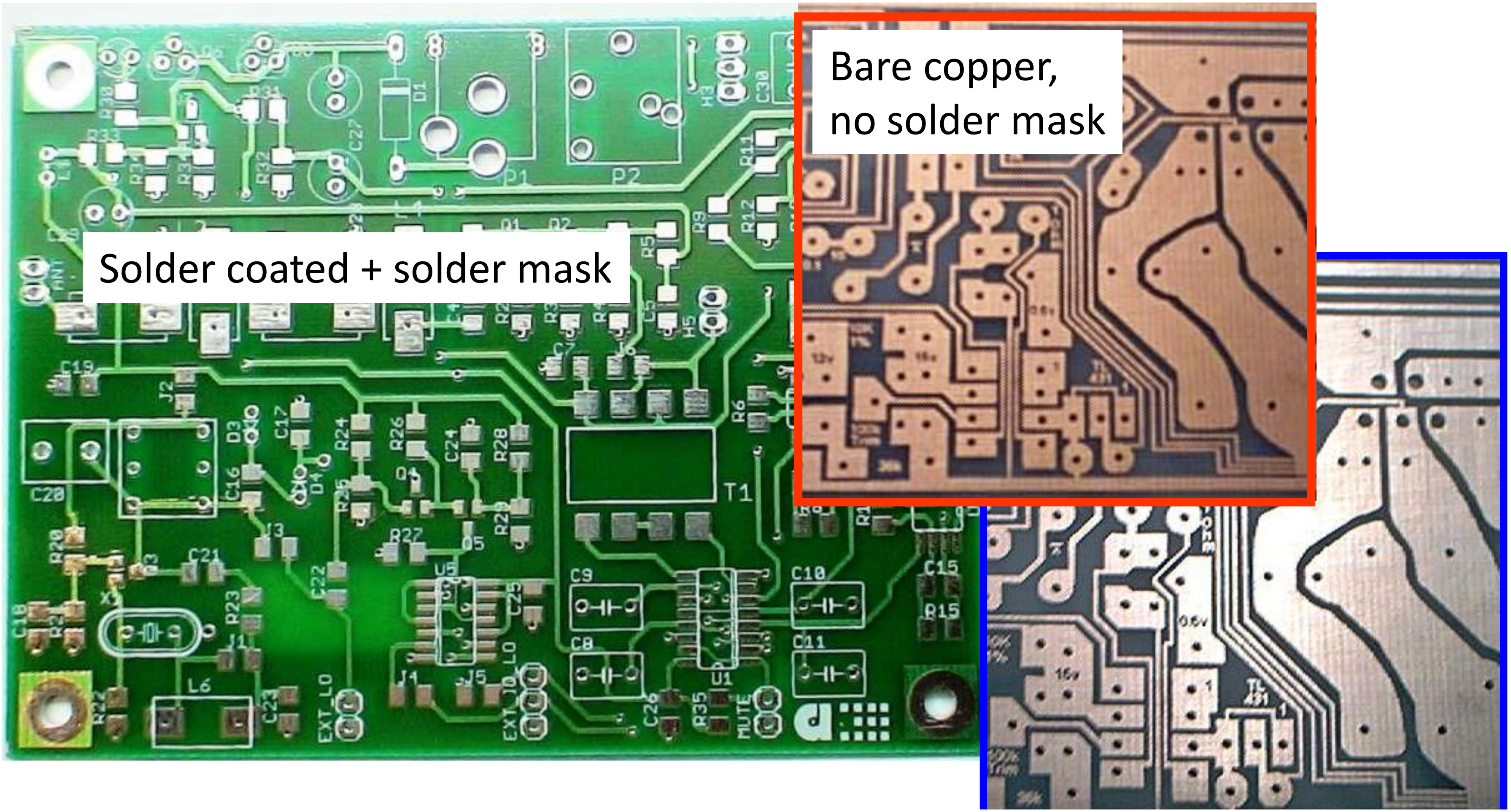


Figure 1-16 Final layers are the soldermask (green) and silk screen (white).

PCB Anatomy: Solder coat / thinning



Solder coated + no solder mask

PCB Anatomy: Mechanical Layers

- Multi-purpose layers
- E.g. Altium supports 32 Mechanical layers: M1 … M32
- Typically
  - <u>M1   Board outline</u>
  - M2   PCB manufacturing info
  - M11-M12 Top and bottom layer dimensions
  - M13 Top layer 3D models and mechanical outlines
  - M14 Bottom layer 3D models and mechanical outlines
  - M15 Top layer assembly information
  - M16 Bottom layer assembly information

PCB Design Best Practices

Best Practices: Estimating board size

- Before starting layout it is good to have an idea of the target size of the PCB board and all other relevant dimensions.

- It is very helpful to have the components at hand to plan the floor-plan.

- An old good trick of the trade is to print the PCB layout at a 1:1 scale, place the printout on a foam and stick on the through hole components.

Best Practices: Floor planning

- Choose your units and set the grid
- Carefully plan the placement of components
  - Place analog and digital sections apart
  - Group components into ‘functional blocks’
  - Place ICs in the same direction
  - Align ICs, resistors, labels, capacitors etc.
  - Place de-caps close by their ICs
  - Place Op-amp resistors near the Op-amp
  - Plan for mounting holes and heat sinks
- Aim for symmetry when possible
- Do use Design Rule check

Best Practices: Routing strategy

- On two sided boards keep traces perpendicular as much as possible
- Avoid 90 degree bends in tracks
- Keep traces a short as possible
- Always connect a trace to the center of the pad
- Use teardrops (Tools >> tear drops), and use vias to avoid lockout
- Do not place vias under SMD pads
- Layout first all critical traces

  e.g. CLK, diff pairs, controlled length

- Polygons as fills:

  Connect to GND, do not leave 'dead copper'

Best Practices: Labelling

- Always sign your design: add date, and name of board
- Label all relevant inputs and outputs
- Default sizes for comments and designators are 60mils x 10mils
- If you have silkscreen on both sides add a 'TOP' label to the top overlay.

Best Practices: Finishing touches

- Add mounting holes
- Run: Reports >> Board Information
  - Board specification → to confirm board size
  - Non-plated hole size
  - Plated hole size
- Using the hole size editor:
  - Minimize the total number of holes sizes
  - Verify that all vias are the same size (if possible)
- Verify that there are no unwanted leftovers on any Mechanical layer

Online resources

- Ten best practices of PCB design – EDN Magazine, Edwin Robledo & Mark Toth
- Circuit Board Layout Techniques – Texas Instruments, Chapter 17 of Op-amps for everyone
- PCB Design Tutorial – David L. Jones