



Altium II

(PCB Layout)

ELEC391
Spring 2017

PCB Design support for ELEC391:

Altium 2016, 150 licenses

Lecture talks:

- Jan 30 Altium I (Design Capture + Simulation)
- Feb 6 Altium II (PCB Layout)
- Mar 13 Guest Lecture – PCB Production
- Support & submission instructions posted [here](#)

Mechanical and PCB design support available 2hrs per lab session,
rooms MCLD315,306

Mon: 13:00-15:00 / 16:00-18:00

Tue : 09:00-11:00 / 12:00-14:00 / 16:00-18:00

Wed: 13:00-15:00 / 16:00-18:00

Tue : 09:00-11:00 / 12:00-14:00 / 16:00-18:00

Contents

- PCB design flow & PCB layers
- Walk-through tutorial, simple PCB
- Instructions for elec391 fab submissions
- PCB design best practices
- Anatomy of a PCB
 - Traces, pads, vias, layers etc.

PCB Basic Design Flow

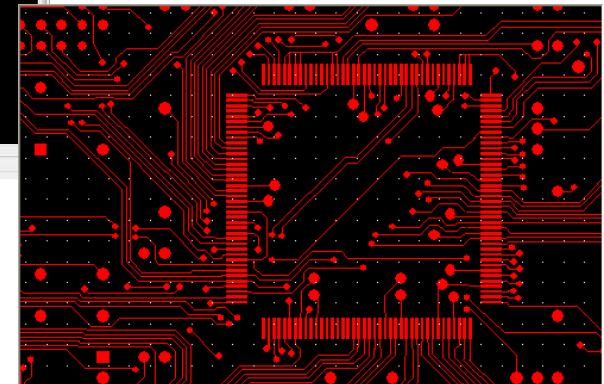
Schematic entry

PCB Layout

- Gerber: 274X
 - Top, Bottom Cu
 - Top, Bottom Solder
 - Silkscreen
 - Mechanical 1
- Drill files (tool list)

CAM files

- Symbol and Footprint creation
- Auto place
- Auto route ...



2 starting points for PCB design

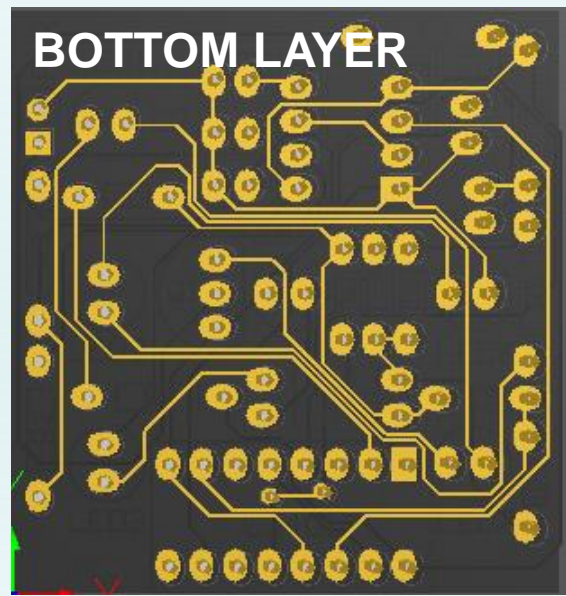
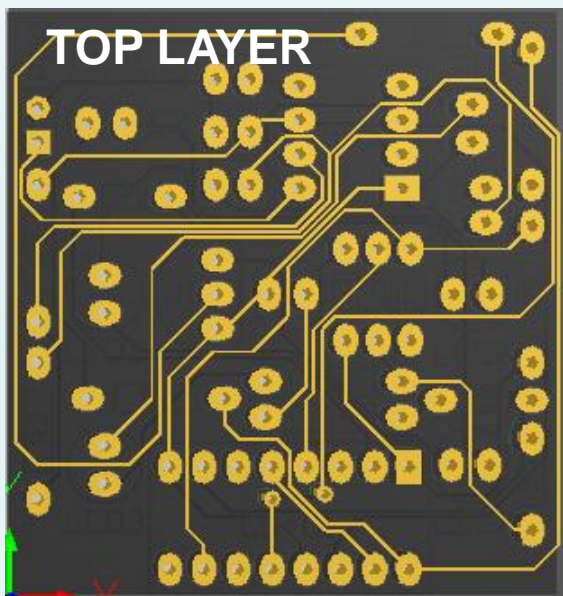
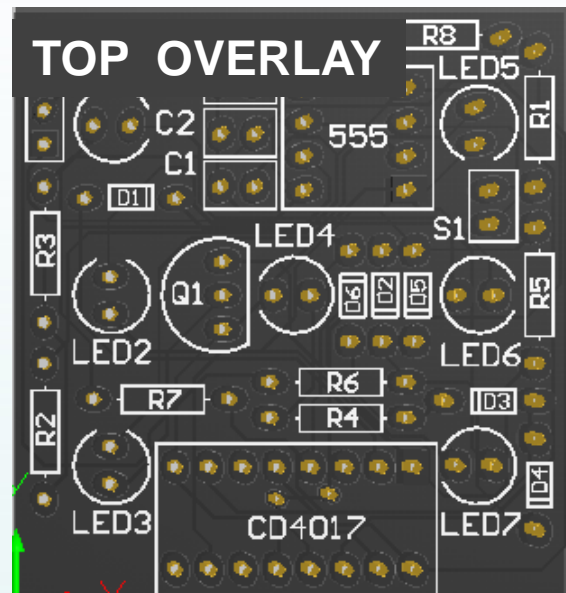
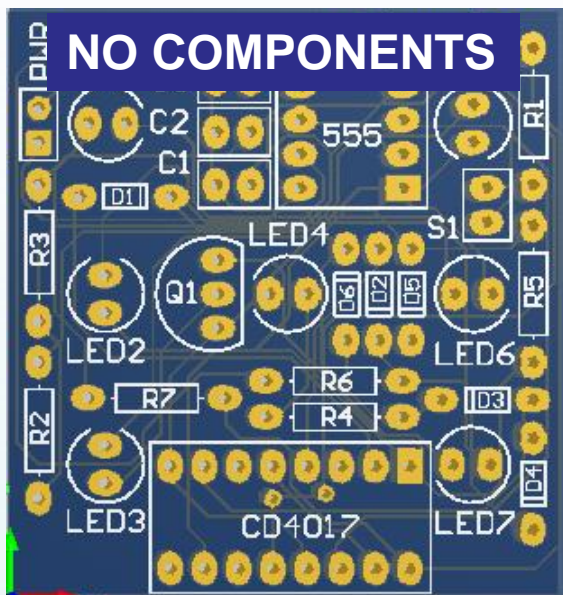
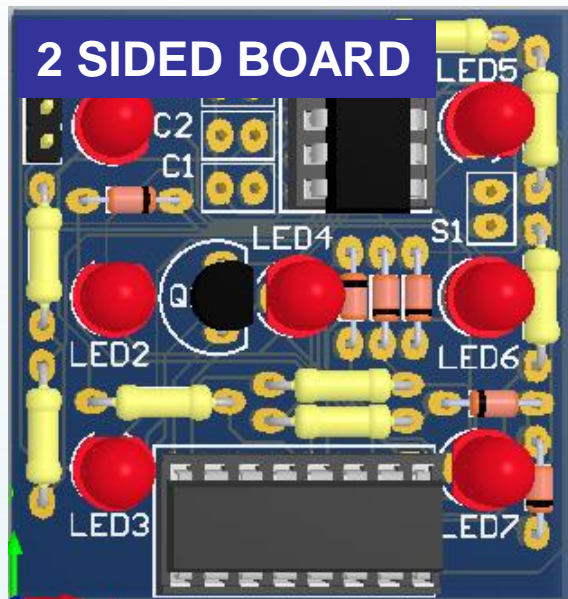
1. From a companion schematic package

- Prepare project schematics
- Import schematic design
- Component footprints are added automatically
- Connectivity is indicated with rats nests
- Net names are imported from the schematic

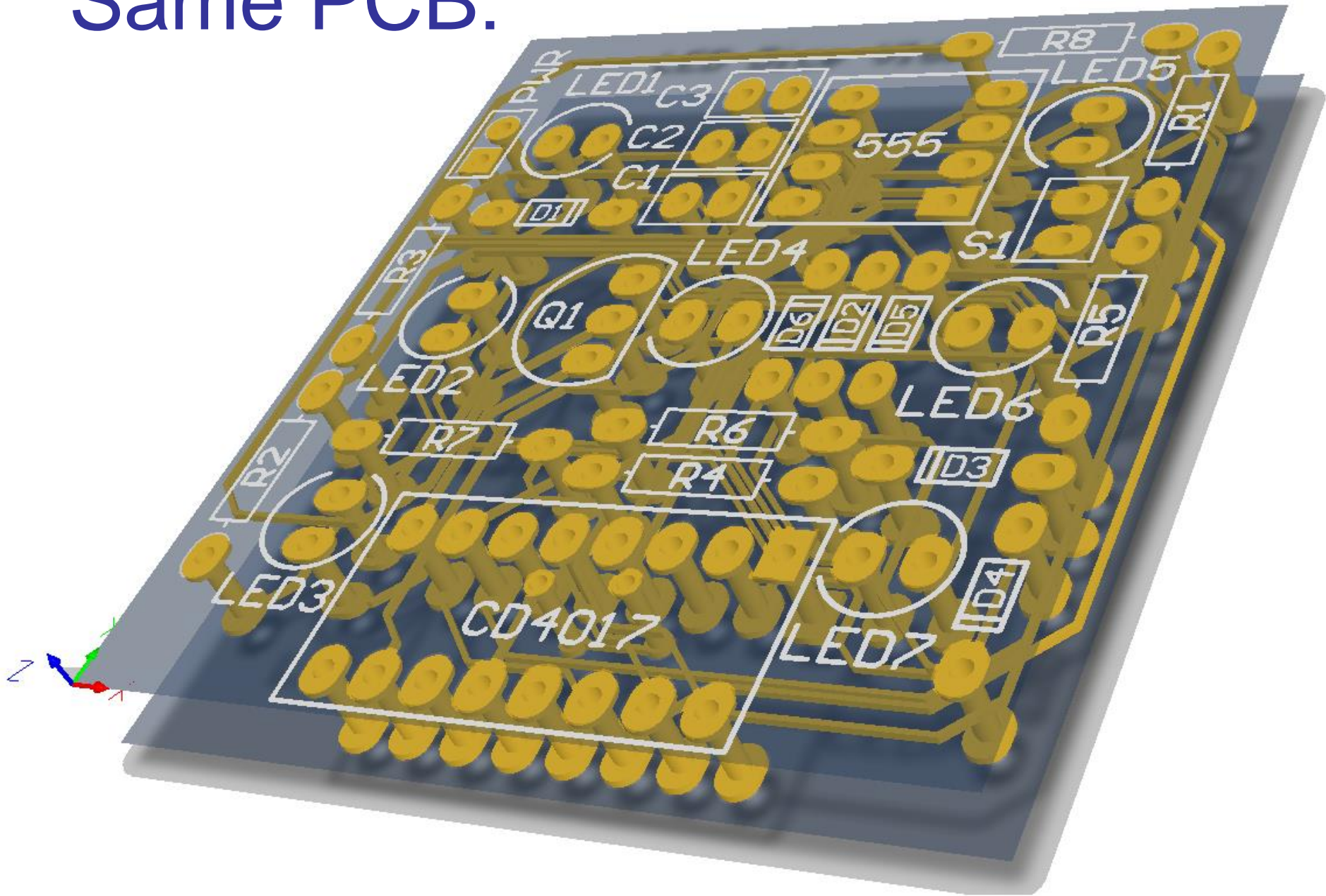
2. Directly from the PCB editor

- You need to select and place manually each component footprint from a library
- No rats nest – connectivity
- You must assign nets manually (at least GND)

PCBs are multi-layered entities



Same PCB:



Configuring the Display Layers

- Design » Board Layers and Colors

View Configurations

Select PCB View Configuration

Name	Kind
Altium Standard 2D	2D simple
Altium Transparent 2D	2D simple
Tutorial	2D simple
Altium 3D Black	3D
Altium 3D Blue	3D
Altium 3D Brown	3D
Altium 3D Color By Layer	3D
Altium 3D Dk Green	3D
Altium 3D Lt Green	3D
Altium 3D Red	3D
Altium 3D White	3D

Path
C:\Users\robertor\AppData\Roaming\Altium\Altium Designer (24F8ECA1-33DC-412A-808C-0336F88BC8A6)\View Configurations\Altium Standard 2D.config_2dsimple

[Explore Folder ...](#)

Description
Altium Standard 2D

Actions

[Create new view configuration ...](#)

[Save view configuration](#)

[Save As view configuration ...](#)

[Load view configuration ...](#)

[Rename view configuration ...](#)

[Remove view configuration...](#)

Board Layers And Colors | Show / Hide | View Options | Transparency

Signal Layers (S)	Color	Show	Internal Planes (P)	Color	Show	Mechanical Layers(M)	Color	Show	Enable	Single Layer Mode	Linked To Sheet
Top Layer (T)	Red	<input checked="" type="checkbox"/>				Mechanical 1	Magenta	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Bottom Layer (B)	Blue	<input checked="" type="checkbox"/>				Mechanical 13	Magenta	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
						Mechanical 15	Green	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
						Mechanical 16	Black	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Only show layers in layer stack Only show planes in layer stack Only show enabled mechanical Layer

[All On](#) [All Off](#) [Used On](#) [All On](#) [All Off](#) [Used On](#) [All On](#) [All Off](#) [Used On](#)

Mask Layers (A)	Color	Show	Other Layers (O)	Color	Show	System Colors (Y)	Color	Show
Top Paste	Grey	<input type="checkbox"/>	Drill Guide	Brown	<input type="checkbox"/>	Default Color for New Nets	Blue	<input checked="" type="checkbox"/>
Bottom Paste	Brown	<input type="checkbox"/>	Keep-Out Layer	Magenta	<input type="checkbox"/>	DRC Error Markers	Green	<input checked="" type="checkbox"/>
Top Solder	Purple	<input checked="" type="checkbox"/>	Drill Drawing	Red	<input type="checkbox"/>	Selections		<input checked="" type="checkbox"/>
Bottom Solder	Magenta	<input checked="" type="checkbox"/>	Multi-Layer	Grey	<input checked="" type="checkbox"/>	DRC Detail Markers		<input checked="" type="checkbox"/>

[All On](#) [All Off](#) [Used On](#) [All On](#) [All Off](#) [Used On](#) [All On](#) [All Off](#) [Used On](#)

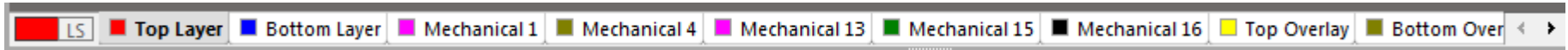
Silkscreen Layers (K)	Color	Show
Top Overlay (E)	Yellow	<input checked="" type="checkbox"/>
Bottom Overlay (R)	Olive	<input checked="" type="checkbox"/>

[All On](#) [All Off](#) [Used On](#)

[All Layers On](#) [All Layers Off](#) [Used Layers On](#) [Selected Layers On](#) [Selected Layers Off](#) [Clear All Layers](#)

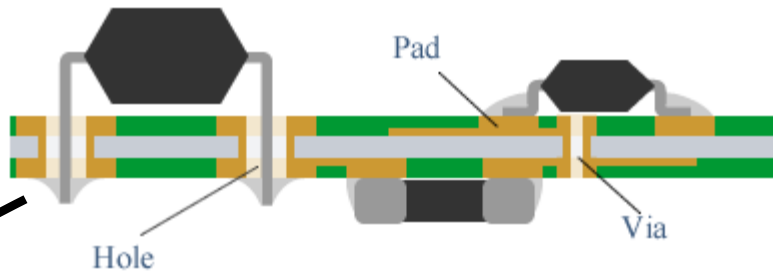
2D Color Profiles Layer Pairs ... OK Cancel Apply

Configuring the Display Layers



- **Electrical layers**
32 signal layers and 16 internal power plane layers.
- **Mechanical layers**
32 general purpose mechanical layers, used for design tasks such as dimensions, fabrication details, assembly instructions, or special purpose tasks such as glue dot layers. These layers can be selectively included in print and Gerber output generation. They can also be paired, meaning that objects placed on one of the paired layers in the library editor, will flip to the other layer in the pair when the component is flipped to the bottom side of the board.
- **Special layers**
these include the top and bottom silkscreen layers, the solder and paste mask layers, drill layers, the Keep-Out layer (used to define the electrical boundaries), the multilayer (used for multilayer pads and vias), the connection layer, DRC error layer, grid layers, hole layers, and other display-type layers.

Thru-hole pads & vias are plated



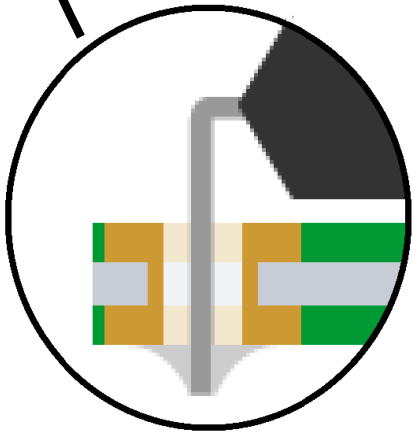
<http://hobbygenius.co.uk/tutorials/pcbdesign/1510>

Plating reduces hole size by 0.003"

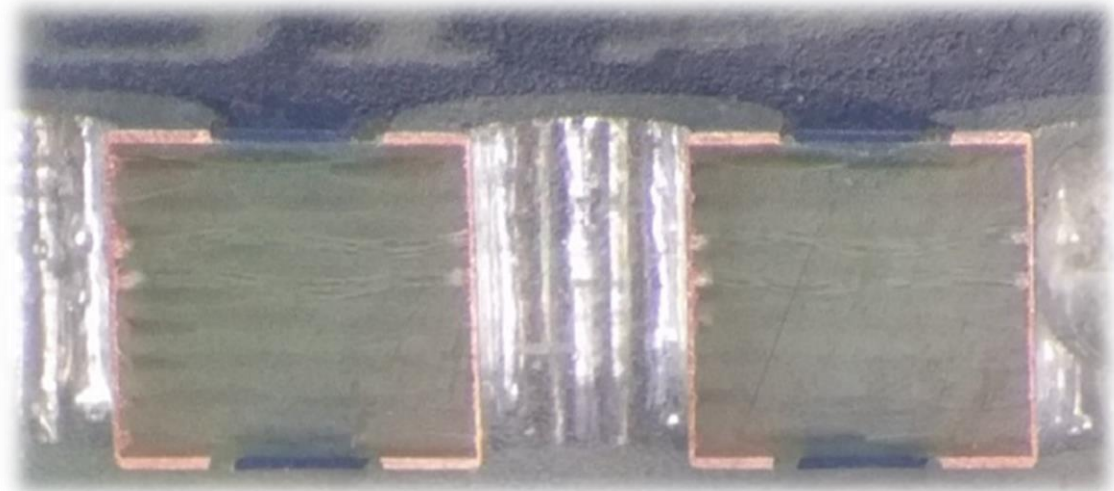
You must specify if using

- 1) Plated hole sizes
- 2) Non plated hole sizes

Not all holes need to be plated



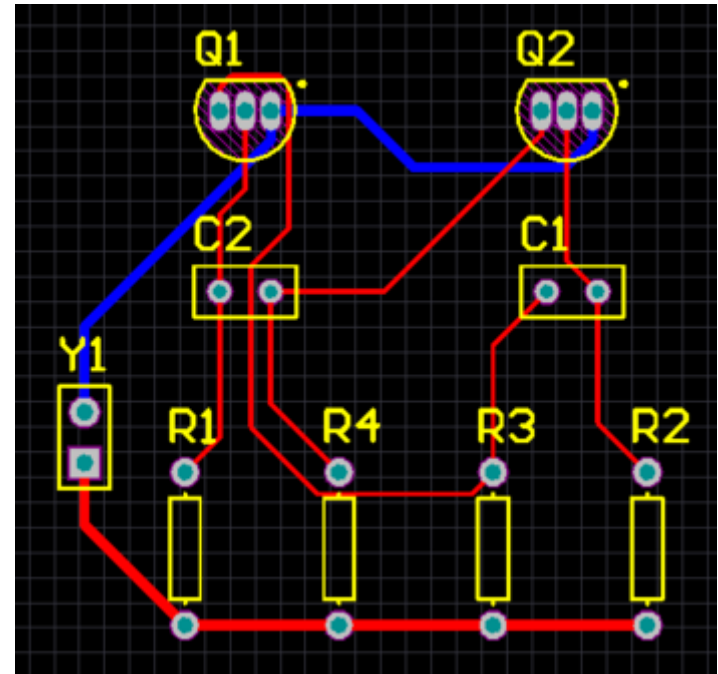
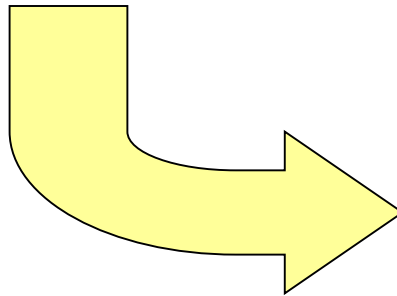
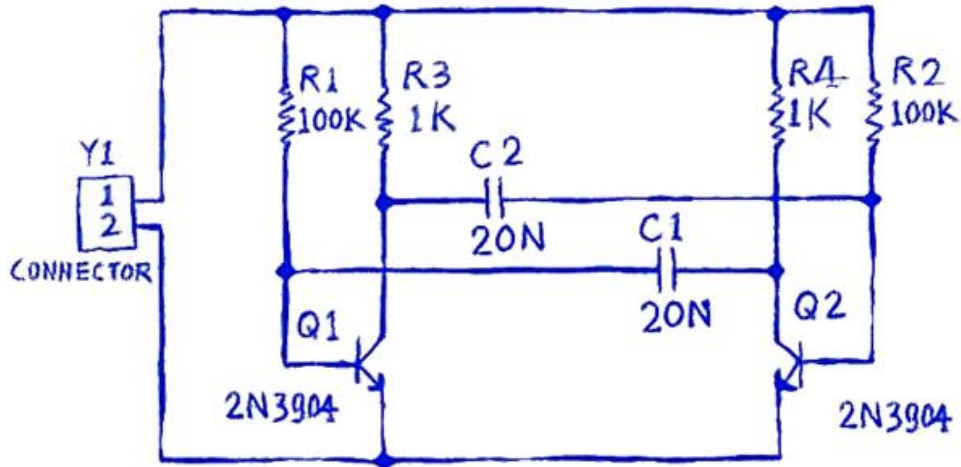
Cross section report for a 2 sided PCB



Board Implementation

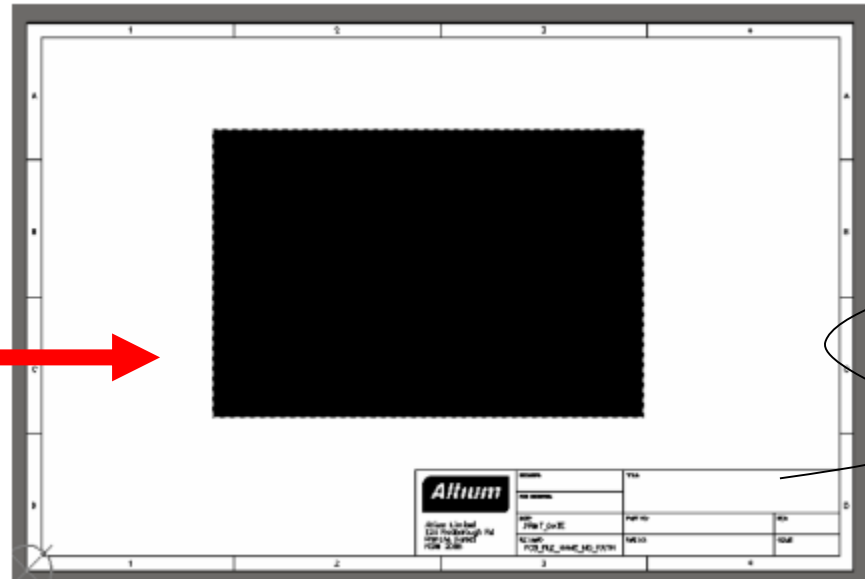
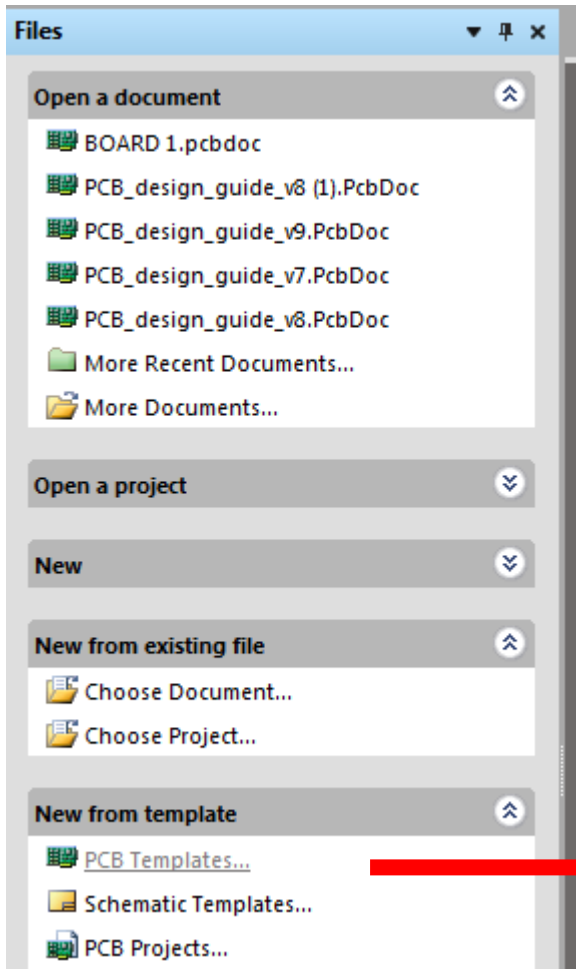
Tutorial - Getting Started with PCB Design

<http://techdocs.altium.com/display/ADOH/Board+Implementation>



Creating a New Board from a template

- Files Panel:
 - New from template
 - select the A4.PcbDoc template
 - Save as ... same name and directory as SchDoc file

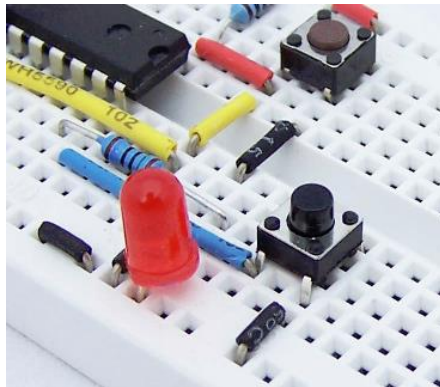


Mechanical 16

First things first ... choosing working units

- Imperial (inches)

- 1/1000th of an inch = 1 mil = 1thou
- 100mils (0.1") is a common dimension



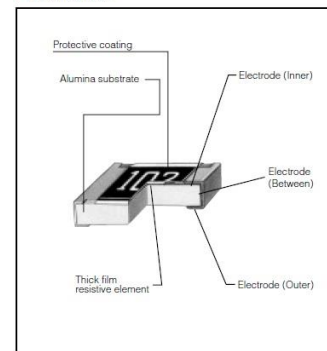
- Metric (mm)

- 1 mm ≠ 1mil !
- Common unit in SM parts

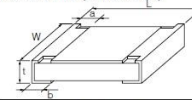
Panasonic

Thick Film Chip Resistors

Construction



Dimensions in mm (not to scale)



Type (inches)	Dimensions (mm)					Mass (Weight) (g/1000 pcs.)
	L	W	a	b	t	
ERJ6S (01005)	0.40 ^{+0.02}	0.20 ^{+0.02}	0.10 ^{+0.02}	0.10 ^{+0.02}	0.13 ^{+0.02}	0.04
ERJ6G (02011)	0.60 ^{+0.03}	0.30 ^{+0.03}	0.10 ^{+0.03}	0.15 ^{+0.03}	0.23 ^{+0.03}	0.15
ERJ6G (0402)	1.00 ^{+0.04}	0.50 ^{+0.04}	0.20 ^{+0.04}	0.25 ^{+0.04}	0.35 ^{+0.04}	0.8
ERJ3G (0603)	1.60 ^{+0.06}	0.80 ^{+0.06}	0.30 ^{+0.06}	0.30 ^{+0.06}	0.45 ^{+0.06}	2
ERJ6G (0805)	2.00 ^{+0.08}	1.25 ^{+0.08}	0.40 ^{+0.08}	0.40 ^{+0.08}	0.60 ^{+0.08}	4
ERJ6G (1206)	3.20 ^{+0.12}	1.60 ^{+0.12}	0.50 ^{+0.12}	0.50 ^{+0.12}	0.60 ^{+0.12}	10
ERJ14 (1210)	3.20 ^{+0.20}	2.50 ^{+0.20}	0.50 ^{+0.20}	0.50 ^{+0.20}	0.60 ^{+0.20}	16
ERJ12 (1812)	4.50 ^{+0.20}	3.20 ^{+0.20}	0.50 ^{+0.20}	0.50 ^{+0.20}	0.60 ^{+0.20}	27
ERJ12Z (2010)	5.00 ^{+0.20}	2.50 ^{+0.20}	0.60 ^{+0.20}	0.60 ^{+0.20}	0.60 ^{+0.20}	27
ERJ1T (2512)	6.40 ^{+0.20}	3.20 ^{+0.20}	0.65 ^{+0.20}	0.60 ^{+0.20}	0.60 ^{+0.20}	45

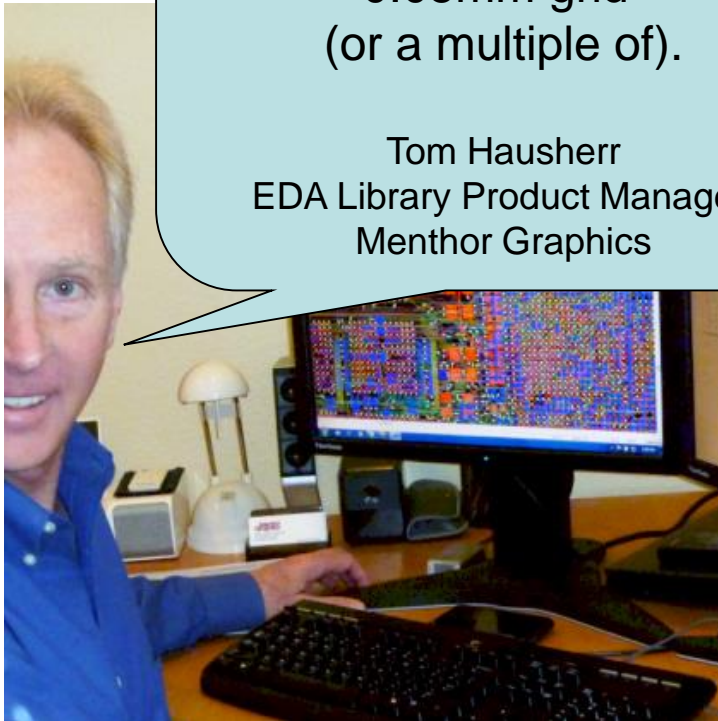
- Remember: 100mils = 2.54mm

- To switch units in Altium Press <Q>

Metric or Imperial?

"every element in a PCB design should reside on a 0.05mm grid" (or a multiple of).

Tom Hausherr
EDA Library Product Manager,
Mentor Graphics



Comment driven by high density & modern surface mount technology

Old PCB wisdom:
"thou shall use thous"

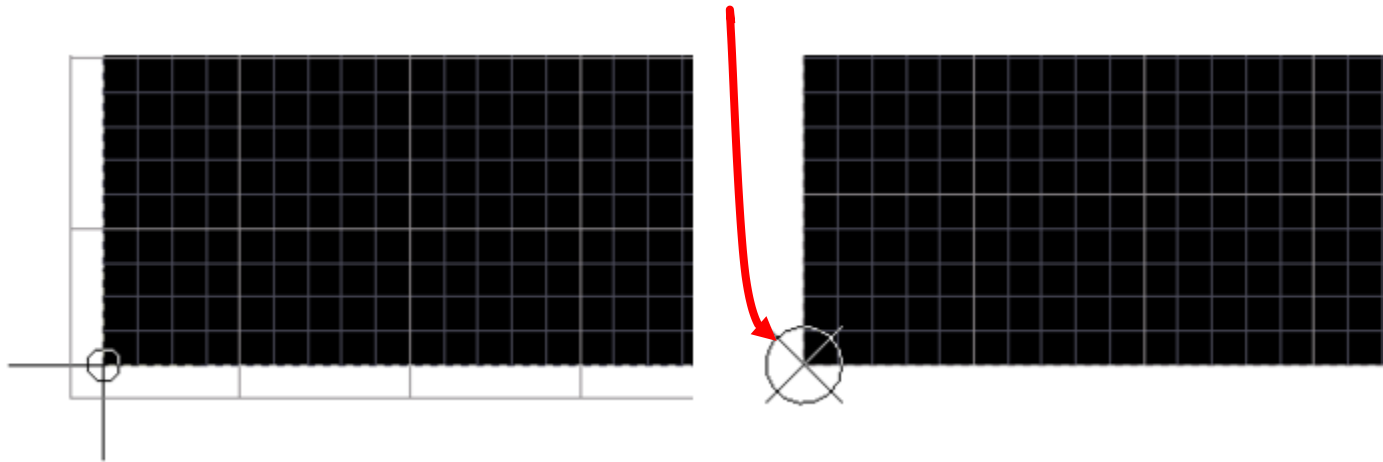
David L. Jones
EEV blog



Comment driven by traditional 0.1" spacing between pins

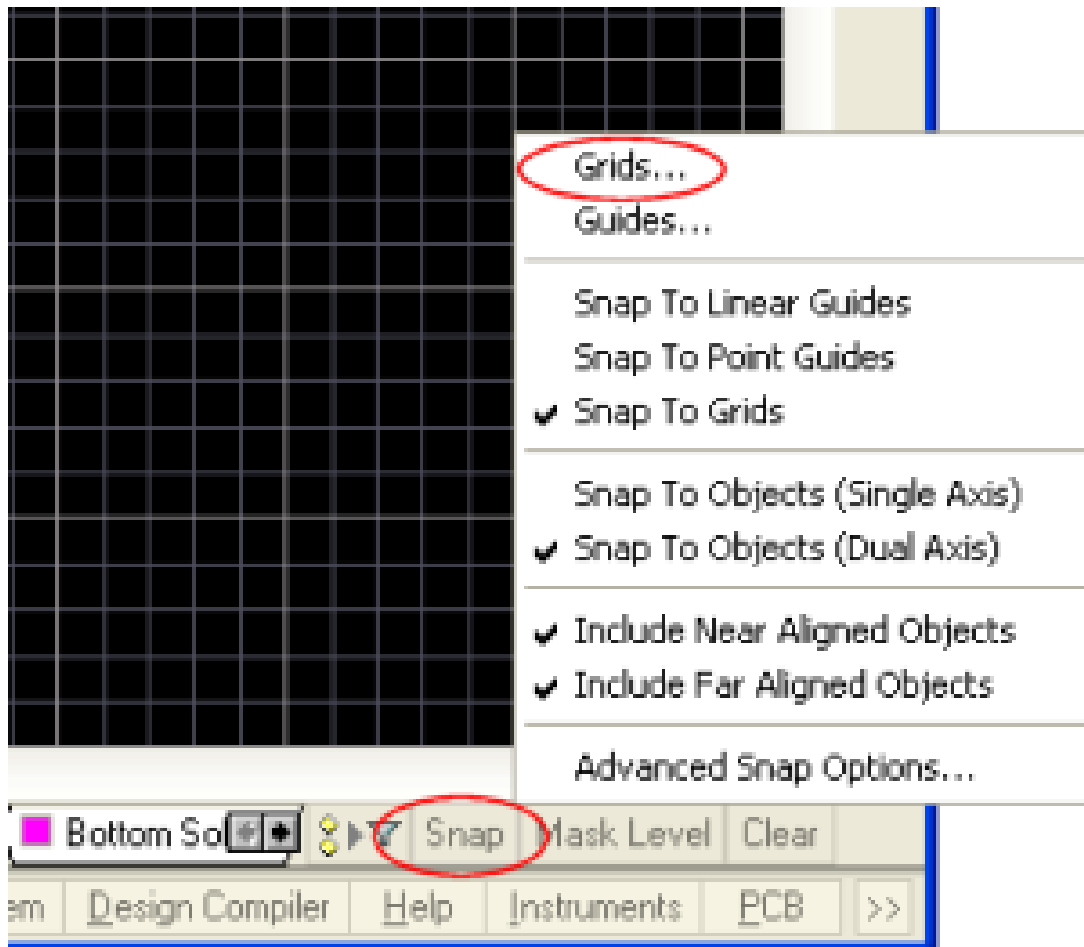
First things first ... setting the board origin

- Absolute origin (lower left corner)
- User-defined relative origin
 - Edit >> Origin >> Set



First things first ... setting the snap grid

- PCBs are grid based objects

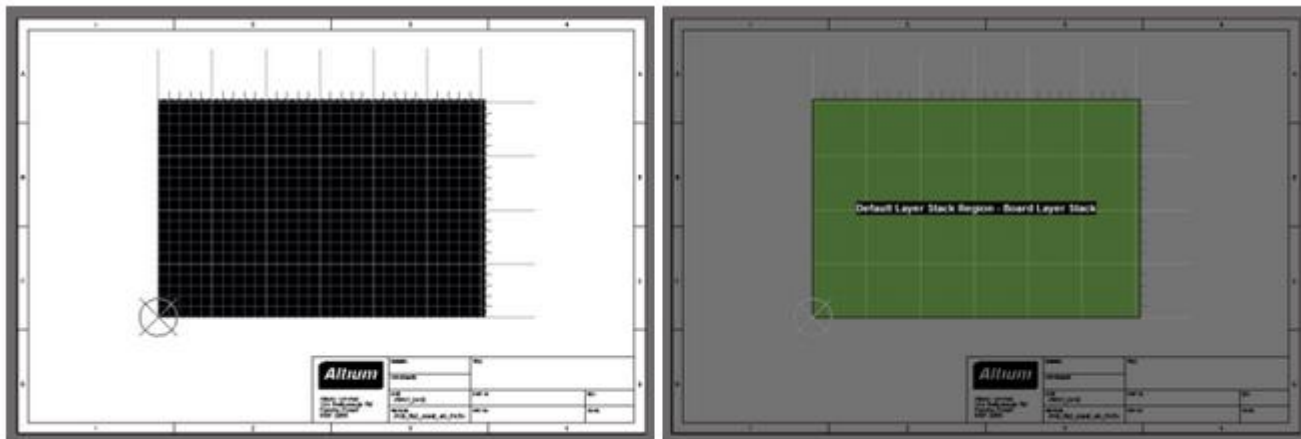


Unified Cursor-Snap System

- Selecting a suitable snap grid:
 - <Ctrl>+<G>
 - Start with a coarse grid to define board size

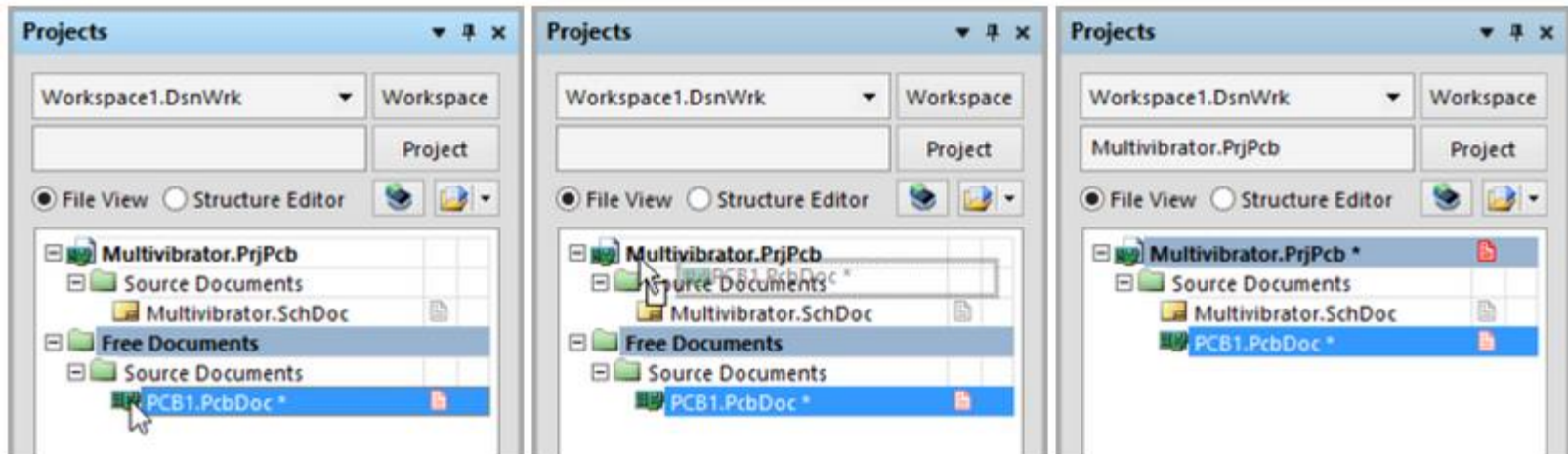
First things first ... redefining the board shape

- Viewing modes:
 - Board Planning Mode (1)
 - **Design » Edit Board Shape** (resize to 1.5" x 1.5")
 - **Design >> Move Board Shape** (Relocate the origin)
 - 2D Layout Mode (2)
 - 3D Layout Mode (3).



Design transfer

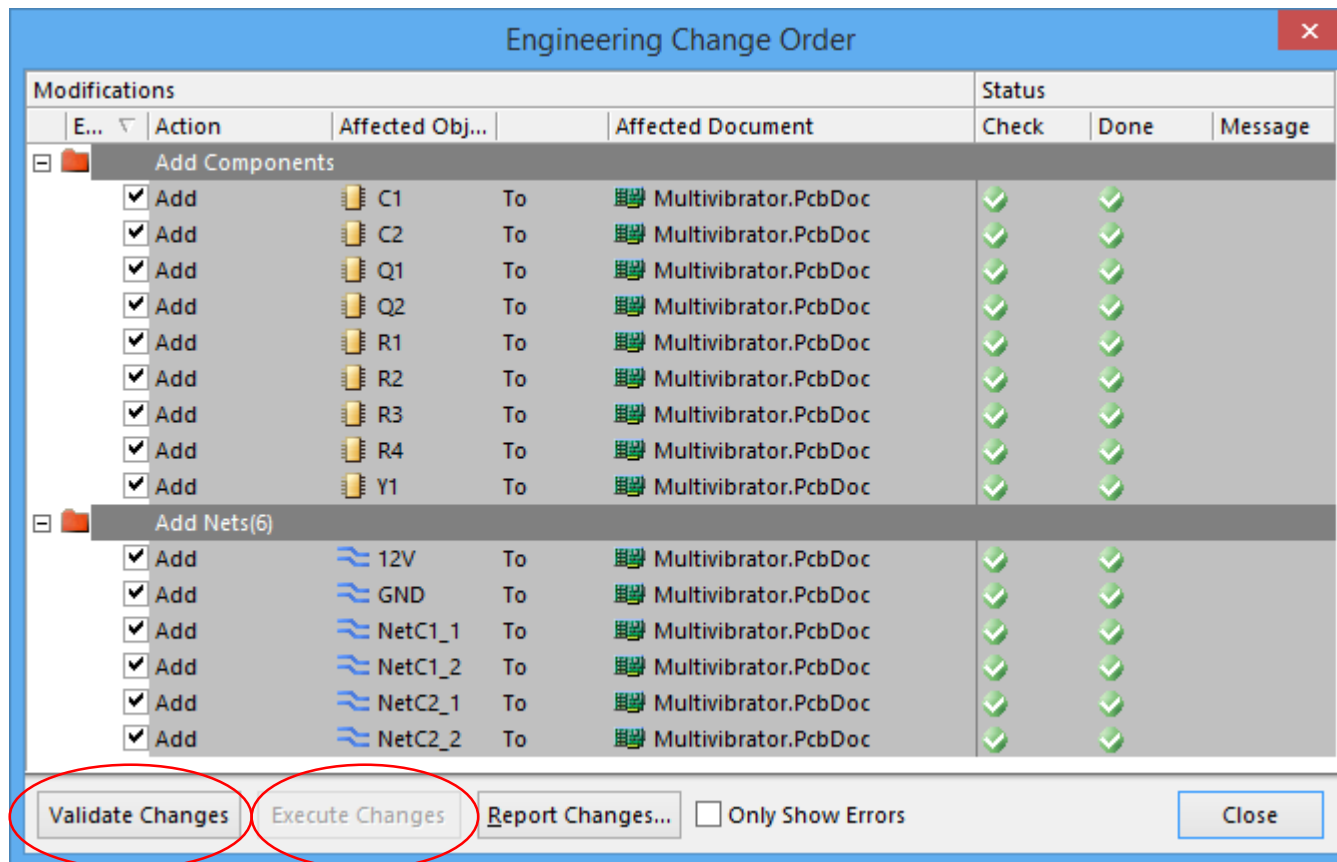
- Make the PCB board part of the project



- Rename the file
- Save the PcBDoc file and the project

Design transfer

- Design transfer
 - On Schematic file
 - Design >> Update PCB Document ...



Design transfer

Multivibrator.SchDoc Multivibrator.PcbDoc *

All parts in the schematic with their selected footprints

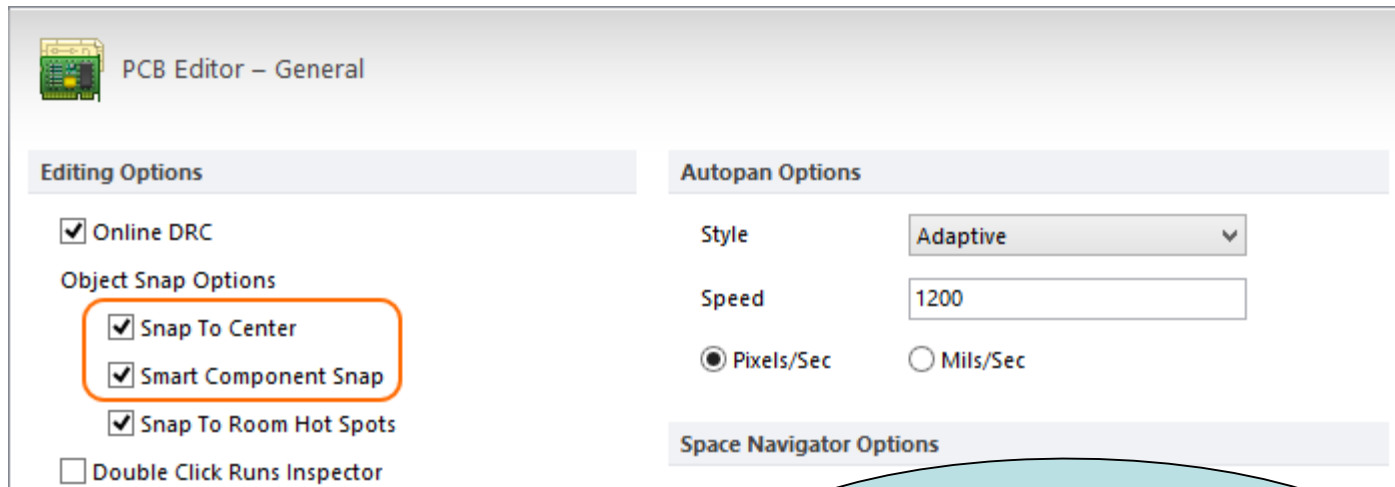
Q2 Q1 C2 Y1 C1 R1 R3 R4 R2

Rat's nests indicate connectivity as per schematic (Net names are assigned to part terminals)

LS Top Layer Bottom Layer Mechanical 13 Mechanical 15 Mechanical 16 Top Overlay Multi-Layer Snap Mask Level Clear

Component positioning and placement options

- Tools >> Preferences



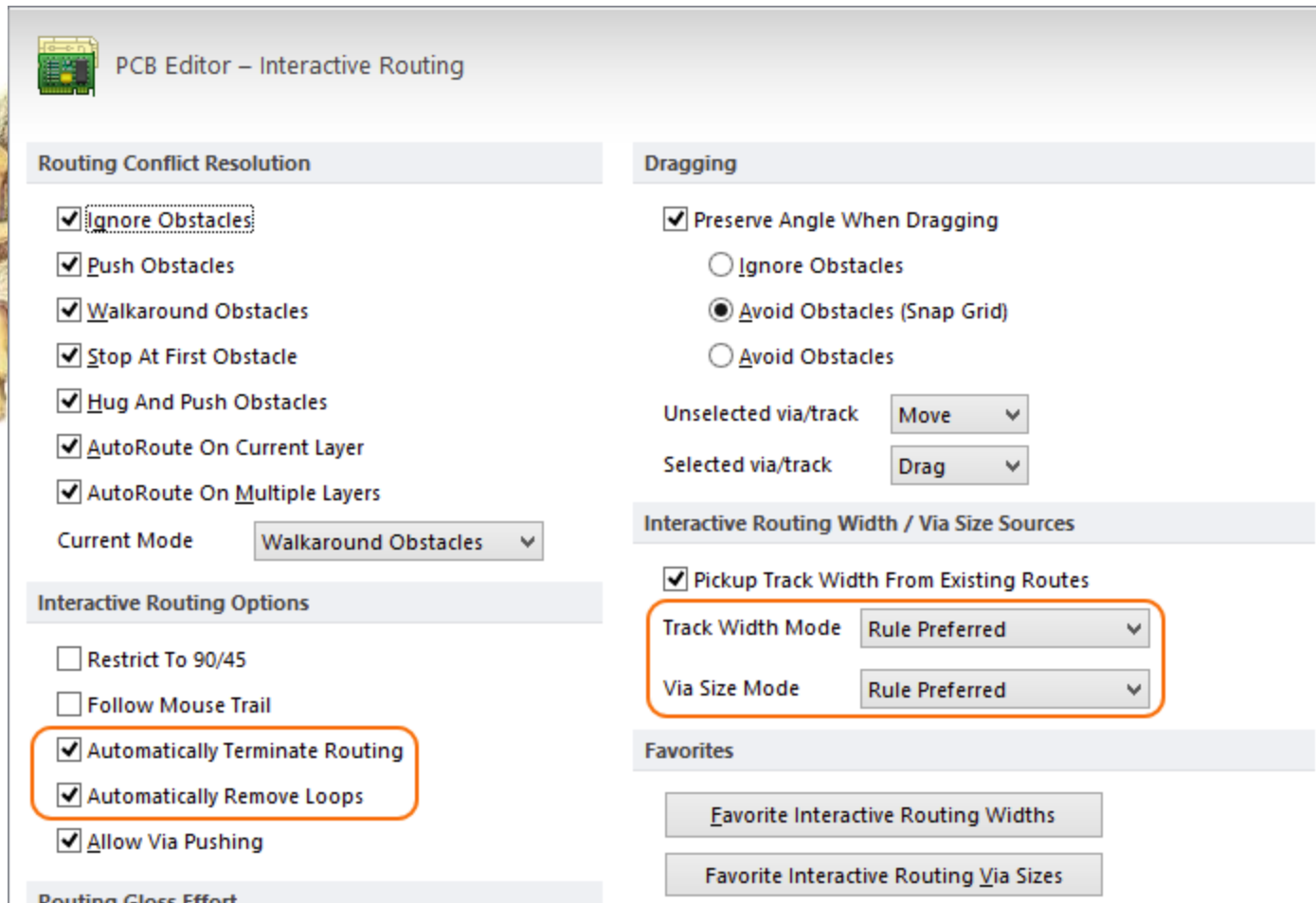
Words of wisdom:
These are very useful!

Snap To Center: When you "grab" a component to position it, the cursor will hold the component by its reference point.

Smart Component Snap force the software to snap to a pad center instead of the reference point

Component positioning and placement options

- Tools >> Preferences



PCB Editor – Interactive Routing

Routing Conflict Resolution

- Ignore Obstacles
- Push Obstacles
- Walkaround Obstacles
- Stop At First Obstacle
- Hug And Push Obstacles
- AutoRoute On Current Layer
- AutoRoute On Multiple Layers

Current Mode: Walkaround Obstacles

Interactive Routing Options

- Restrict To 90/45
- Follow Mouse Trail
- Automatically Terminate Routing
- Automatically Remove Loops
- Allow Via Pushing

Dragging

- Preserve Angle When Dragging
 - Ignore Obstacles
 - Avoid Obstacles (Snap Grid)
 - Avoid Obstacles

Unselected via/track: Move

Selected via/track: Drag

Interactive Routing Width / Via Size Sources

- Pickup Track Width From Existing Routes

Track Width Mode: Rule Preferred

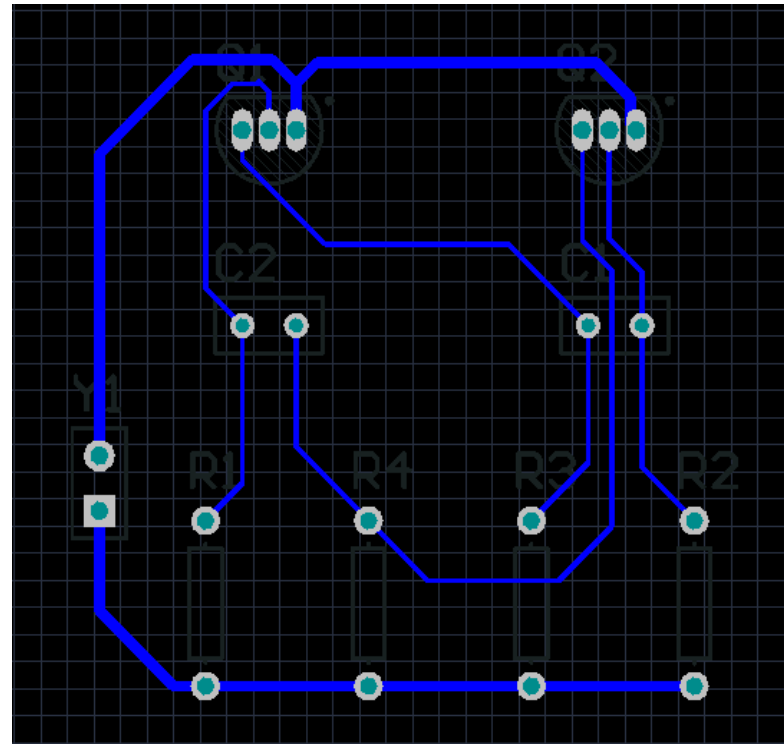
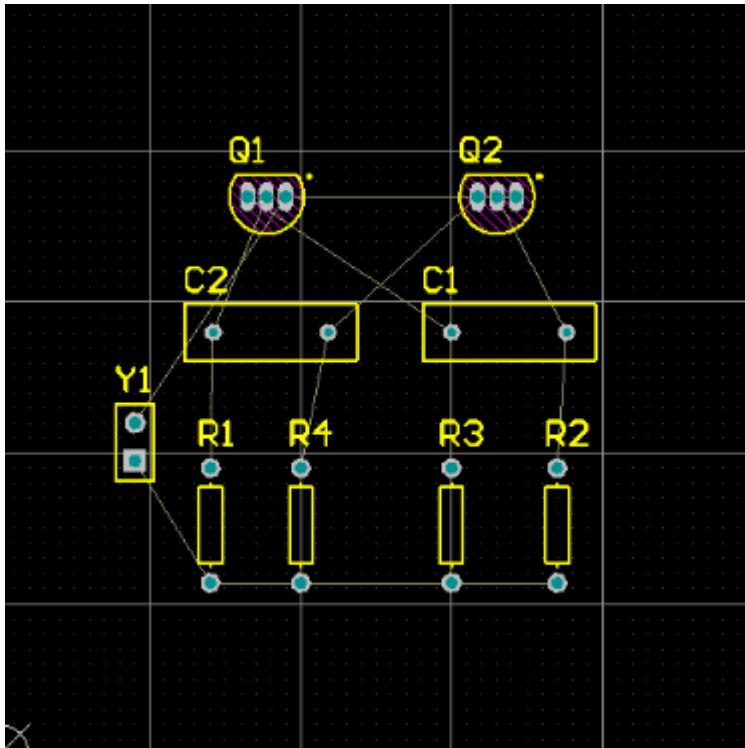
Via Size Mode: Rule Preferred

Favorites

Favorite Interactive Routing Widths

Favorite Interactive Routing Via Sizes

Positioning components & routing



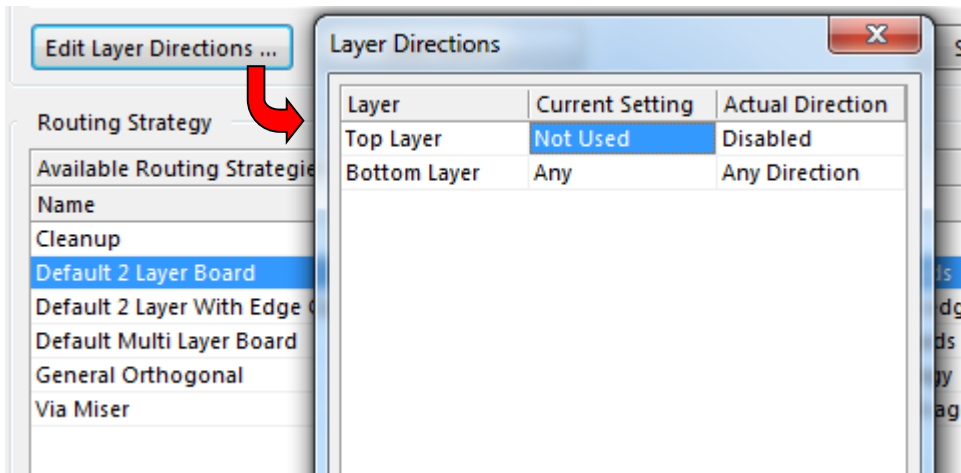
Change C2 & C1 footprints from RAD-0.3 to RAD-0.1
Rotate & align resistors: Edit >> Align

Handy shortcuts for routing

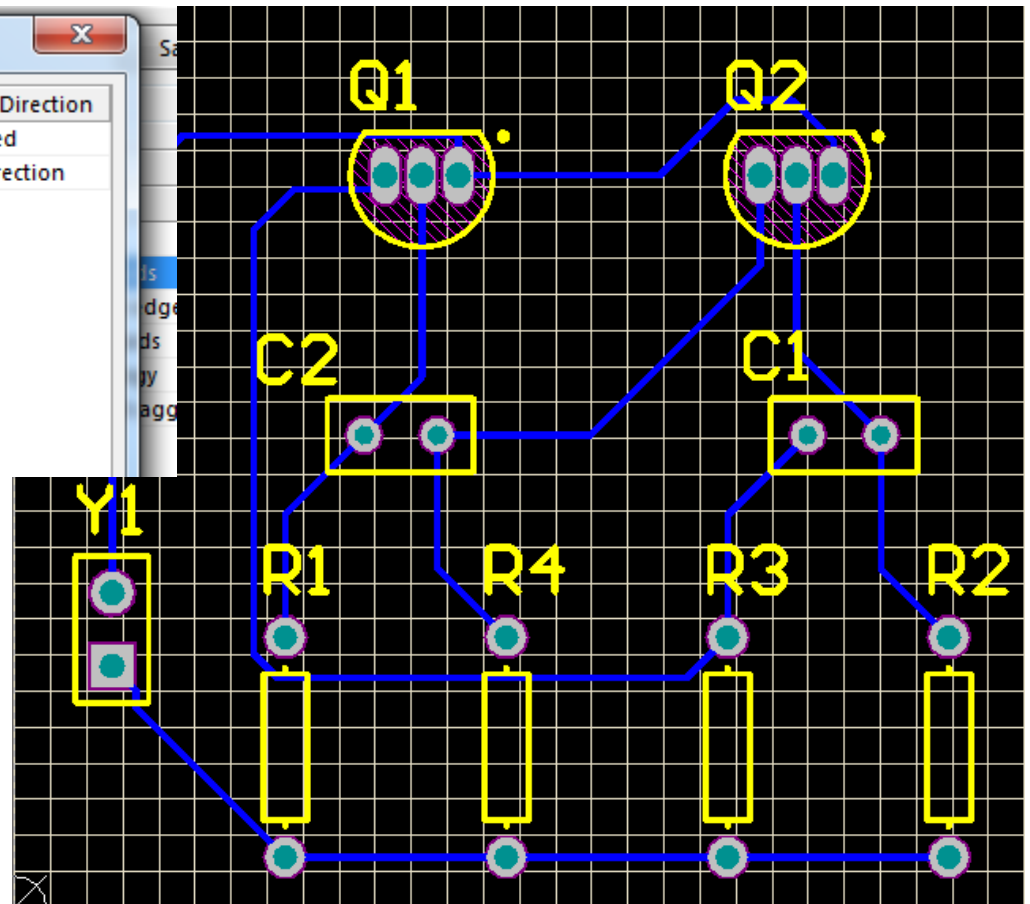
- Press * on the numeric keypad while routing to cycle through the available signal layers. A via will automatically be added, in accordance with the applicable Routing Via Style design rule. Alternatively, use **Ctrl+Shift+Roll** shortcuts to move back and forth through the available signal layers.
- **Shift+R** to cycle through the enabled conflict resolution modes, including Push, Walkaround, Hug and Push, and Ignore. Enable the required modes in the **PCB Editor - Interactive Routing** page of the *Preferences* dialog.
- **Shift+S** to cycle single layer mode on and off, ideal when there are many objects on multiple layers.
- **Spacebar** to toggle the corner direction (for all but any angle mode).
- **Shift+Spacebar** to cycle through the various track corner modes. The styles are: any angle, 45°, 45° with arc, 90° and 90° with arc. There is an option to limit this to 45° and 90° in the **PCB Editor - Interactive Routing** page of the *Preferences* dialog.

Auto route

- Tools » Un-Route » All
- Auto Route » All



- You can set single layer routing



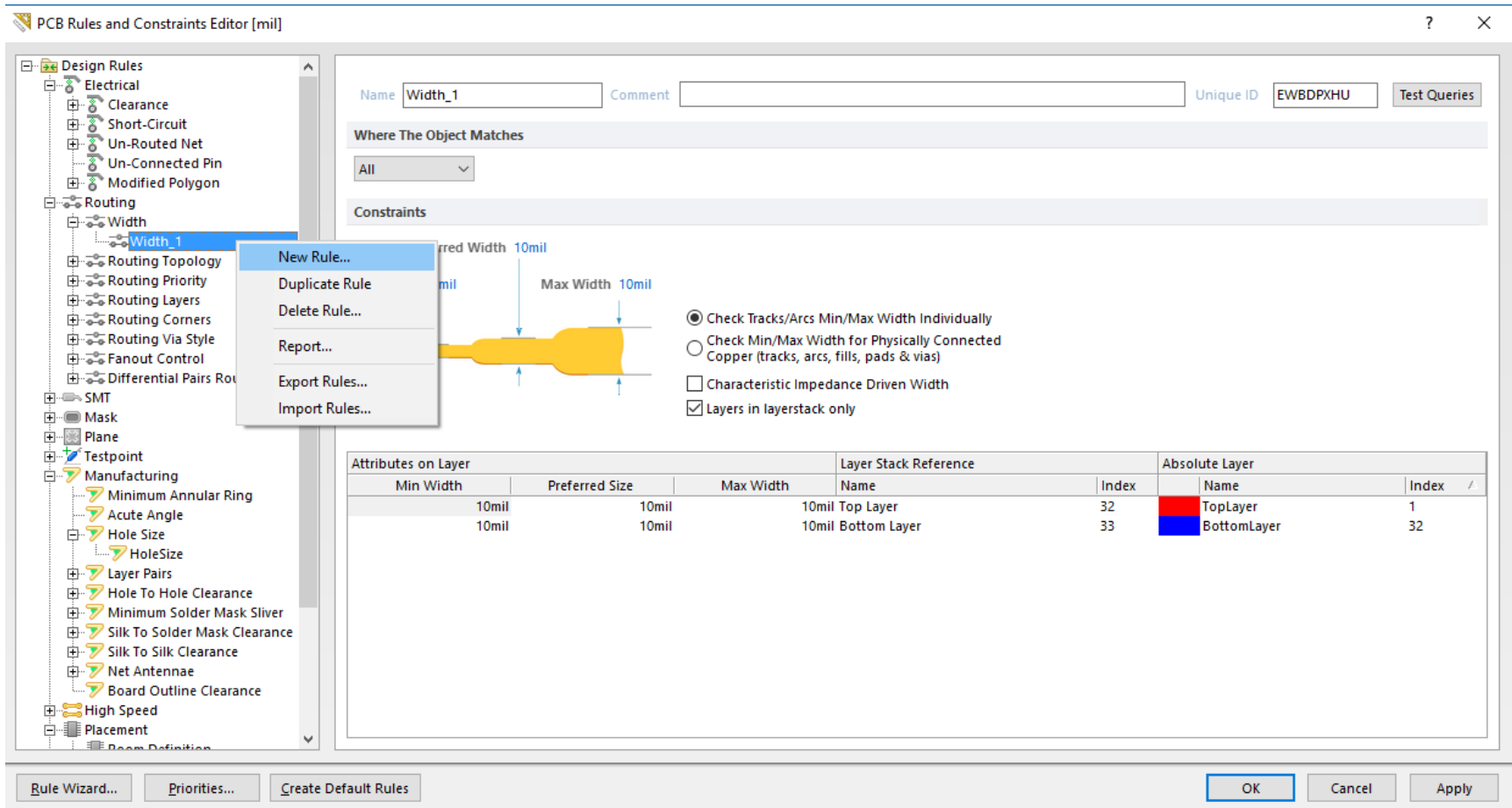
Design Rules

- Design >> Rules

Rule	Constrain	Query
Electrical, Clearance	Min clearance = 10mil	All
Routing, Width*	Min width = 7mils Max width =50mils Preferred =10mils	All
Routing, Width_Power (see next slide)	Min width = 7mils Max width =60mils Preferred =40mils	Advanced (Query) (InNet('12V') OR InNet('GND'))

These rule settings are just for this example, elec391 rules are described ahead

Custom Routing design rules



Rename to "Width_power"

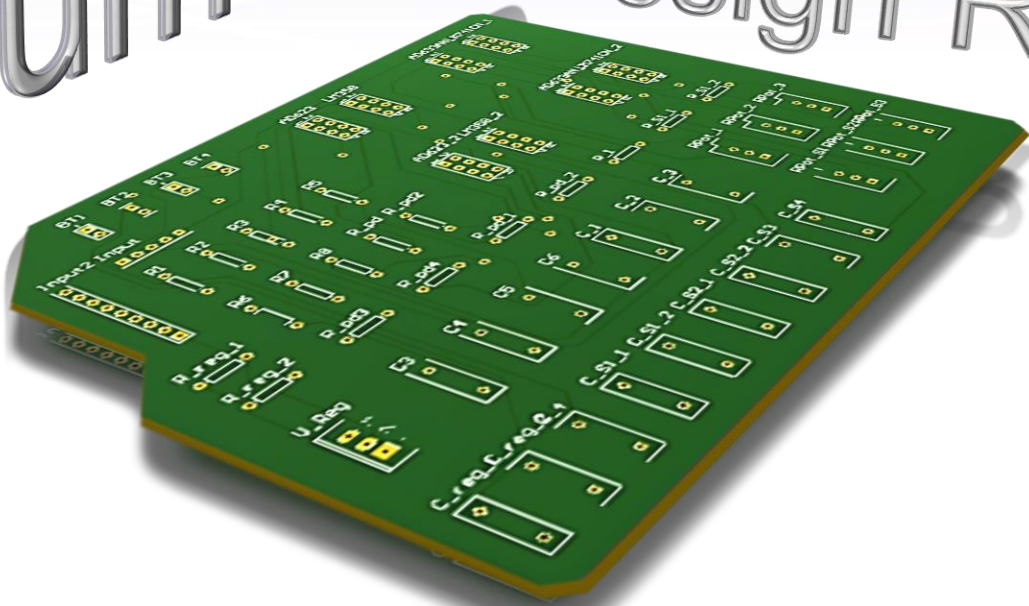
Use 'Custom Query' to set
Belongs to net 12V
OR
Belongs to net GND

Set rule execution
priority

ELEC 391

Altium PCB

Design Rules



Andy

Submission Instructions

- Every group is entitled to **three** submissions
- Cost: \$25 + \$10/ sq-in, from project budget
- Submission dates:

Midnight, every Monday until March 13
we will check submissions and accept fixes
until Tuesday 5PM

- Turn around: 5-6 business days
- Work within the given guidelines
- Verify PCB layout and design - prior to design submission
- Submissions will be rejected if guidelines are not followed

M	T	W	Th	F	Sa	S
M	T	W	Th	F	Sa	S



We will panelize your designs to speed up fabrication and reduce costs

Panelized designs from elec391 Spring 2016

Submission Instructions

- Email pcb@ece.ubc.ca
Subject: [PCB] ELEC391, Group Section #, submission# (out of 3)
- Attach: Zipped file with your PCB Project file (*.PrjPcb) and all associated files, also include the latest DRC report.
(make sure all files are under the same directory)

Body:

Total number of boards to fabricate:

Name of boards to fabricate and number of copies for each

- You can send several different boards per submission.
You can request up to 2 copies of each.

Design constrains

1) Layers:

- 1) Maximum number of electrical layers = 2
- 2) Bottom overlay (PCB underside text) will not be manufactured - please use "bottom layer" for bottom text

2) Try to minimize the size of your PCB

Components can be placed side by side (recommend 50-100 mil IC's separation for most cases)

3) Do not forget to:

Add your group number on the top overlay – make it visible

Draw a board outline on Mechanical 1

if several boards in a single file, draw a board outline for each
(min spacing from edge of board for any feature is 10mils)

Design constrains

4) Use latest version of course component library available [here](http://www.ece.ubc.ca/~eng-services/files/courses/elec391-spring2017/pcb-design/)
<http://www.ece.ubc.ca/~eng-services/files/courses/elec391-spring2017/pcb-design/>

5) Using other libraries

If you do, make sure parts will pass Design-Rule-Checking

These two Altium libraries contain useful parts:

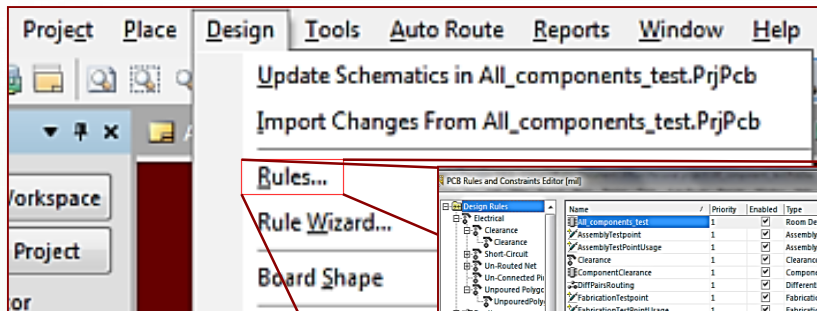
- Miscellaneous Devices.IntLib
- Miscellaneous Connectors.IntLib

6) Install provided Design-Rules file - please do not modify base rules, but you can add custom routing rules.

Submission that do not pass DRC will be rejected

Rules and Checks

1

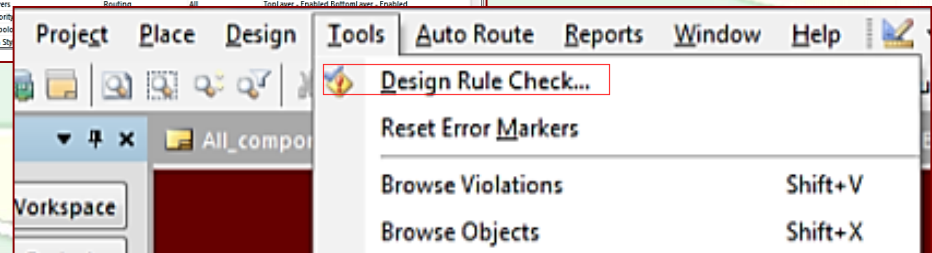


2

PCB Rules and Constraints Editor (mil)

Design Rules	Name	Priority	Enabled	Type	Category	Scope	Attributes
Electrical	All_components_test		<input checked="" type="checkbox"/>	Room Definition	Placement	InComponentClass(# Region (B) = (680mil, 2310mil, (0,5115mil, 21540mil))	Style
Clearance	Clearance	1	<input checked="" type="checkbox"/>	Assembly Testpoint Usage	Testpoint	All	Under Comp - Allow Sides - Top, Bottom Pref Size = 60mil
Clearance	Clearance	1	<input checked="" type="checkbox"/>	Clearance	Electrical	All - All	Clearance = 10mil
Component Clearance	Component Clearance	1	<input checked="" type="checkbox"/>	Component Clearance	Placement	All - All	Horizontal Clearance = 10mil Vertical Clearance = 10mil
Differential Pairs Routing	Differential Pairs Routing	1	<input checked="" type="checkbox"/>	Differential Pairs Routing	Routing	All	Pref Gap = 10mil Min Gap = 10mil Max Gap = 10milPref
Fabrication Testpoint	Fabrication Testpoint	1	<input checked="" type="checkbox"/>	Fabrication Testpoint Usage	Testpoint	All	Under Comp - Allow Sides - Top, Bottom Pref Size = 60mil
Fabrication Testpoint Usage	Fabrication Testpoint Usage	1	<input checked="" type="checkbox"/>	Fabrication Testpoint Usage	Testpoint	All	Testpoint - One Required Multiple - Not Allowed
Fanout	Fanout_BGA	1	<input checked="" type="checkbox"/>	Fanout Control	Routing	isBGA	Style - Auto Direction - Alternating In and Out Via Grid = 1
Fanout	Fanout_Default	5	<input checked="" type="checkbox"/>	Fanout Control	Routing	All	Style - Auto Direction - Alternating In and Out Via Grid = 1
Fanout	Fanout_LCC	2	<input checked="" type="checkbox"/>	Fanout Control	Routing	isLCC	Style - Auto Direction - Alternating In and Out Via Grid = 1
Fanout	Fanout_Small	4	<input checked="" type="checkbox"/>	Fanout Control	Routing	(CompPriCount < 5)	Style - Auto Direction - Out Then In Via Grid = 1mil
Fanout	Fanout_SOIC	3	<input checked="" type="checkbox"/>	Fanout Control	Routing	isSOIC	Style - Auto Direction - Alternating In and Out Via Grid = 1
Height	Height	1	<input checked="" type="checkbox"/>	Height	Placement	All	Pref Height = 500mil Min Height = 0mil Max Height = 10
HoleSize_1	HoleSize_1	2	<input checked="" type="checkbox"/>	Hole Size	Manufacturing	All	Min = 42mil Max = 42mil
HoleSize_2	HoleSize_2	1	<input checked="" type="checkbox"/>	Hole Size	Manufacturing	All	Min = 20mil Max = 20mil
HoleToHoleClearance	HoleToHoleClearance	1	<input checked="" type="checkbox"/>	Hole To Hole Clearance	Manufacturing	All - All	Hole To Hole Clearance = 10mil
Layer Pairs	Layer Pairs	1	<input checked="" type="checkbox"/>	Layer Pairs	Manufacturing	All	Layer Pairs - Enforce
Minimum Annular Ring	Minimum Annular Ring	1	<input checked="" type="checkbox"/>	Minimum Annular Ring	Manufacturing	All	Min = 2mil
Minimum Solder Mask Sliver	Minimum Solder Mask Sliver	1	<input checked="" type="checkbox"/>	Minimum Solder Mask Sliver	Manufacturing	All - All	Minimum Solder Mask Sliver = 10mil
Net Antennae	Net Antennae	1	<input checked="" type="checkbox"/>	Net Antennae	Manufacturing	All	Net Antennae Tolerance = 0mil
Paste Mask Expansion	Paste Mask Expansion	1	<input checked="" type="checkbox"/>	Paste Mask Expansion	Mask	All	Expansion = 0mil
Plane Clearance	Plane Clearance	1	<input checked="" type="checkbox"/>	Power Plane Clearance	Plane	All	Clearance = 20mil
Power Plane Connect Style	Power Plane Connect Style	1	<input checked="" type="checkbox"/>	Power Plane Connect Style	Plane	All	Style - Relief Connect Expansion = 20mil Width = 10mil
Polygon Connect	Polygon Connect	1	<input checked="" type="checkbox"/>	Polygon Connect Style	Plane	All - All	Style - Relief Connect Width = 10mil Angle = 90 # Ends
Routing Corners	Routing Corners	1	<input checked="" type="checkbox"/>	Routing Corners	Routing	All	Style - 45 Degree Min Setback = 100mil Max Setback = 1C
Routing Layers	Routing Layers	1	<input checked="" type="checkbox"/>	Routing Layers	Routing	All	Test over - Enabled Bottom Layer - Enabled
Routing Priority	Routing Priority	1	<input checked="" type="checkbox"/>	Routing Priority	Routing	All	
Routing Topology	Routing Topology	1	<input checked="" type="checkbox"/>	Routing Topology	Routing	All	
Routing Via Style	Routing Via Style	1	<input checked="" type="checkbox"/>	Routing Via Style	Routing	All	
Silk To Silk Clear	Silk To Silk Clear	1	<input checked="" type="checkbox"/>	Silk To Silk Clear	Routing	All	

3



Rules – design rules

- DRC file available [here](http://www.ece.ubc.ca/~eng-services/files/courses/elec391-spring2017/pcb-design/):
<http://www.ece.ubc.ca/~eng-services/files/courses/elec391-spring2017/pcb-design/>
- Download and save as “.RUL” file
- On your PCB design select:
Design >> Rules
- On the 'PCB Rules and Constrains Editor', Right click anywhere on the left column
 - Select: Import Rules
 - Select all rules in window (using shift and mouse)
→ OK
 - Browse to select .RUL file
 - Clear existing rules prior to import? → NO

Rules – design rules

- Component clearance and (electrical) clearance:
 - Minimum distance = 7 mil
- (Routing) width:
 - Minimum trace width = 7 mil
- Annular ring size:
 - Minimum annular ring size = 7 mil
 - Minimum annular ring size for vias = 5 mil
- Board outline clearance: 10mils
- Limited set of allowed hole sizes



Rules – hole sizes

- Pre-selected hole and drill sizes: non-plated vs. plated sizes

Drill Number Set	Drill Size	Finished Size	Approximate Use
#76	.020"	.017"	via holes
#70	.028"	.025"	via holes, fine lead devices such as trim pots etc.
#65	.035"	.032"	IC's, 1/4 watt resistors, small diodes, ripple caps etc.
#62	.038"	.035"	Square posted pins that measure .025" on the flat.
#58	.042"	.039"	TO-220 packages, IDC type square posted headers, 1/2 watt resistors, 1N9000 series diodes, IC chip carriers, etc.
#55	.052"	.049"	larger connectors, transformer leads, etc.
#53	.060"	.057"	similar to .052" above
#44	.086"	.083"	TO-220 mounting holes, screw holes, general mounting
1/8 in.	.125"	.122"	mounting holes
#24	.152"	.149"	mounting holes

PCB Hole Size Editor

The image shows the Altium Designer PCB Hole Size Editor interface. The left pane displays the Hole Size Editor settings, and the right pane shows the Libraries panel with a context menu open. Red callouts 1, 2, 3, and 4 point to specific elements in the interface.

1 Points to the **PCB** option in the context menu.

2 Points to the **PCB** option in the context menu.

3 Points to the **PCB** option in the context menu.

4 Points to the **PCB** option in the context menu.

The Hole Size Editor settings on the left include:

- Hole Size Editor** (dropdown)
- Apply**, **Clear**, **Zoom Level...** (buttons)
- Normal** (dropdown)
- Select**, **Zoom**, **Clear E** (checkboxes)
- Condition** (dropdown)
- Primitive Type**: Any
- Plating**: Any
- Include**: Layer Pairs
- 6 Unique Holes** (Highlighted)
- Table of holes:

C..	Hole...	Len	Type	P...	Sy...
64	2mil	-	Round	<input checked="" type="checkbox"/>	
42	40mil	-	Round	<input checked="" type="checkbox"/>	
13	43.307r	-	Round	<input checked="" type="checkbox"/>	*

Below the table, there are fields for **0 Pads/0 Vias (0 Pads/0 Vias Highigh...)**, **Kind**, and **Designato...**.

The Libraries panel on the right shows a list of components, including:

- A PartsD: 555 timer (sing DIP8_L)
- A PartsD: 555 timer (dua DIP14_)
- A PartsD: triple 2x1 mux DIP16_
- A PartsD: dual 4x1 mux (DIP16_)
- A PartsD: A-Mux8 DIP16_
- C PartsD: Banana plug f Ban1 cr
- C PartsD: DB9 conn DSUB-:
- C PartsD: DB25 conn DSUB-:
- C PartsD: Header, 2-Pin HDR1X
- C PartsD: Header, 4-Pin HDR1X
- C PartsD: Header, 4-Pin HDR1X
- C PartsD: Header, 6-Pin HDR1X

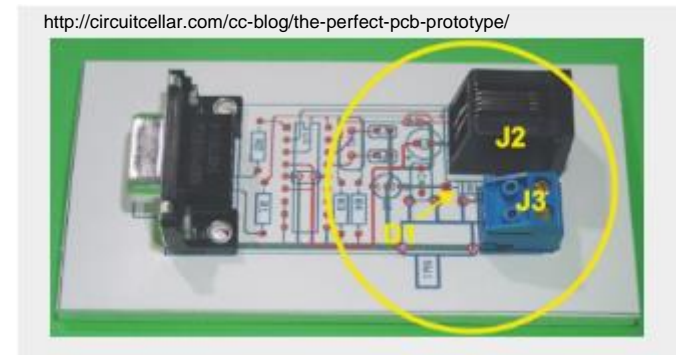
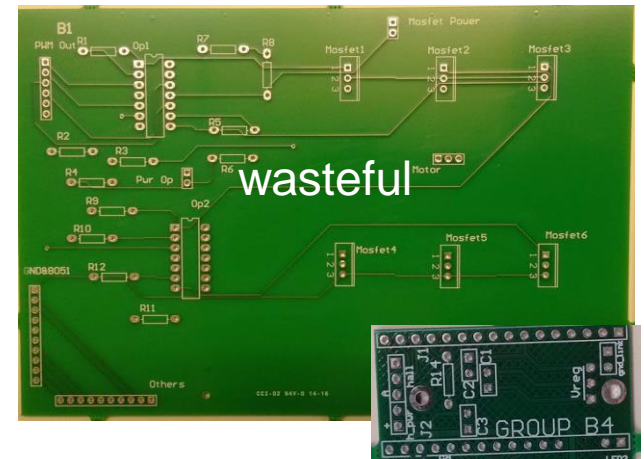
The context menu is open, showing options like **3D Visualization**, **Board Insight**, **Collaborate, Compare and Merge**, **PCB** (checked), **PCB 3D Movie Editor**, **PCB Filter**, **PCB Inspector**, **PCB List**, and **PCB Rules And Violations**.



PCB Design Best Practices

Best Practices: Estimating board size

- Before starting layout it is good to have an idea of the target size of the PCB board and all other relevant dimensions.
- It is very helpful to have the components at hand to plan the floor-plan.
- An old good trick of the trade is to print the PCB layout at a 1:1 scale, place the printout on a foam and stick on the through hole components.

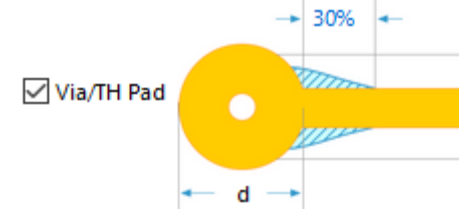


Best Practices: Floor planning

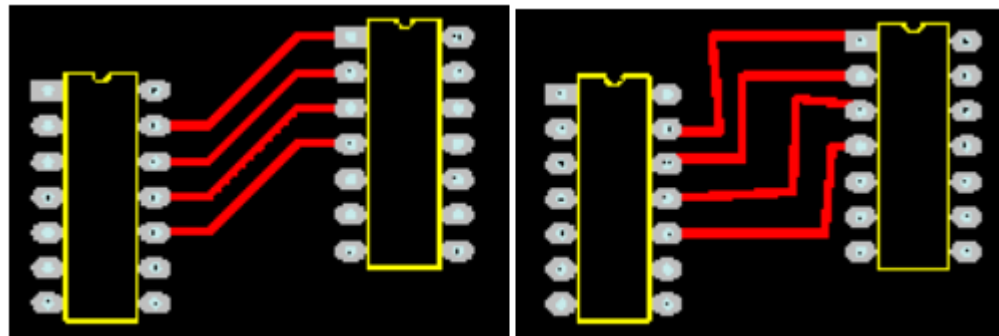
- Choose your units and set the grid
- Carefully plan the placement of components
 - Place analog and digital sections apart
 - Group components into 'functional blocks'
 - Place ICs in the same direction
 - Align ICs, resistors, labels, capacitors etc.
 - Place de-caps close by their ICs
 - Place Op-amp resistors near the Op-amp
 - Plan for mounting holes and heat sinks
- Aim for symmetry when possible
- Do use Design Rule check

Best Practices: Routing strategy

- On two sided boards keep traces perpendicular as much as possible
- Avoid 90 degree bends in tracks (?) (reduced chances of acid traps)
- Keep traces as short as possible
- Always connect a trace to the center of the pad
- Use teardrops (Tools >> tear drops), and use vias to avoid lockout
- Do not place vias under SMD pads
- Layout first all critical traces
 - e.g. CLK, diff pairs, controlled length

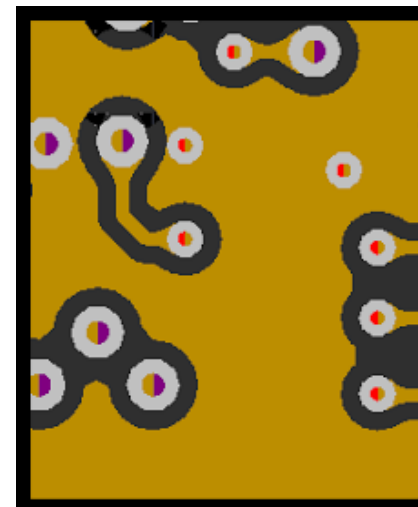


- Polygons as fills:
Connect to GND (EMC), or do not leave 'dead copper' →
- Rout nicely



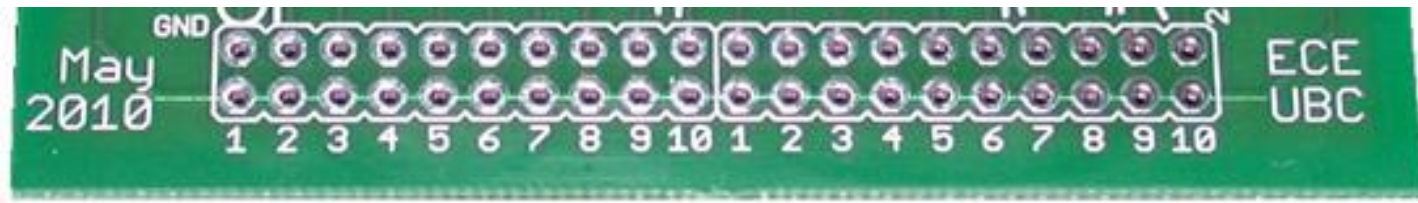
[Ref 3]

An example of GOOD routing (Left) and BAD routing (Right)



Best Practices: Labelling

- Always sign your design: add date, version, and name of board
- Label all relevant inputs and outputs
- Default sizes for comments and designators are 60mils x 10mils
- If you have silkscreen on both sides add a 'TOP' label to the top overlay.



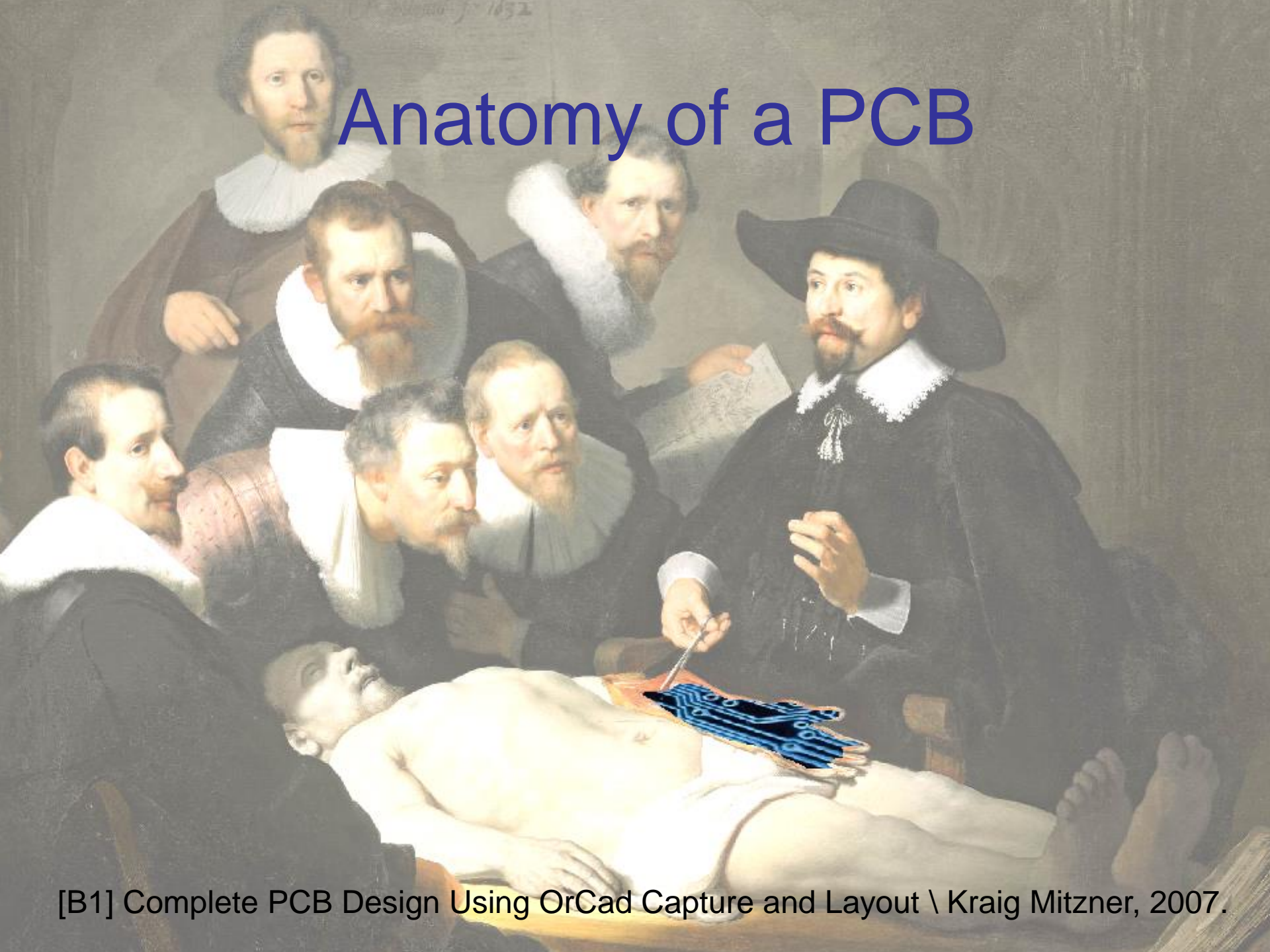
Best Practices: Finishing touches

- Add mounting holes
- Run: Reports >> Board Information
 - Board specification → to confirm board size
 - Non-plated hole size
 - Plated hole size
- Using the hole size editor:
 - Minimize the total number of holes sizes
 - Verify that all vias are the same size (if possible)
- Verify that there are no unwanted leftovers on any Mechanical layer

Online resources

1. [Ten best practices of PCB design – EDN Magazine, Edwin Robledo & Mark Toth](#)
2. [Circuit Board Layout Techniques – Texas Instruments, Chapter 17 of Op-amps for everyone](#)
3. [PCB Design Tutorial – David L. Jones](#)

Anatomy of a PCB



[B1] Complete PCB Design Using OrCad Capture and Layout \ Kraig Mitzner, 2007.

PCB Anatomy: Substrate

- Substrate (laminate)
 - Rigid board of insulating material
 - Provides structural support to the circuit components
 - Most commonly used material type is FR4, 62-63mils thick
 - Laminates are available in different thicknesses

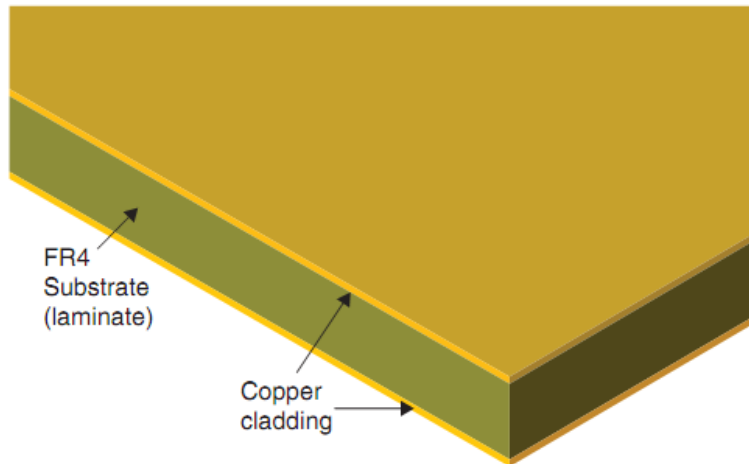


Figure 1-2 A double-sided copper clad FR4 substrate.

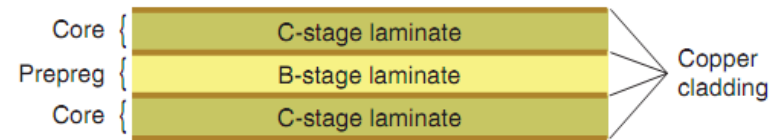


Figure 1-3 Cores and prepreg.

Cu thickness measured in weight oz/ft²

½ oz → 0.7mils

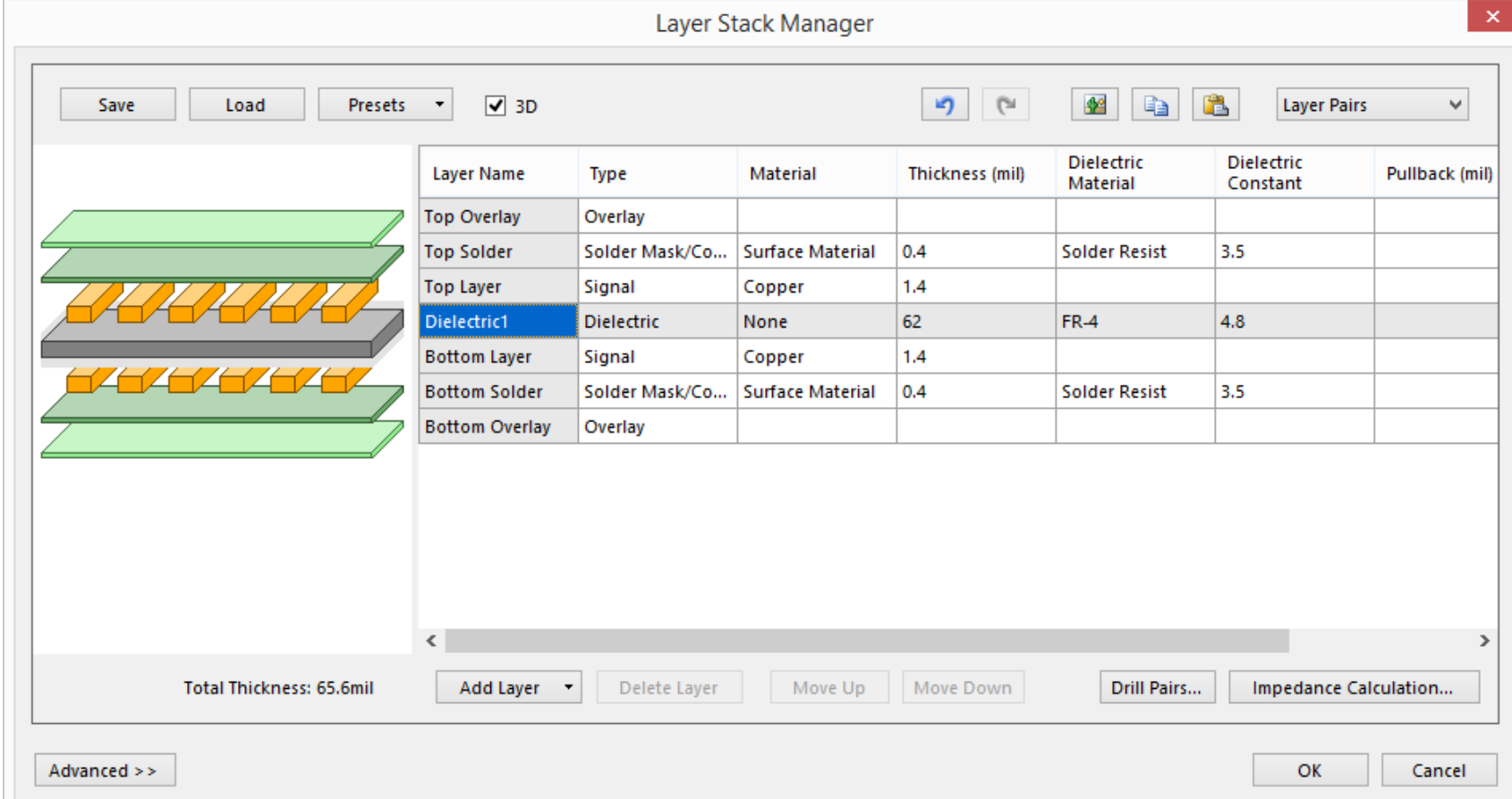
1 oz → 1.4mils

2 oz → 2.8mils

1mil = 25µm

PCB Anatomy: Layer Stackup

Design >> Layer Stack Manager ...



The Layer Stack Manager dialog box displays a 3D visualization of a PCB stackup on the left and a table of layer properties on the right. The 3D view shows a multi-layer board with alternating green (dielectric) and orange (copper) layers, with solder mask and overlay layers on top and bottom. The table lists the following layers:

Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)
Top Overlay	Overlay					
Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5	
Top Layer	Signal	Copper	1.4			
Dielectric1	Dielectric	None	62	FR-4	4.8	
Bottom Layer	Signal	Copper	1.4			
Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5	
Bottom Overlay	Overlay					

At the bottom of the dialog, the total thickness is shown as 65.6mil. Control buttons include Save, Load, Presets, 3D (checked), Layer Pairs, Add Layer, Delete Layer, Move Up, Move Down, Drill Pairs..., Impedance Calculation..., OK, and Cancel. An Advanced >> button is also present.

PCB Anatomy: Traces / Tracks

- Copper traces are patterned either by:
 - Photolithography: requires photomasks
 - Laser: used to draw patterns on photoresist
 - Mechanical milling: Cu is removed to isolate the traces.
- Trace width and thickness determines:
 - Ampacity (current carrying capacity)
 - Characteristic impedance for RF designs
- Practical limitations:
 - Minimum trace width and gap

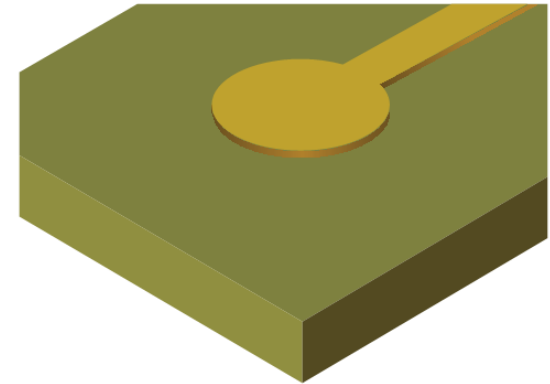


Figure 1-11 Copper pad and trace after etching and resist stripping.

Negative view:
Copper planes, Drill
holes, Solder Masks



Figure 1-18 Copper in a plane layer (negative view without drill info). (a) Copper plane with thermal relief. (b) Negative view in Layout.

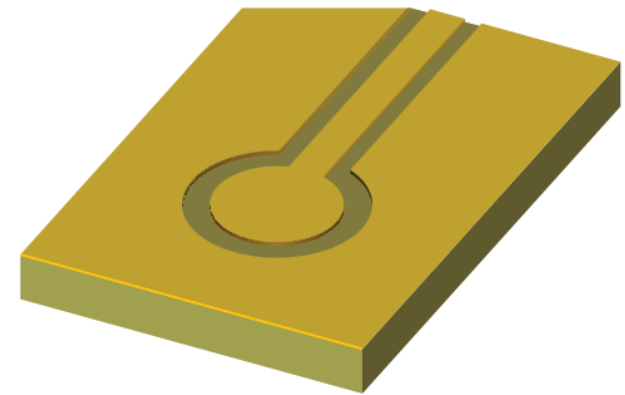
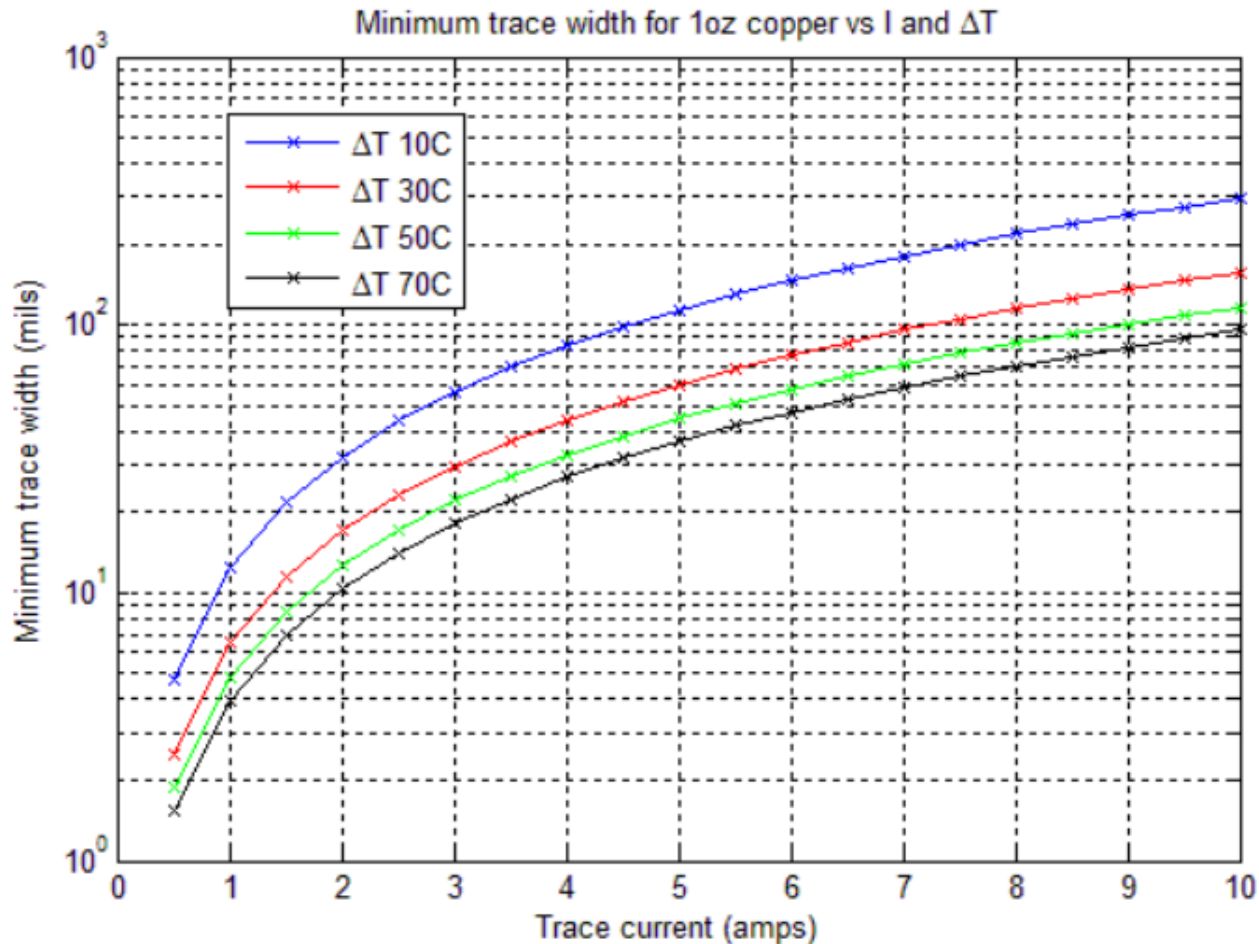


Figure 1-12 A mechanically milled trace.

PCB Anatomy: Trace width



Use the following online trace width calculator:

<http://circuitcalculator.com/wordpress/2006/01/31/pcb-trace-width-calculator>

PCB Anatomy: Vias

- Connection between layers is accomplished with via holes
- After the holes are drilled, their inner walls are plated
- Top and bottom traces are patterned after plating

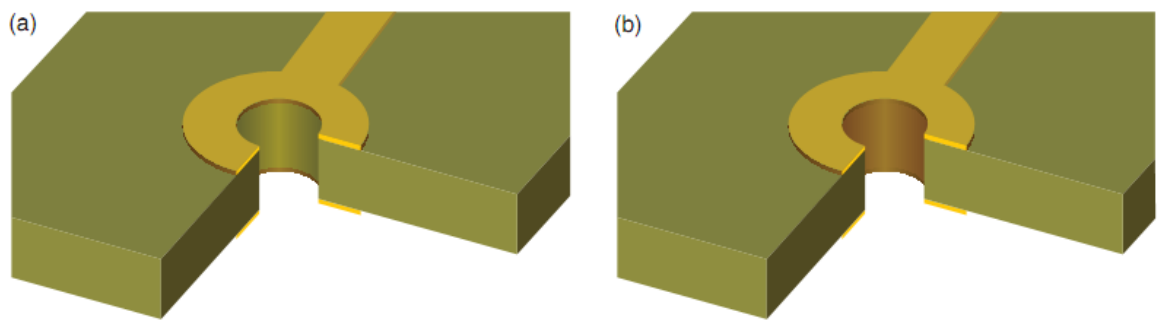
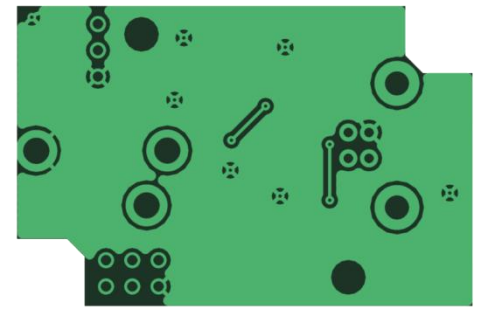


Figure 1-13 Holes are drilled into the board and then copper plated. (a) A nonplated through-hole. (b) A plated through-hole.

Thermal relief is needed when connecting a via to a copper plane

PWR and GND planes are commonly inner layers

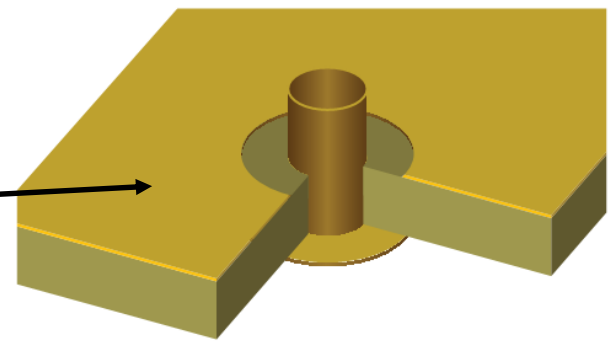


Figure 1-15 A clearance area provides isolation between a plated hole and a plane.

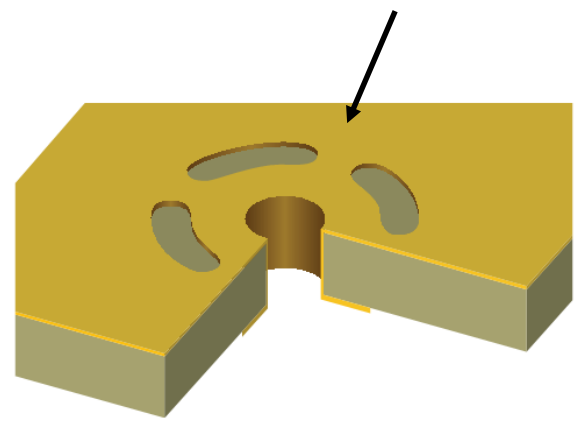
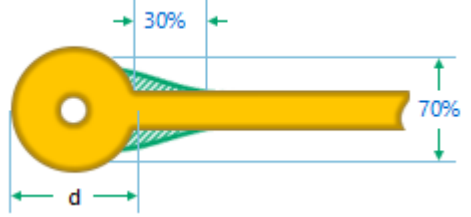


Figure 1-14 A connection to a plane layer through a thermal relief.

Teardrops:



PCB Anatomy: Vias

- Types of via holes:
 - Plated and un-plated through-hole, blind, buried

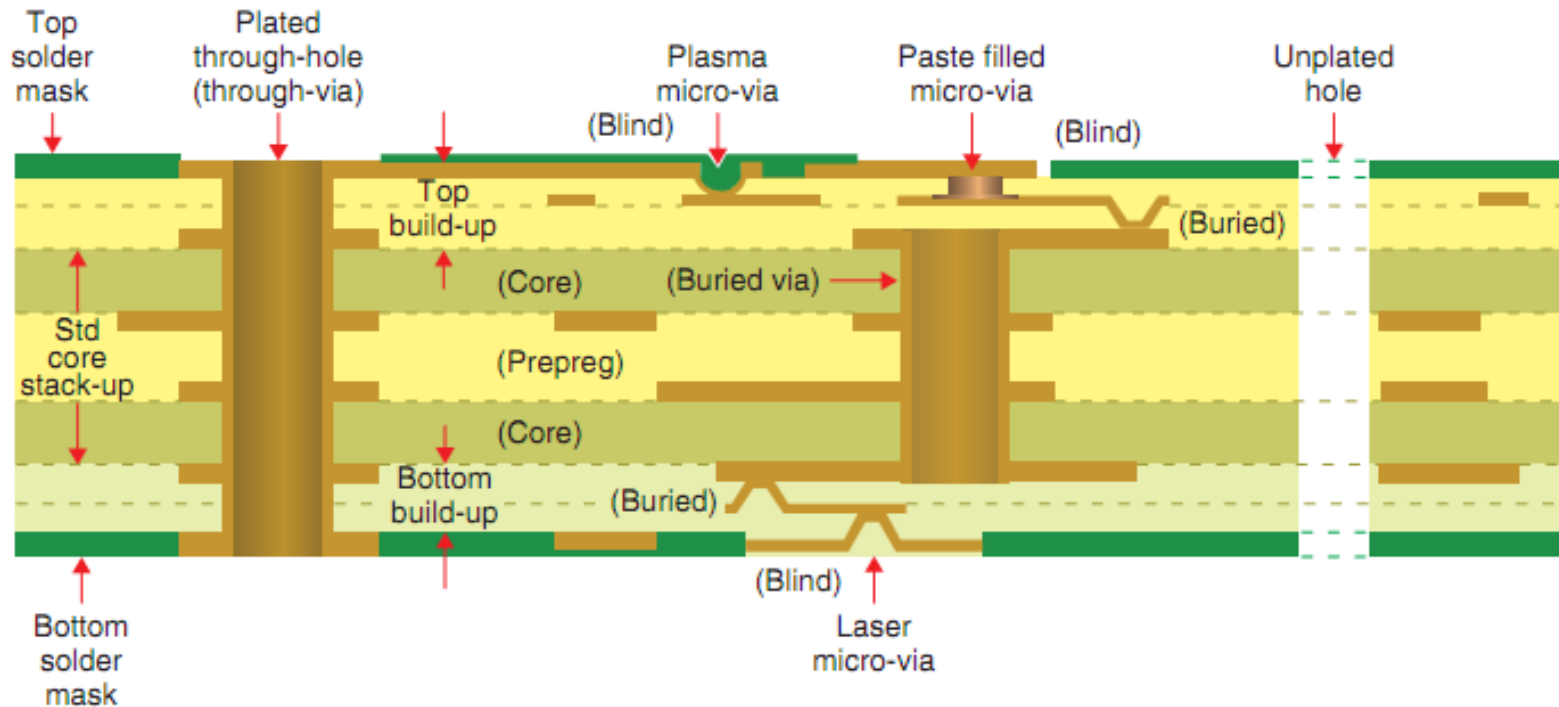


Figure 1-5 A built-up, multitechnology, PCB stack-up.

PCB Anatomy: Holes

Holes can be:

- Vias, multi-layer pads, mounting holes, or cuts
- Plated or non plated

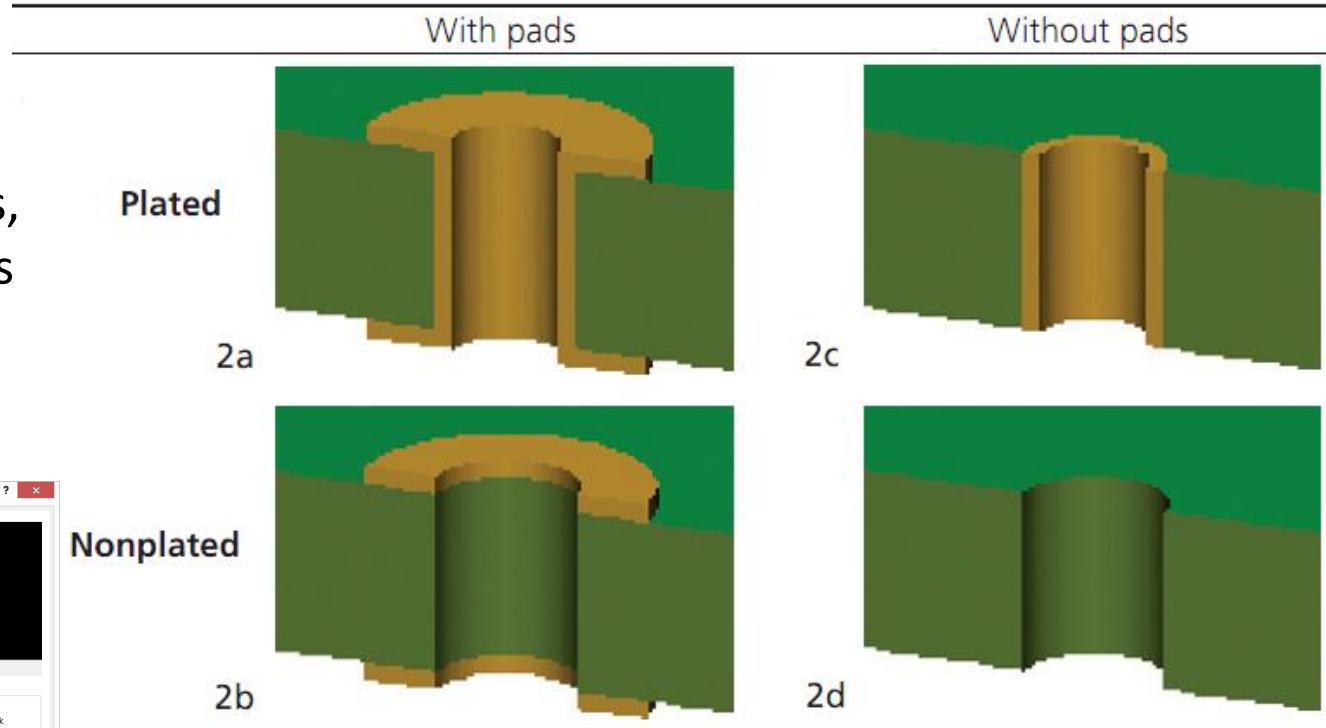
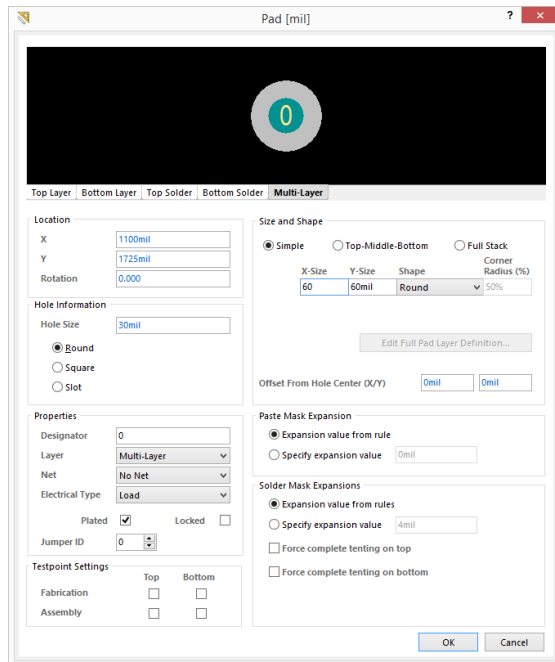


Table 8-2 Basic hole types

You must specify whether a hole is plated or non plated during the design process

PCB Anatomy: Pads

- Pads: contact areas for soldering components, test points, and solder traps
- Pads can have any shape
- Single layer pads: Top/bottom layer, common for SMT, end launch connectors
- Multi-layer pads: for through hole components
- Footprints are a collection of pads

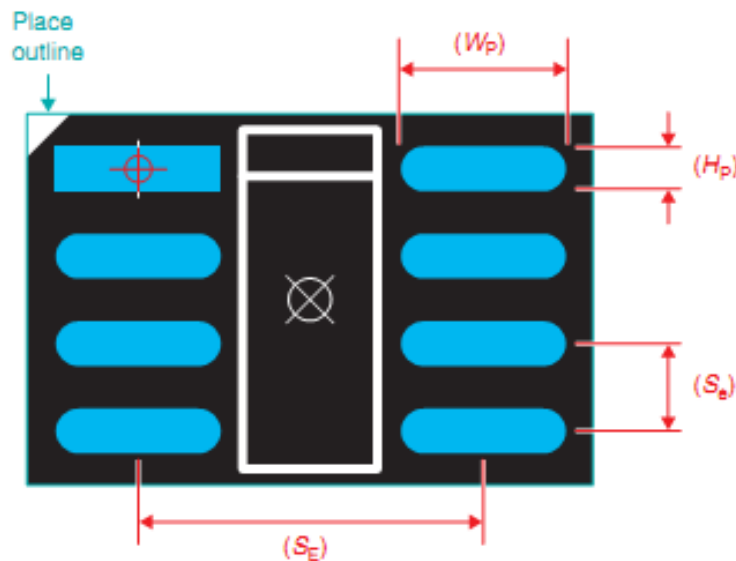


Figure 5-7 Footprint dimensions (typical convention).

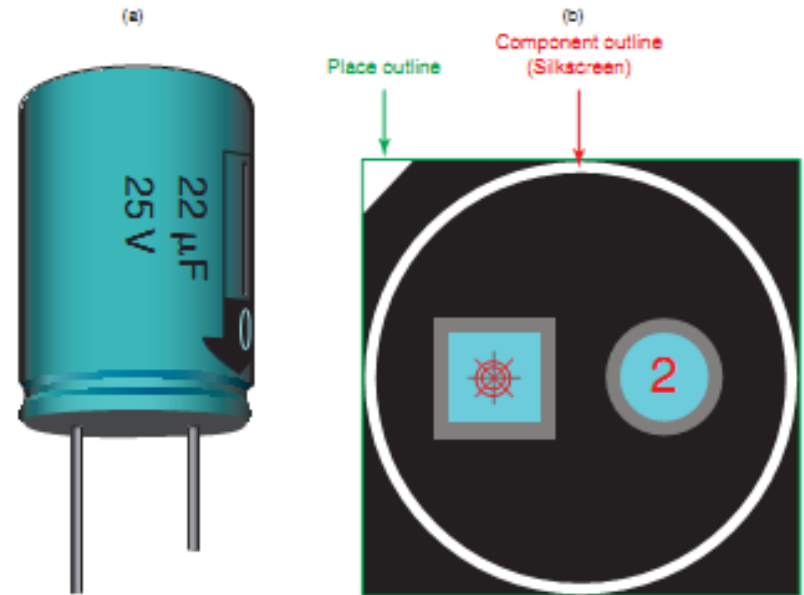


Figure 5-12 Radial-leaded through-hole device. (a) Axial-leaded capacitor. (b) Layout axial footprint

PCB Anatomy: Solder mask

- Solder mask or solder resist:
 - Thin polymer layer deposited on top and bottom layers
 - Protects outer layers from oxidation and prevents solder bridges
 - Allows for wave or reflow soldering of components
 - Holes are opened with photolithography wherever components will be soldered
 - Default color is green, but any other color is possible

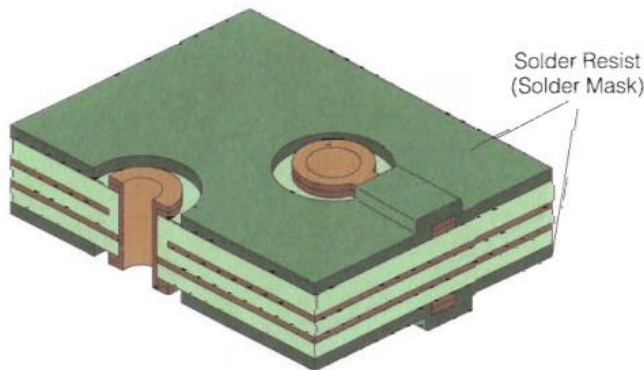


Illustration ML-14. *Apply solder resist.* The specified resist (either dry film, liquid photoimageable, or screen printed) is applied to the surfaces of the PCB or panel.

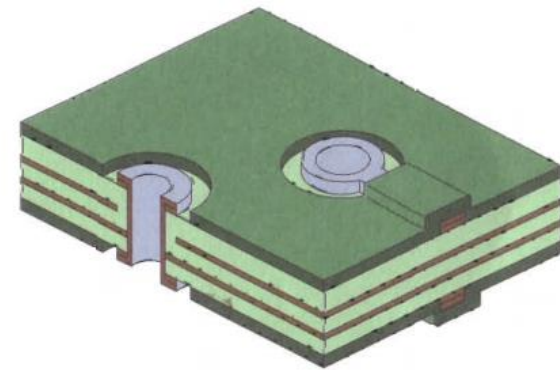
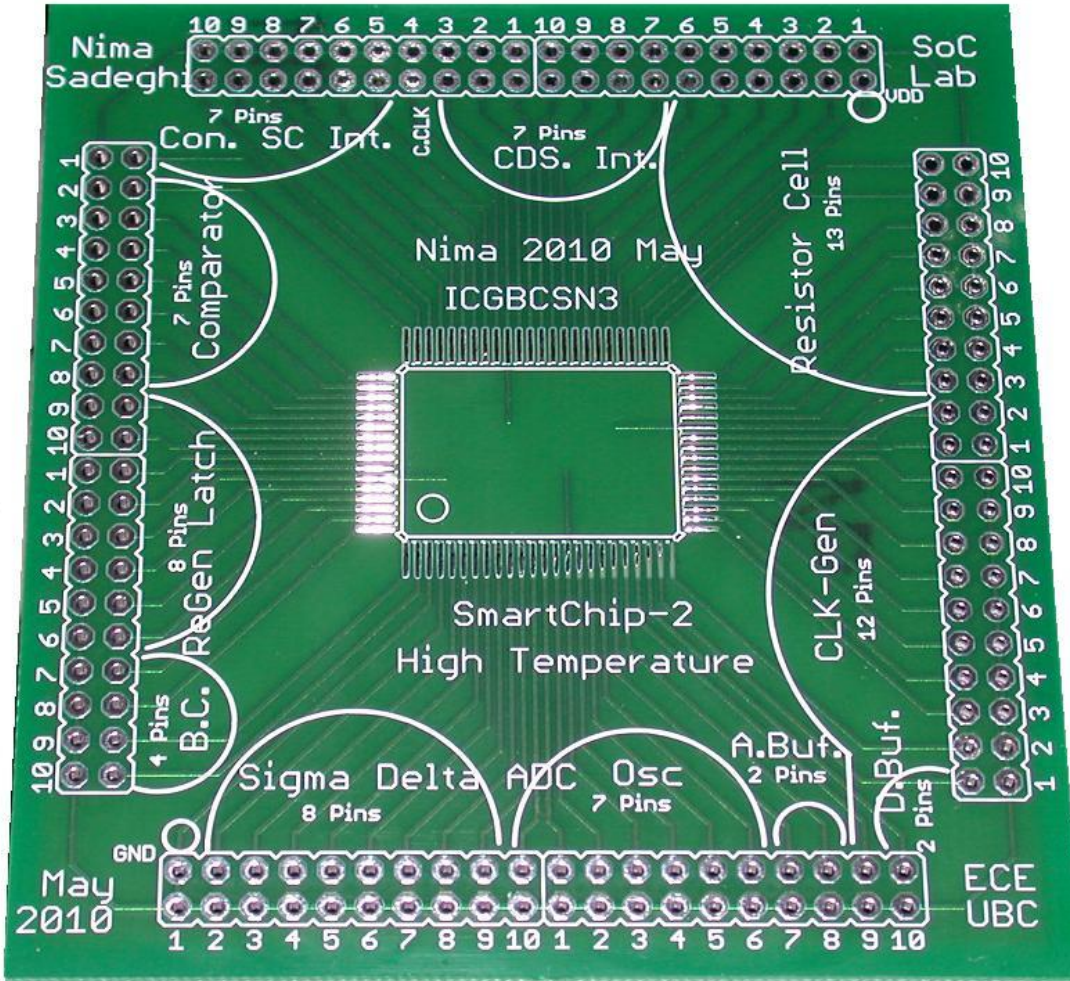


Illustration ML-15. *Solder coat.* Solder (tin/lead) is applied to the exposed copper areas, and the excess solder is removed.

Source: Printed Circuit Board Basics: An Introduction to the PCB Industry, by: Michael Flatt

PCB Anatomy: Legend / Silkscreen / Overlay



- Legend or silkscreen:
 - Applied on top of the solder resist
 - Can be applied to one or both outer layers
 - Default color is white but any other color is possible

Tip: add (Top) and (Bottom)

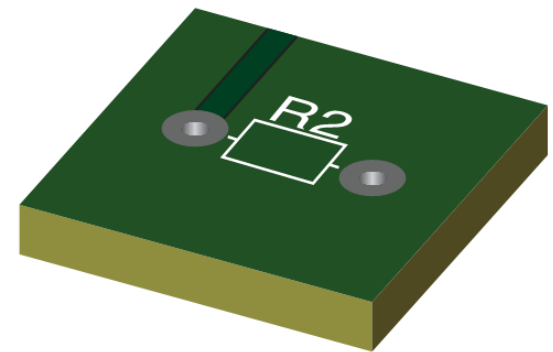
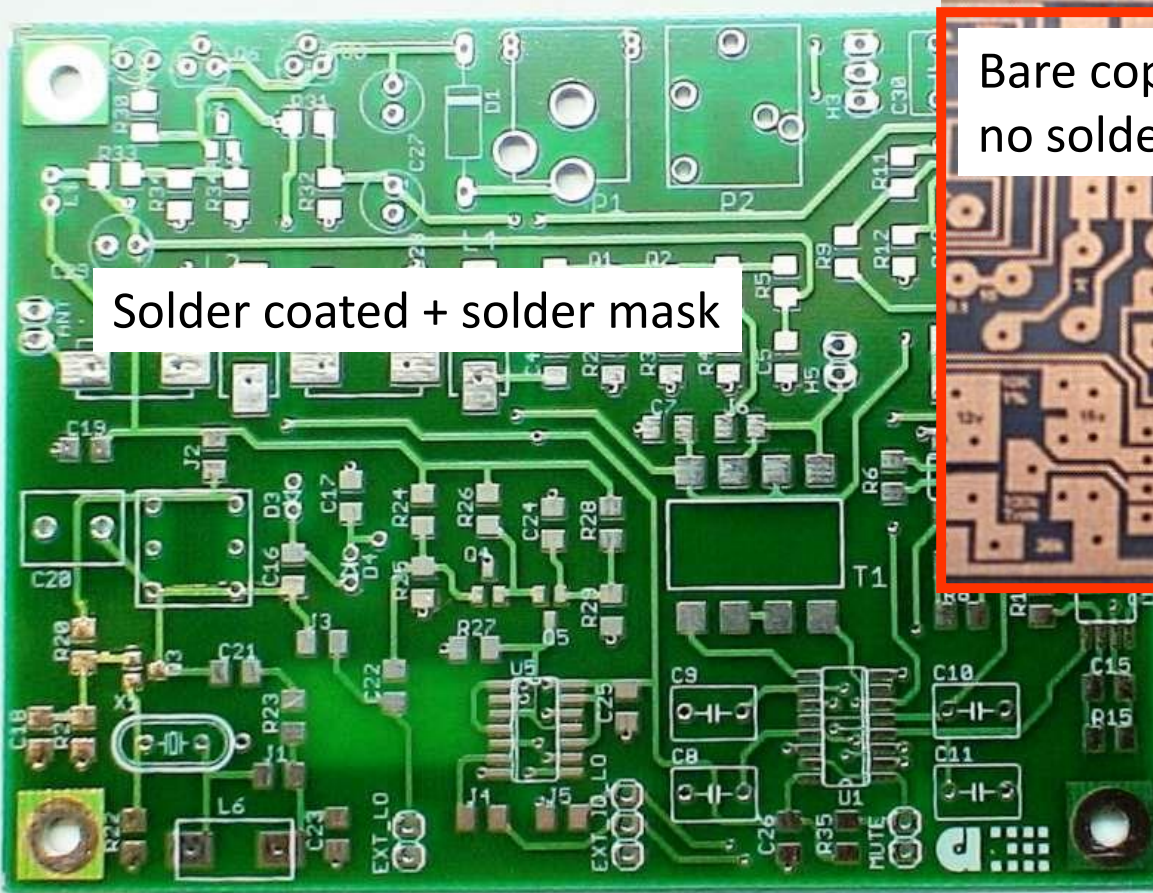
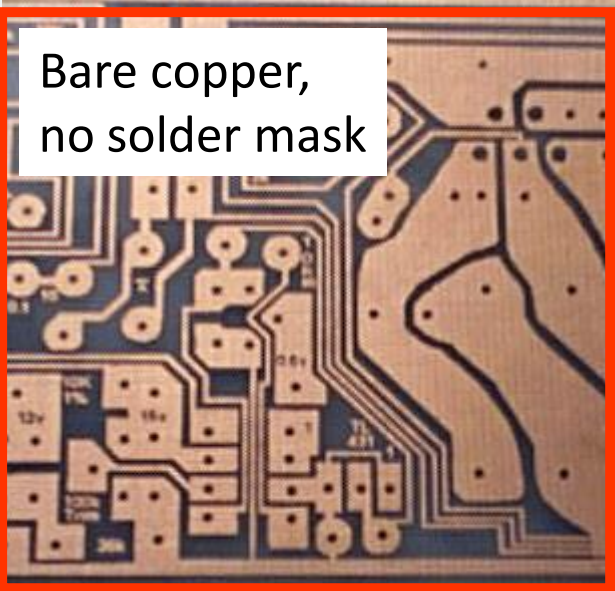


Figure 1-16 Final layers are the soldermask (green) and silk screen (white).

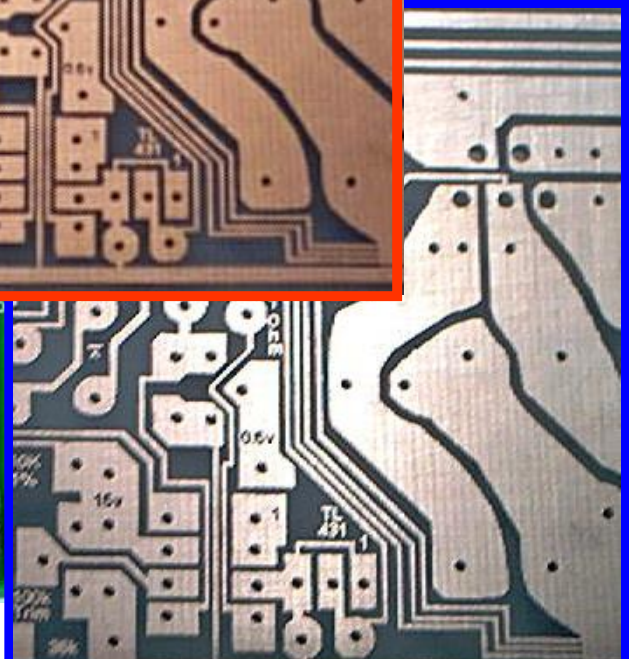
PCB Anatomy: Solder coat / thinning



Solder coated + solder mask



Bare copper, no solder mask



Solder coated + no solder mask

PCB Anatomy: Mechanical Layers

- Multi-purpose layers
- E.g. Altium supports 32 Mechanical layers: M1 ... M32
- Typically
 - M1 Board outline
 - M2 PCB manufacturing info
 - M11-M12 Top and bottom layer dimensions
 - M13 Top layer 3D models and mechanical outlines
 - M14 Bottom layer 3D models and mechanical outlines
 - M15 Top layer assembly information
 - M16 Bottom layer assembly information