

Altium I

(Circuit Design + Layout)

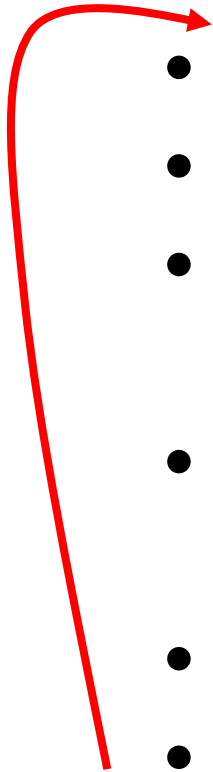
ELEC391

Summer T1 2018

Contents

- PCB Design support for ELEC391
 - PCB design flow
 - How to install Altium Designer 2016
 - Understanding Altium Designer

 - Walk-through example

 - PCB design best practices
 - Anatomy of a PCB
- 

Credits: Unless explicitly stated all source material is from the Altium website and Altium training documents.

PCB Design support for ELEC391:

Altium 2016, 150 licenses

- Jun 4 Altium I (Circuit Design + Layout)
- PCB Submissions Jun 10



We will panelize your designs to speed up fabrication and reduce costs

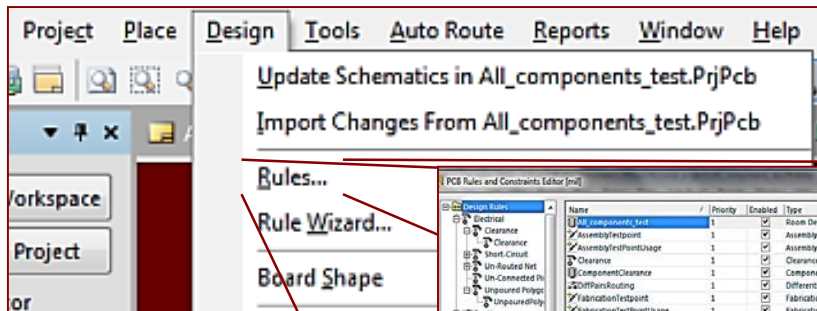
Panelized designs from elec391 Spring 2016

Submission Instructions

- FR4 62mils, 7mils/7mils, 2-layers, top overlay only.
- Designs must pass DRC
- You can send several different boards per submission.
- You can request several copies of each but that increases your area.
- Email pcb@ece.ubc.ca
Subject: [PCB] ELEC391, Group #, submission#
- Attach: *PcbDoc files only
Body:
Total number of designs (not copies) to fabricate
Name of designs to fabricate and number of copies for each

Rules and Checks

1

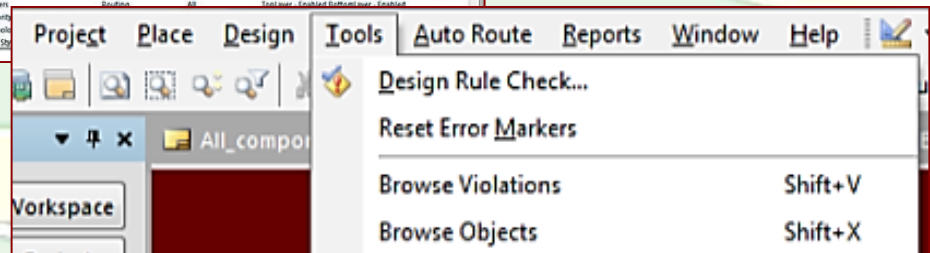


2

PCB Rules and Constraints Editor [mli]

Design Rules	Name	Priority	Enabled	Type	Category	Scope	Attributes
Electrical	All_components_test	1	<input checked="" type="checkbox"/>	Route Definition	Placement	ICComponentClass{A Region (S) = 5580Mx 2320Mx (S)1511Mx 21540Mx}	50M
Clearance	AssemblyTestpointUsage	1	<input checked="" type="checkbox"/>	Assembly Testpoint Usage	Testpoint	All	Under Comp - Allow Sides - Top, Bottom - Pref Size = 60mil
Clearance	Clearance	1	<input checked="" type="checkbox"/>	Clearance	Electrical	All - All	Clearance = 10mil
Component Clearance	ComponentClearance	1	<input checked="" type="checkbox"/>	Component Clearance	Placement	All - All	Horizontal Clearance = 10mil Vertical Clearance = 10mil
Differential Pairs Routing	Differential Pairs Routing	1	<input checked="" type="checkbox"/>	Differential Pairs Routing	Routing	All	Pref Gap = 10mil Min Gap = 10mil Max Gap = 10milRef
Fabrication Testpoint	FabricationTestpoint	1	<input checked="" type="checkbox"/>	Fabrication Testpoint Usage	Testpoint	All	Under Comp - Allow Sides - Top, Bottom - Pref Size = 60mil
Fabrication Testpoint Usage	FabricationTestpointUsage	1	<input checked="" type="checkbox"/>	Fabrication Testpoint Usage	Testpoint	All	Testpoint - One Required - Multiple - Not Allowed
Fanout	Fanout_61A	1	<input checked="" type="checkbox"/>	Fanout Control	Routing	3DGA	Style - Auto Direction - Alternating In and Out Via Grid = 1
Fanout	Fanout_Default	5	<input checked="" type="checkbox"/>	Fanout Control	Routing	All	Style - Auto Direction - Alternating In and Out Via Grid = 1
Fanout	Fanout_LCC	2	<input checked="" type="checkbox"/>	Fanout Control	Routing	3LCC	Style - Auto Direction - Alternating In and Out Via Grid = 1
Fanout	Fanout_Small	4	<input checked="" type="checkbox"/>	Fanout Control	Routing	{CompPctCount < 5}	Style - Auto Direction - Out Then In Via Grid = 1mil
Fanout	Fanout_SOIC	3	<input checked="" type="checkbox"/>	Fanout Control	Routing	3SOIC	Style - Auto Direction - Alternating In and Out Via Grid = 1
Height	Height	1	<input checked="" type="checkbox"/>	Height	Placement	All	Pref Height = 500mil Min Height = 6mil Max Height = 10
Hole Size	HoleSize_1	2	<input checked="" type="checkbox"/>	Hole Size	Manufacturing	All	Min = 42mil Max = 42mil
Hole Size	HoleSize_2	1	<input checked="" type="checkbox"/>	Hole Size	Manufacturing	All	Min = 20mil Max = 20mil
Hole To Hole Clearance	HoleToHoleClearance	1	<input checked="" type="checkbox"/>	Hole To Hole Clearance	Manufacturing	All - All	Hole To Hole Clearance = 10mil
Layer Pairs	LayerPairs	1	<input checked="" type="checkbox"/>	Layer Pairs	Manufacturing	All	Layer Pairs - Enforce
Minimum Annular Ring	MinimumAnnularRing	1	<input checked="" type="checkbox"/>	Minimum Annular Ring	Manufacturing	All	Min = 2mil
Minimum Solder Mask Siver	MinimumSolderMaskSiver	1	<input checked="" type="checkbox"/>	Minimum Solder Mask Siver	Manufacturing	All - All	Minimum Solder Mask Siver = 10mil
Net Antennae	NetAntennae	1	<input checked="" type="checkbox"/>	Net Antennae	Manufacturing	All	Net Antennae Tolerance = 0mil
Paste Mask Expansion	PasteMaskExpansion	1	<input checked="" type="checkbox"/>	Paste Mask Expansion	Mask	All	Expansion = 0mil
Plane Clearance	PlaneClearance	1	<input checked="" type="checkbox"/>	Plane Clearance	Plane	All	Clearance = 20mil
Plane Connect	PlaneConnect	1	<input checked="" type="checkbox"/>	Plane Connect Style	Plane	All	Style - Relief Connect Expansion = 20mil Width = 10mil
Polygon Connect	PolygonConnect	1	<input checked="" type="checkbox"/>	Polygon Connect Style	Plane	All - All	Style - Relief Connect Width = 10mil Angle = 90 # Ends
Routing Corners	RoutingCorners	1	<input checked="" type="checkbox"/>	Routing Corners	Routing	All	Style - 45 Degree Min Setback = 100mil Max Setback = 10
Routing Layers	RoutingLayers	1	<input checked="" type="checkbox"/>	Routing Layers	Routing	All	Testpoint - Enforce Inhibit Layer - Enforce
Routing Priority	RoutingPriority	1	<input checked="" type="checkbox"/>	Routing Priority	Routing	All	
Routing Testpoint	RoutingTestpoint	1	<input checked="" type="checkbox"/>	Routing Testpoint	Routing	All	
Routing Via Style	RoutingViaStyle	1	<input checked="" type="checkbox"/>	Routing Via Style	Routing	All	

3

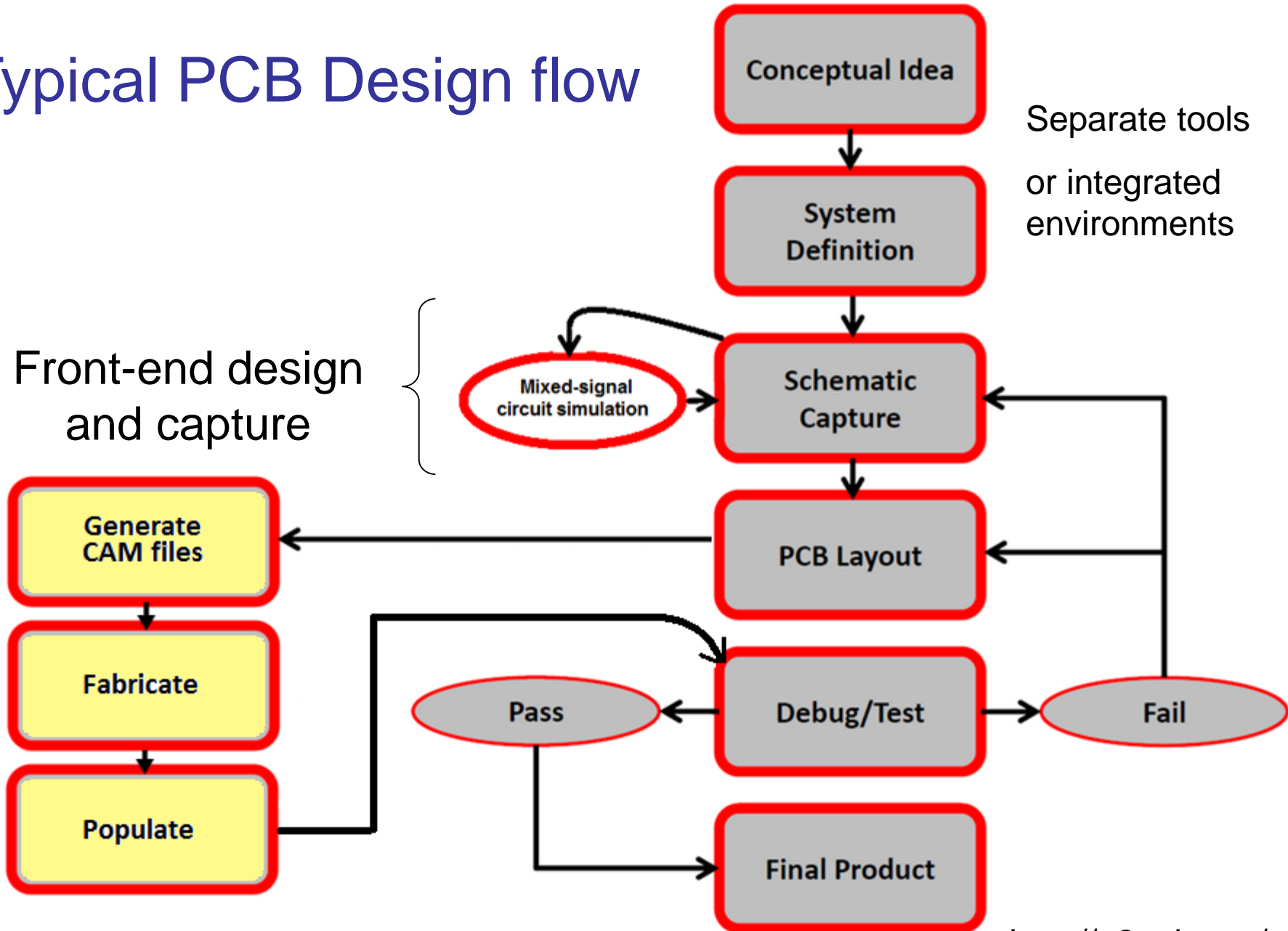


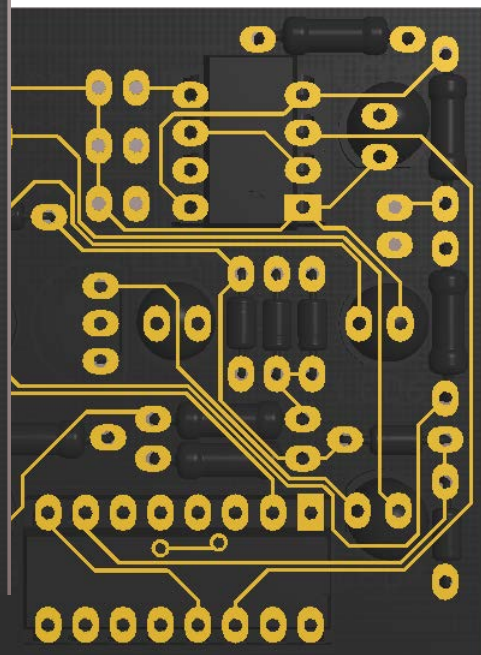
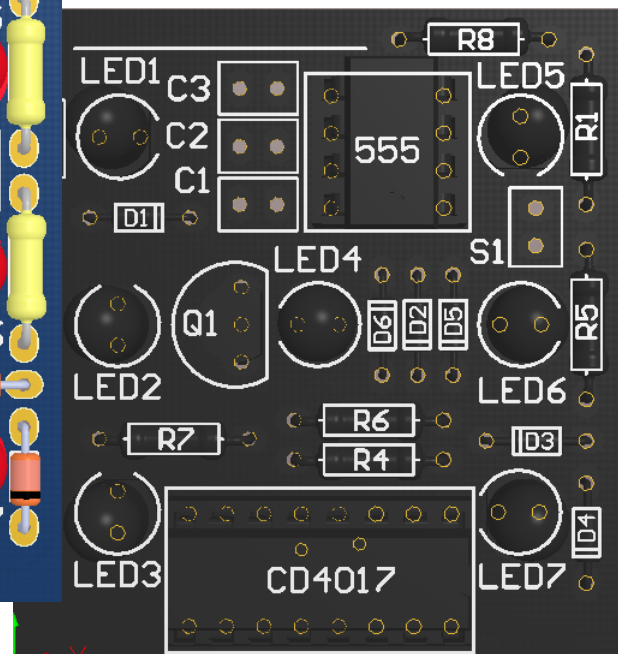
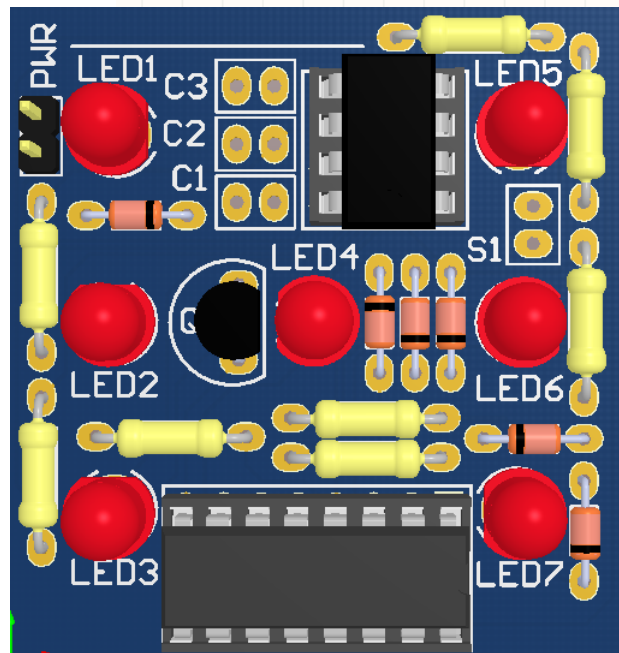
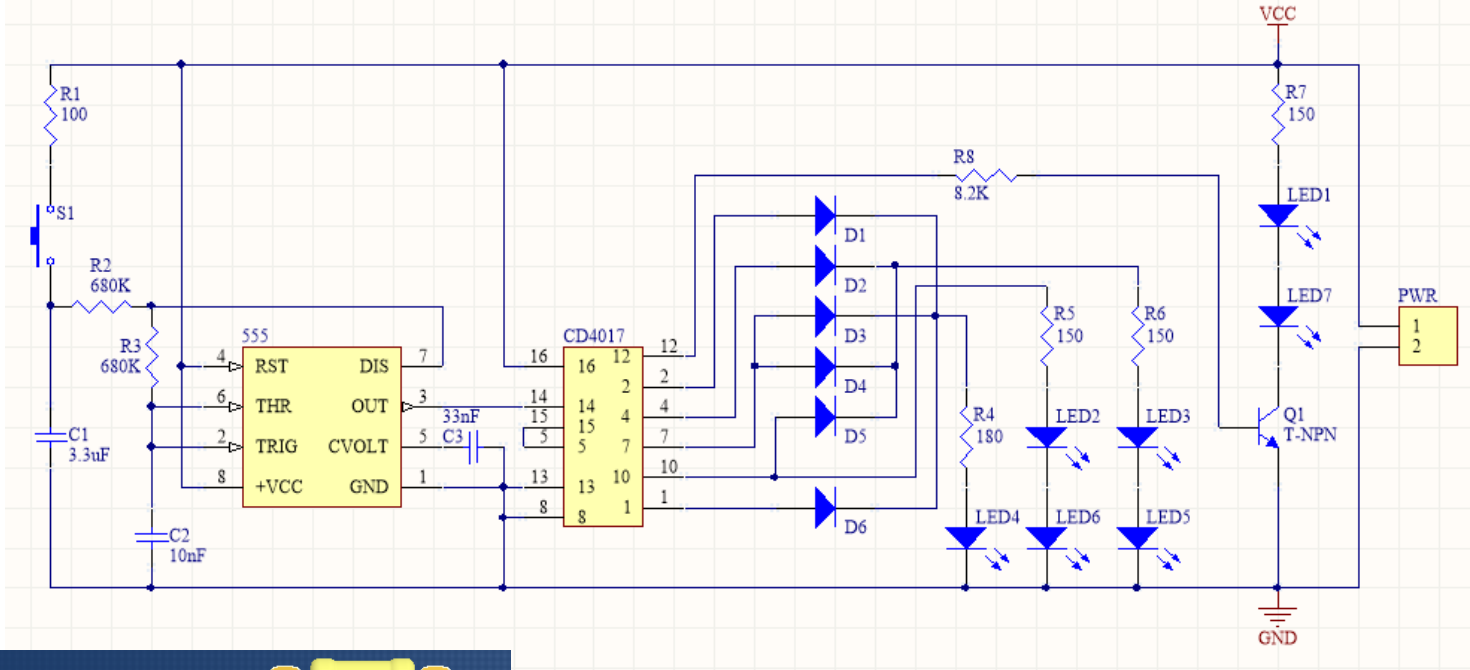
Rules – design rules

- Component clearance and (electrical) clearance:
 - Minimum distance = 7 mil
- (Routing) width:
 - Minimum trace width = 7 mil
- Annular ring size:
 - Minimum annular ring size = 7 mil
 - Minimum annular ring size for vias = 5 mil
- Board outline clearance: 10mils

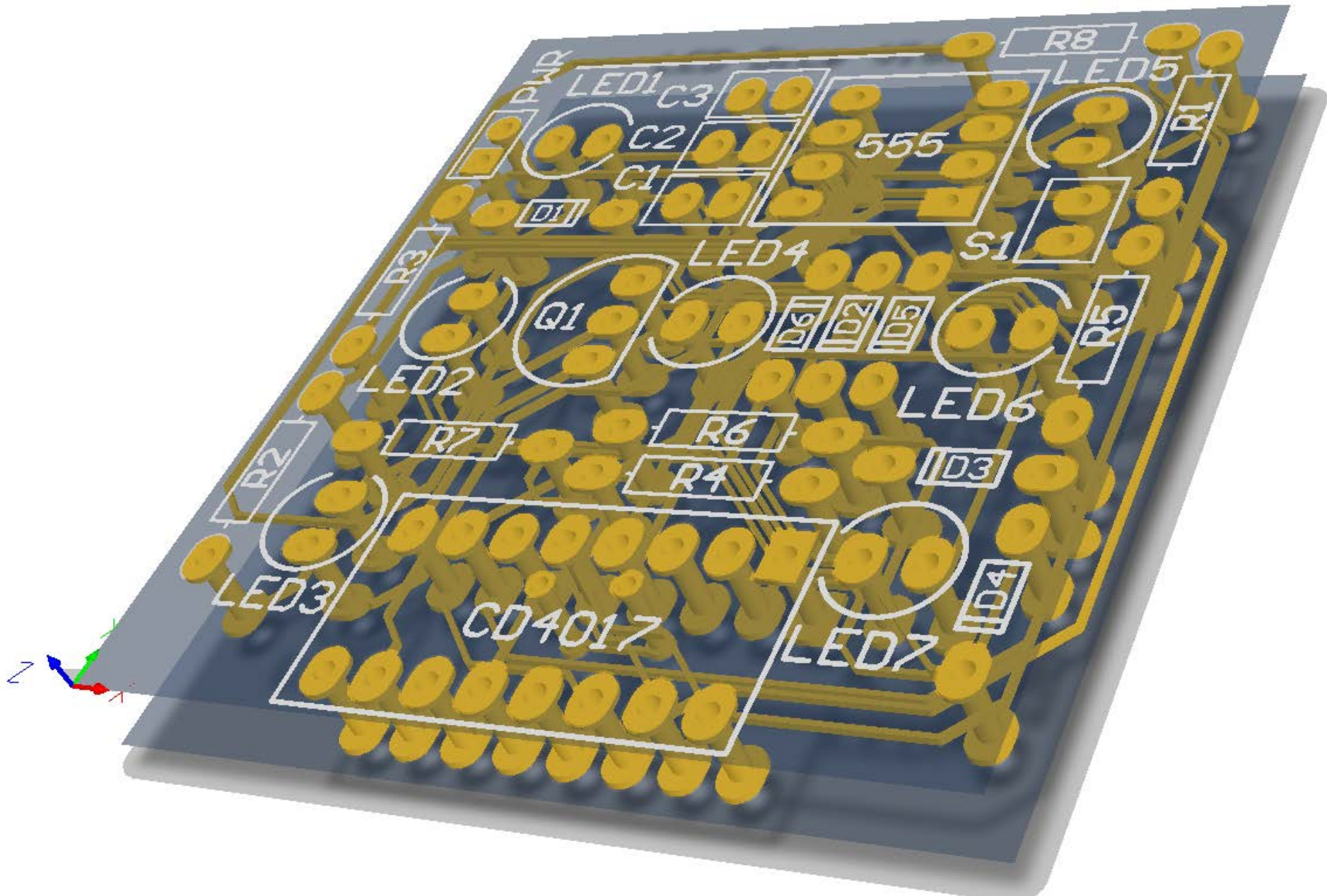


Typical PCB Design flow





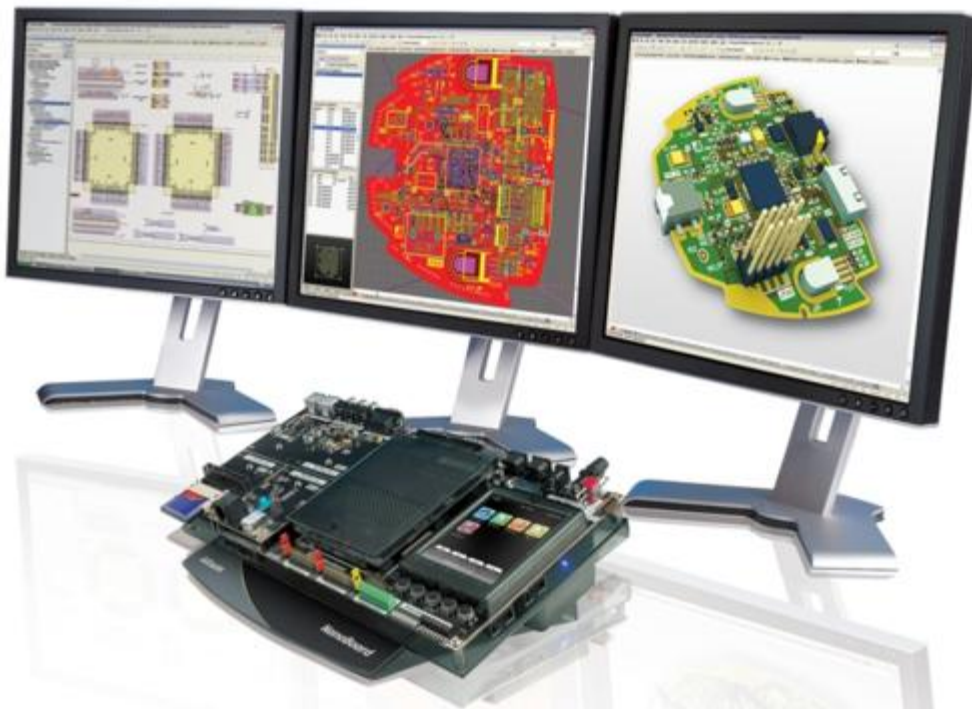
PCBs are multi-layer objects



Altium Designer 2016

A complete product development system

System requirements (MS W7, W8, W10)



- Front-end design and capture
- Physical PCB design
- FPGA hardware design
- FPGA system implementation and debugging
- Embedded software development
- Mixed-signal circuit simulation
- Signal integrity analysis
- PCB manufacturing

How to install Altium 2016

- Link to our download site:
<https://download.ece.ubc.ca>
- Create an Altium Live account:
<http://live.altium.com/#signin> (slow)
email: engservices@ece.ubc.ca (fast)



Electronic Software Distribution

Install .zip file

Search

Admin

- Groups
- Software
- Eligibility

History

- Previous Downloads
- Accepted Licenses

Help

- Login
- Eligibility
- ISO Files

ALTIUM DESIGNER

Circuit Design Software

External Links

- [Altium](#)
- [Altium Designer](#)

- [Summer 09 Release](#)
- [10](#)
- [2014](#)
- [16](#)

ALTIUM DESIGNER 16

File	Size	
README.html		README
AltiumDesigner16Setup.exe	10.4 MB	Windows installer (requires
EULA.pdf	56.2 KB	End-User License Agreement
OfflineSetupAD16_1_9.zip	3 GB	Windows installer



USING THE ECE LICENSE SERVER

The ECE license server for Altium is accessible only from the UBC network. Before starting Altium, you should be connected by one of the following means:

- A wired connection on the ECE network
- A wired connection on UBC ResNet
- A wireless connection at the UBC Vancouver campus on the ubcprivate, ubcsecure, or ubc network (ubcvisitor and eduroam are not sufficient)
- A [myVPN](#) connection to the UBC Vancouver network
- A myVPN connection to the ece.prof pool

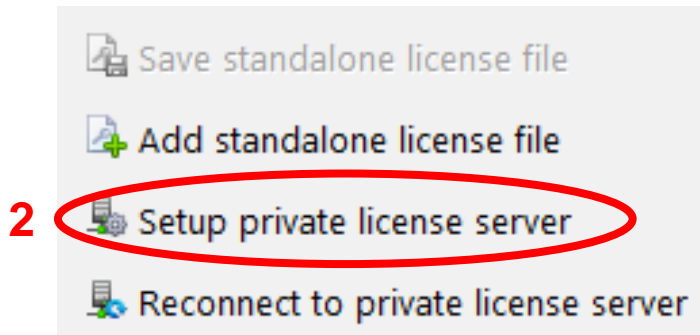
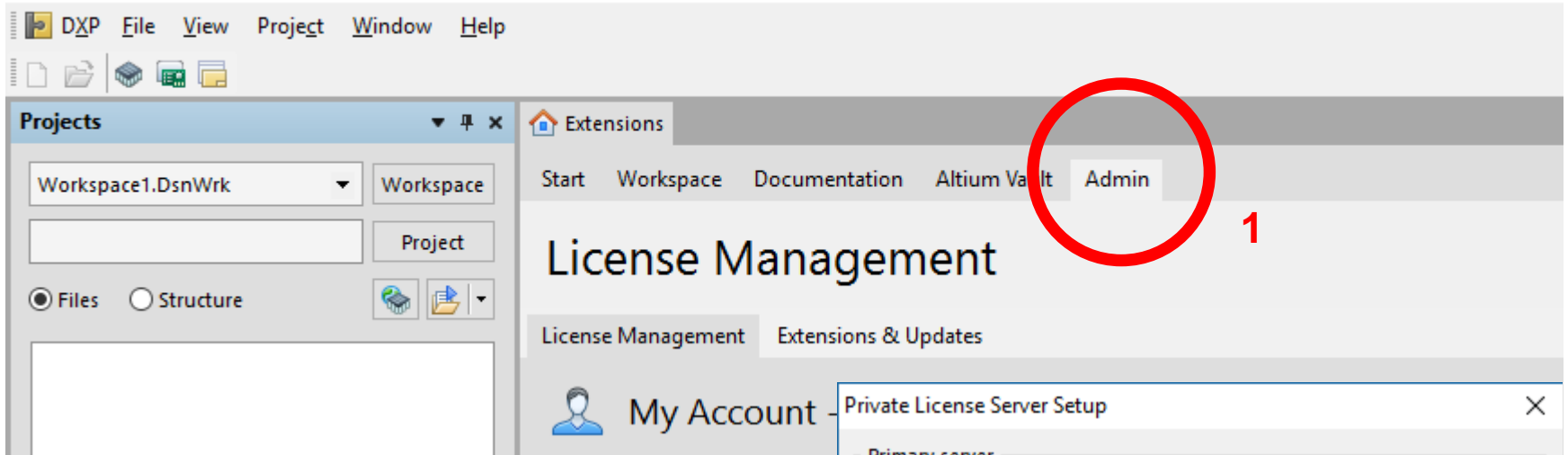
Start Altium, and from your "My Account" page, click on "Setup private license server". Enter:

Server name:	See file: README.html
Server port:	
Secondary server name:	
Server port:	

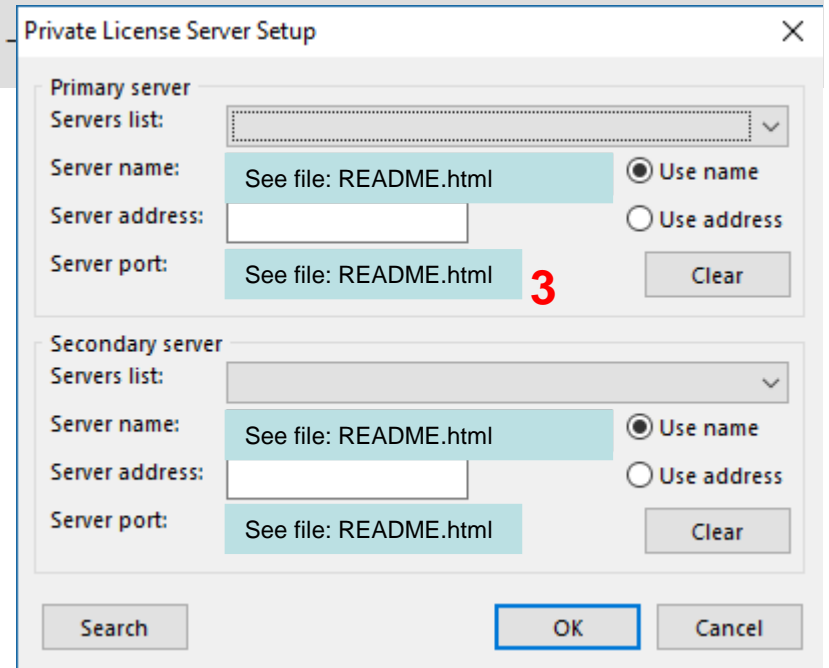
Select the new license that appears and click on "Use". You may as well also delete any old, expired licenses that are also showing.

To set license server

Altium Designer (16.1) - Workgroup [Workspace1.DsnWrk] - DXP://Extensions?Updates - Free Documents.

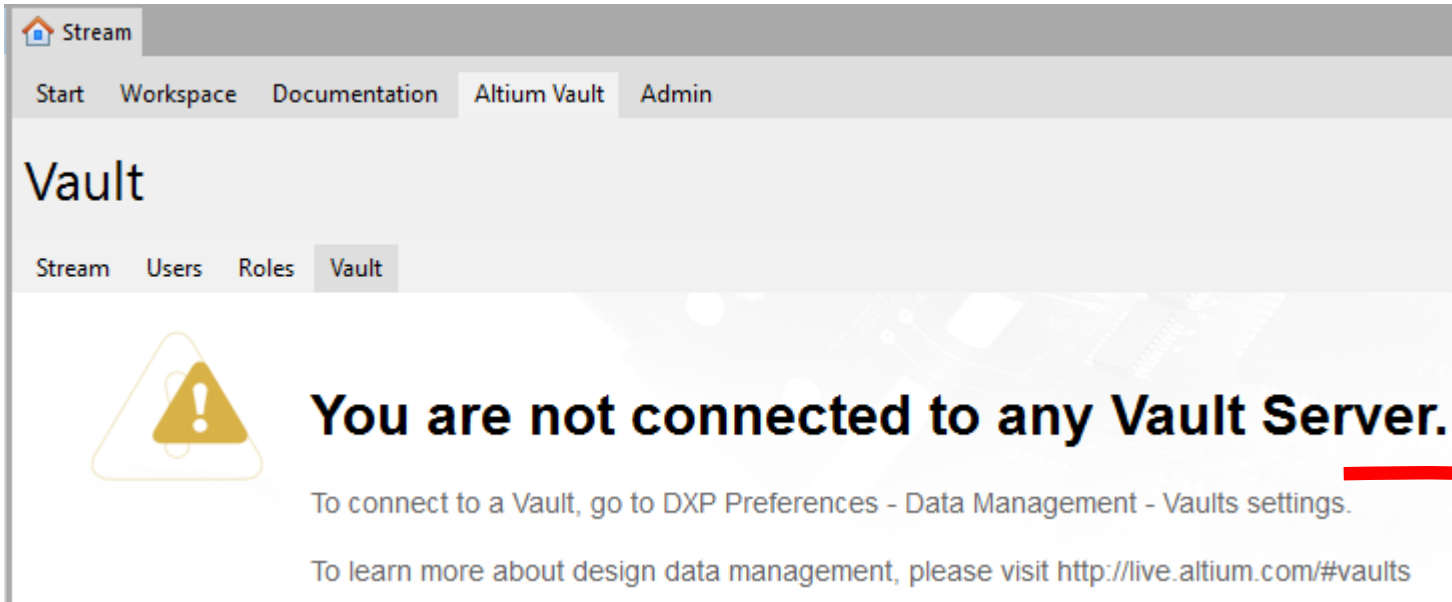


If you loose connection to server click here:



As per README.html file

Connecting to the Altium Vault




Stream

Start Workspace Documentation **Altium Vault** Admin

Vault

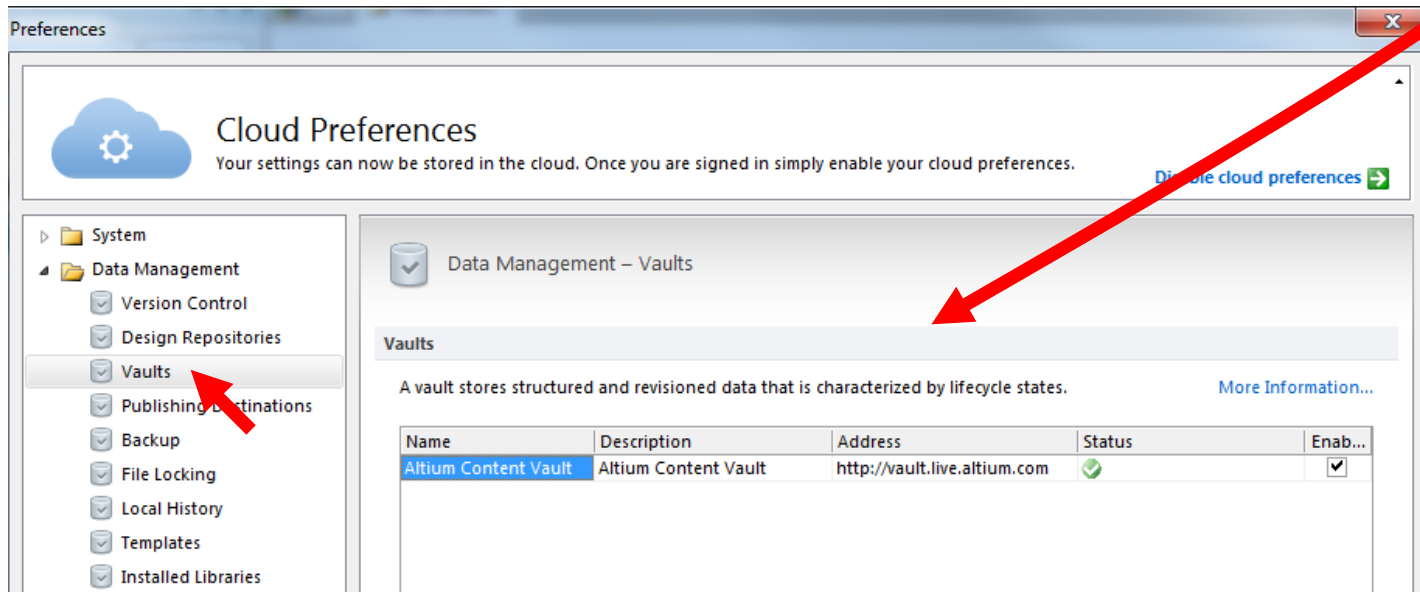
Stream Users Roles **Vault**



You are not connected to any Vault Server.

To connect to a Vault, go to DXP Preferences - Data Management - Vaults settings.

To learn more about design data management, please visit <http://live.altium.com/#vaults>



Preferences

Cloud Preferences

Your settings can now be stored in the cloud. Once you are signed in simply enable your cloud preferences. [Disable cloud preferences](#) →

- System
 - Data Management
 - Version Control
 - Design Repositories
 - Vaults**
 - Publishing Destinations
 - Backup
 - File Locking
 - Local History
 - Templates
 - Installed Libraries

Data Management – Vaults

Vaults

A vault stores structured and revisioned data that is characterized by lifecycle states. [More Information...](#)

Name	Description	Address	Status	Enab...
Altium Content Vault	Altium Content Vault	http://vault.live.altium.com	✓	<input checked="" type="checkbox"/>

Understanding Altium

- DXP (Design explorer): Unified platform
- Collaborative environment (corporate tool):
 - Multiple users, some with dedicated tasks
 - Design team incremental changes day-by-day
 - Built-in version control (SVN subversion or CVS concurrent versions system)
 - Design repositories / **Vaults** (accessible by multiple users with different credentials)
- Cloud oriented support:
 - Save preferences online
 - <http://live.altium.com/> (forum, design content, blog)

Altium Design Environment

Altium Designer

Menus/Toolbars/Shortcuts
Resources change according to the active document editor.

System Menu
Access to features including environment preferences and server information.

Document Tabs
Each open document has its own tab. Click on a document tab to make it the active document. Right-click on a tab for further controls.

Navigation
Provides controls for jumping to a particular document, stepping back and forth through viewed documents, and accessing the Home page.

Workspace Panels
Various panels provide functionality specific to a particular editor, or at a system level. Panels can be docked, placed in a 'pop-out' mode, or floating.

Main Design Window
Display and arrange open documents in this window.

Panel Access
Workspace panels are accessible using these buttons.

System Information Panel

Host Site	Top Level	Altium Designer
Project Name	PB01 - Audio/Video Peripheral B1	6.17.2014 10:00 AM
Host	AM	Project: D:\C1A-986
Host	AM	Project: E7

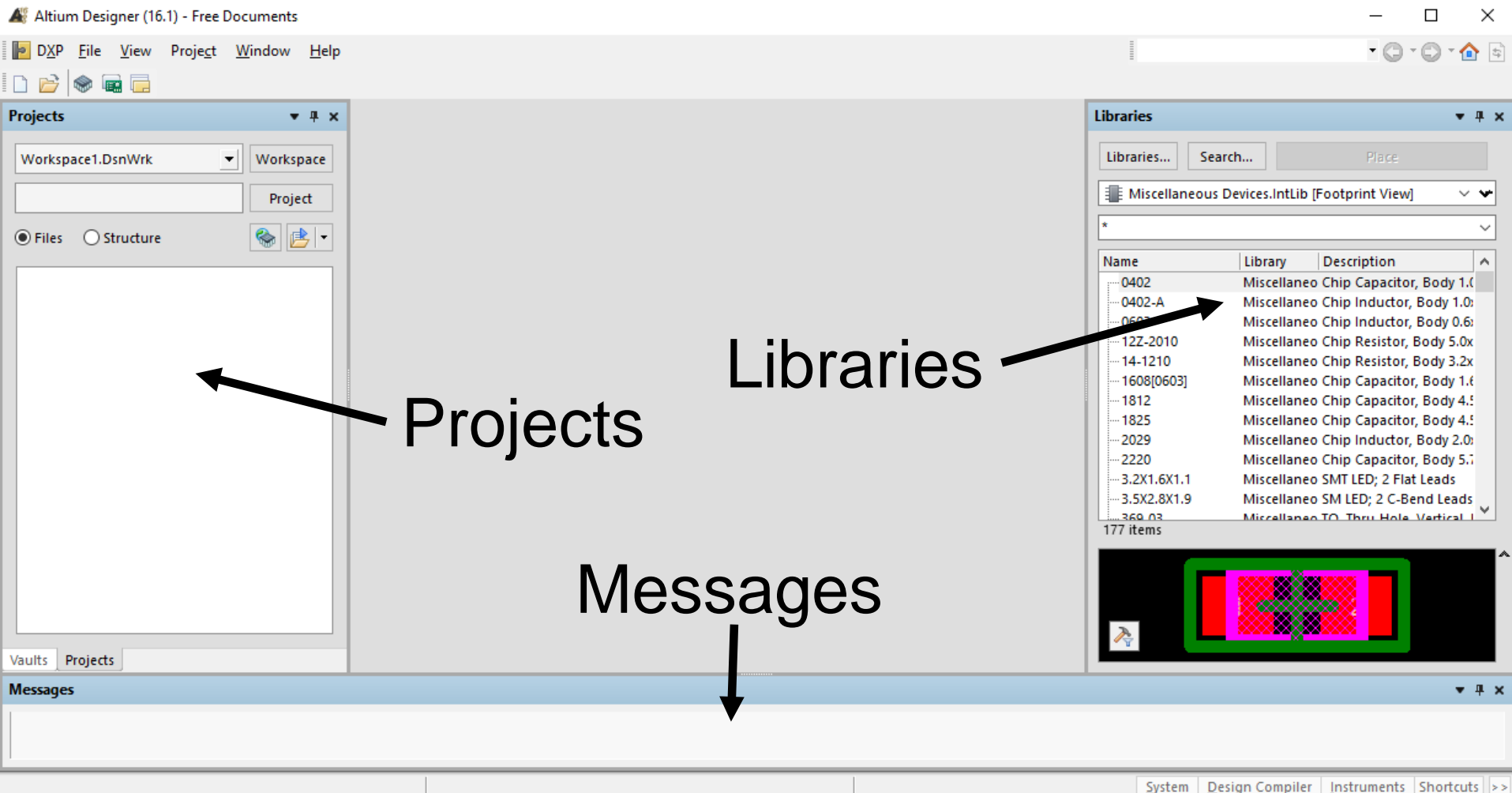
Altium

Navigator | SCH Filter | Projects | Editor

X:565 Y:45 Grid 5

Design Compiler | System | SD1 | Help | Soft Devices | >>

Recommended basic panels



For more help working with panels read [this](#)

Understanding Altium

(Basics for the single user)



Don't forget:

- Use Keyboard shortcuts
<Shift + F1> while running a command
- <Esc> or Right Click to exit a command
- Save documents to see some changes take effect

Altium Projects

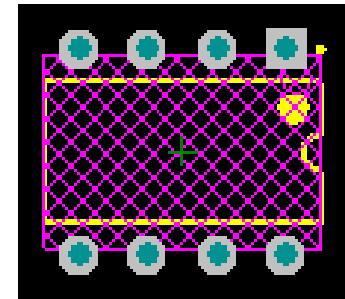
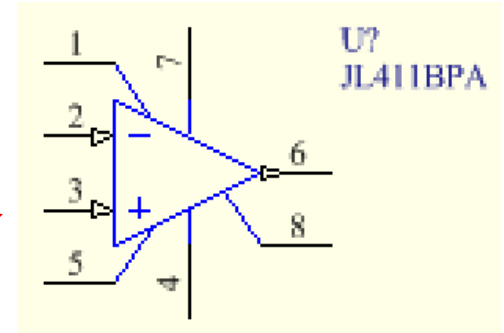
- Project: collection of design documents
 - 1 Project = 1 implementation
 - It stores links to all source documents
 - relative reference: same drive
 - absolute reference: different drive
 - It creates links to all output documents
 - Saves project options
- Create a PCB_Project, Save as: new name
(does not move the file creates a copy)
- The active project is highlighted
- Add/Remove documents to/from a project

Project types

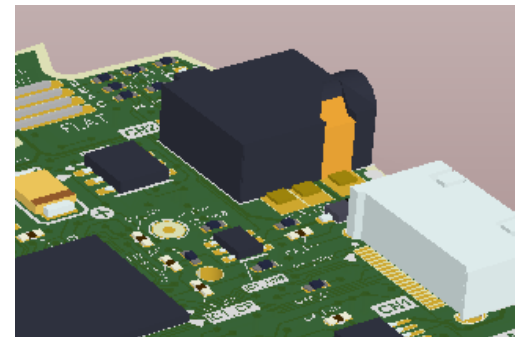
- PCB Project (*.PrjPcb)
 - Schematic, libraries, PCB layout
- FPGA Project (*.PrjFpg)
- Embedded Project (*.PrjEmb)
- Core Project (*.PrjCor)
- Integrated Library (*.LibPkg) & (*.IntLib)
- Script Project (*.PrjScr)

Component, Model and Library Concepts

- Component representations:
 - Schematic symbol
 - PCB footprint
 - SPICE model definitions
 - Signal integrity description
 - 3D graphical description



```
*****INPUT STAGE*****
*
IOS 2 1 25.0P
*^Input offset current
CI1 1 0 3P
CI2 2 0 3P
R1 1 3 1E12
R2 3 2 1E12
I1 99 4 1.0M
J1 5 2 4 JX
J2 6 7 4 JX
R3 5 50 650
R4 6 50 650
*Fp2=28 MHZ
G1 5 6 4 3700
```



Libraries = collections of components

- Collection of components, models or both
- **Model Libraries** (*.MDL, *.CKT, *.PCBLib)
 - Simulation models are one file per model
- **Schematic Libraries** (*.SchLib)
 - Symbol and a link to a model library
- **Integrated Libraries** (*.IntLib)
 - Unified components: Symbol, footprint and other domain models + parametric information are compiled into a single portable file

To setup libraries in Altium

Libraries panel

Available Libraries Dialog

Libraries

Libraries... Search... Place 2N3904

Miscellaneous Devices.IntLib [Component View]

Component Na...	Description	Footprint
2N3904	NPN General Purpose Amp TO-92A	
2N3906	PNP General Purpose Ampl TO-92A	
ADC-8	Generic 8-Bit A/D Converte SOT403-1_N	
Antenna	Generic Antenna	PIN1
Battery	Multicell Battery	BAT-2
Bell	Electrical Bell	PIN2
Bridae1	Full Wave Diode Bridge	D-38

195 components

Q?
2N3904

Model Name	Model Type	Source
2N3904	Signal Integrity	
2N3904	Simulation	2N3904.mdl
TO-92A	Footprint	Miscellaneous Devic

Available Libraries

Project Installed Search Path

Installed Libraries	Activated	Path	Type
Miscellaneous Devices.IntLib	<input checked="" type="checkbox"/>	Miscellaneous Devices.IntLib	Integrated
Miscellaneous Connectors.IntLib	<input checked="" type="checkbox"/>	Miscellaneous Connectors.IntLib	Integrated
FPGA 32-Bit Processors.IntLib	<input type="checkbox"/>	FPGA\FPGA 32-Bit Processors.IntLib	Integrated
FPGA Configurable Generic.IntLib	<input type="checkbox"/>	FPGA\FPGA Configurable Generic.IntLib	Integrated
FPGA DB Common Port-Plugin.IntLib	<input type="checkbox"/>	FPGA\FPGA DB Common Port-Plugin.IntLib	Integrated
FPGA Generic.IntLib	<input type="checkbox"/>	FPGA\FPGA Generic.IntLib	Integrated
FPGA Instruments.IntLib	<input type="checkbox"/>	FPGA\FPGA Instruments.IntLib	Integrated
FPGA Memories.IntLib	<input type="checkbox"/>	FPGA\FPGA Memories.IntLib	Integrated
FPGA NB2DSK01 Port-Plugin.IntLib	<input type="checkbox"/>	FPGA\FPGA NB2DSK01 Port-Plugin.IntLib	Integrated

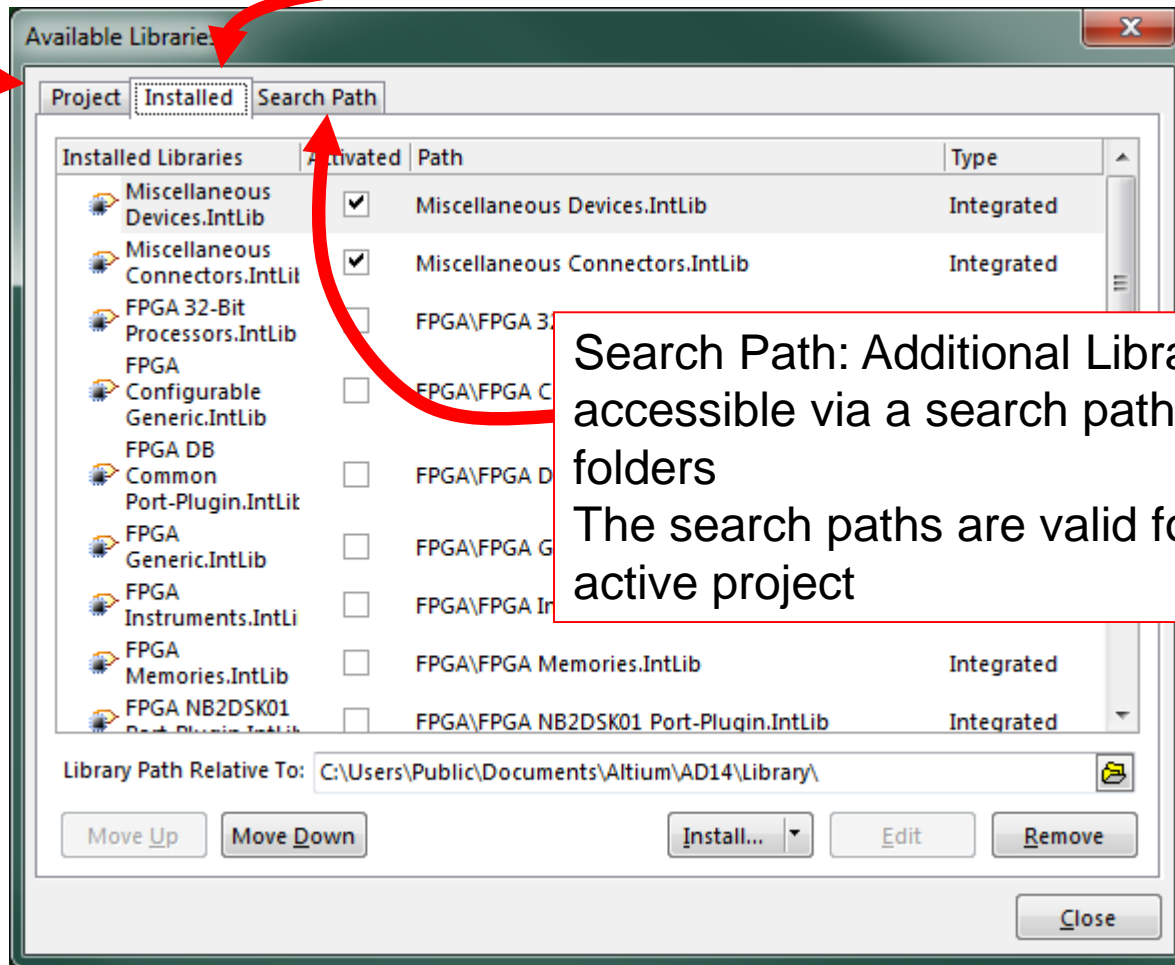
Library Path Relative To: C:\Users\Public\Documents\Altium\AD14\Library\

Move Up Move Down Install... Edit Remove

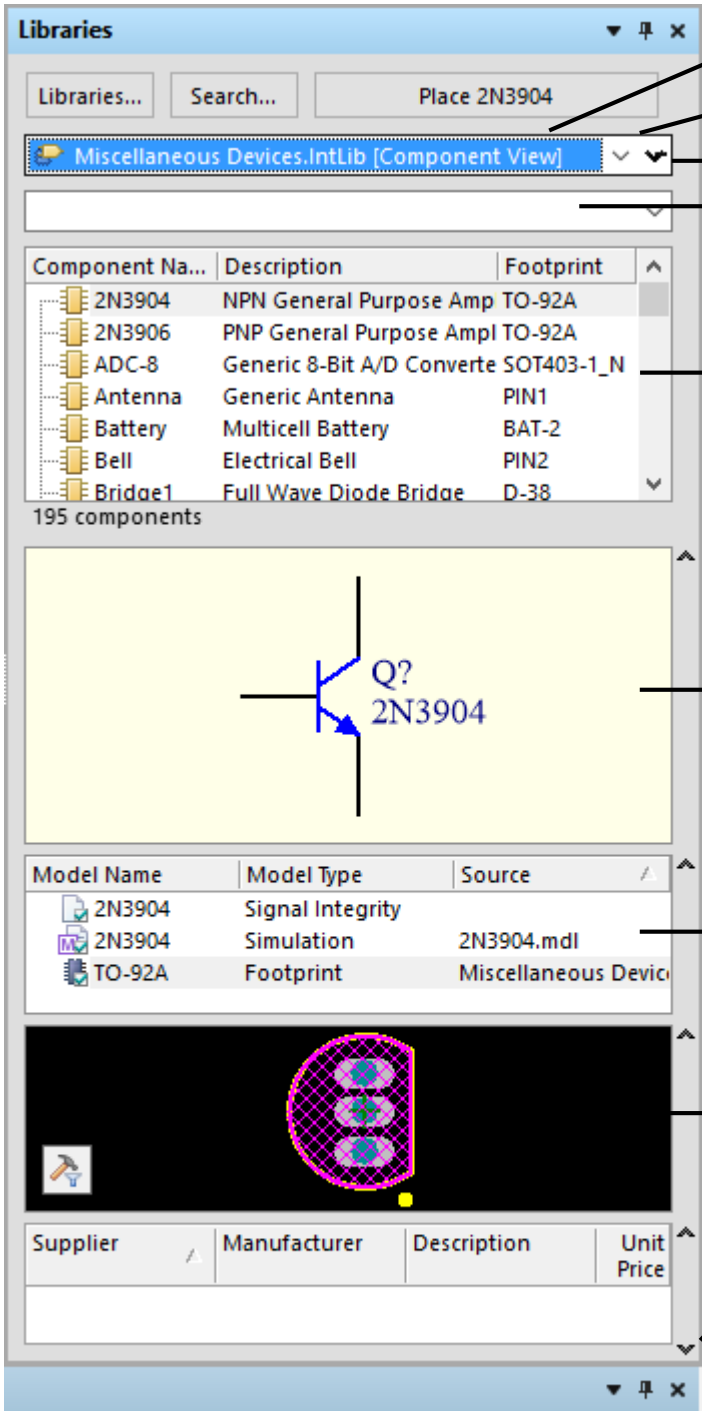
Close

Project: part of and available only to the active project and its documents
You have to keep track of where these are if you move the project files

Installed: All installed libraries.
Components are available to all open projects and list is persistent across design sessions



Search Path: Additional Libraries accessible via a search path and sub-folders
The search paths are valid for the active project



Current library

Select a different library

Set library browse mode

Search in current library

List of components.
Select the component of interest

Schematic symbol for selected component

Models linked to the selected component

Graphical display of the selected model

Icons used to show/hide panel sections

Libraries Panel:

All libraries available to the active project

Project + Installed + Search Path

When placing component:

<spacebar> to rotate

<x> or <y> to flip

<Tab> open properties dialog

<L> for PCB footprints
to flip component side

To search across libraries:

Search ...

Obtaining integrated libraries

1. Frozen (legacy) libraries: [from here](#)

you can install anywhere but it is a good idea to make a subfolder under:

C:\Users\Public\Public Documents\Altium\AD16\Library
or a cloud storage service if you work from more than one PC

2. AltiumLive website: [Resources / Design Content](#)



Manufacturer: **National Semiconductor**

Updated: 3+ months ago

Tags: Analog, Amplifier

National Semiconductor Amplifiers. This collection offers amplifiers from single to quad, up to 1.7GHz with low-distortion, low-power and low-voltage options.

GO TO VAULT

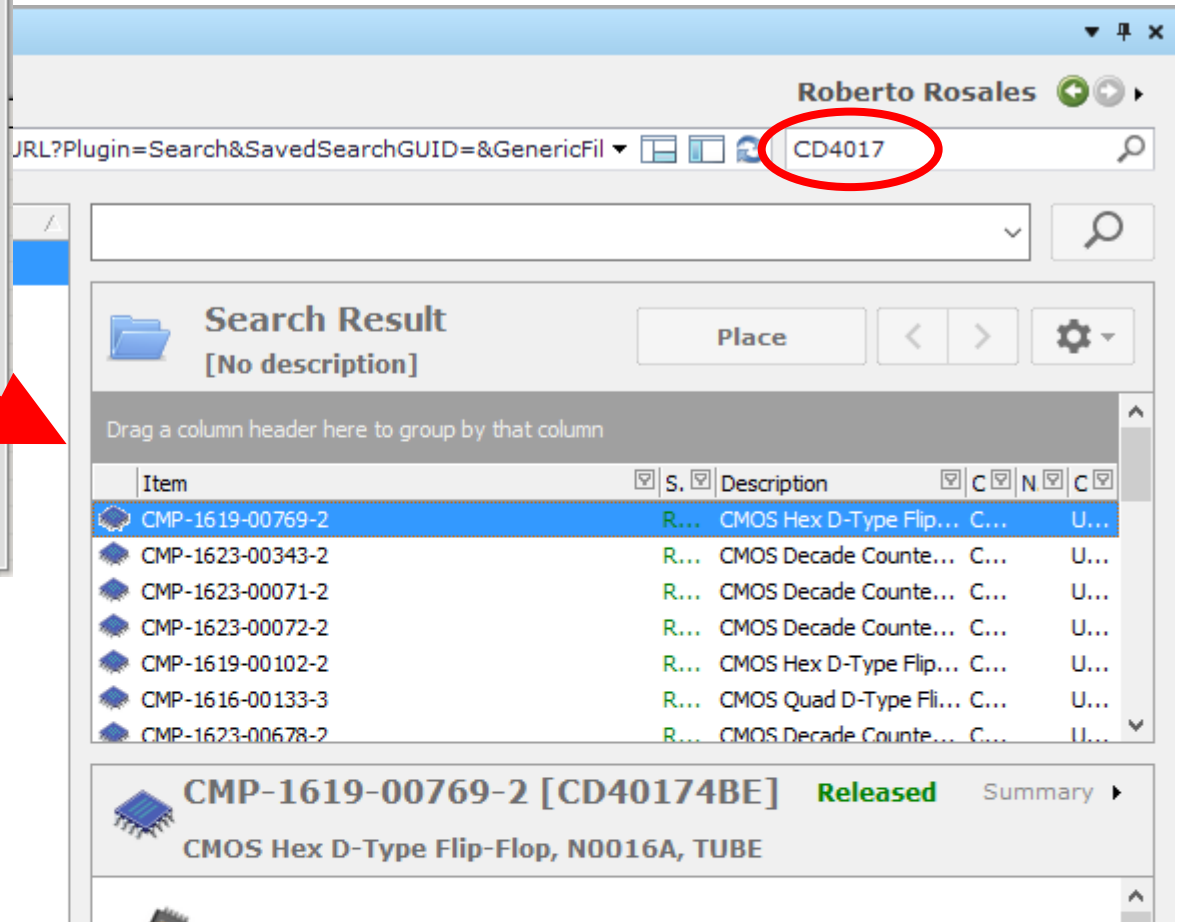
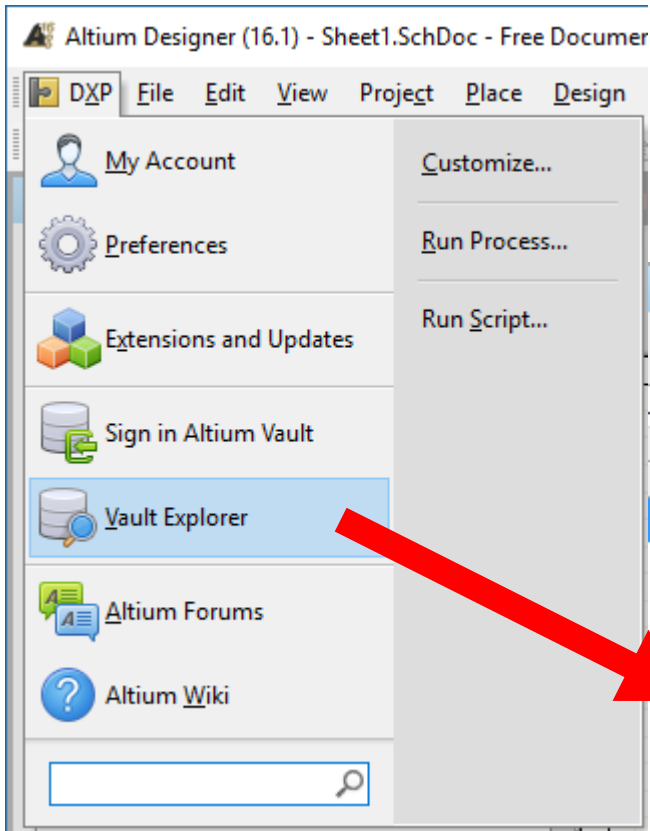
DOWNLOAD LIBRARY

This is useful to
preview component

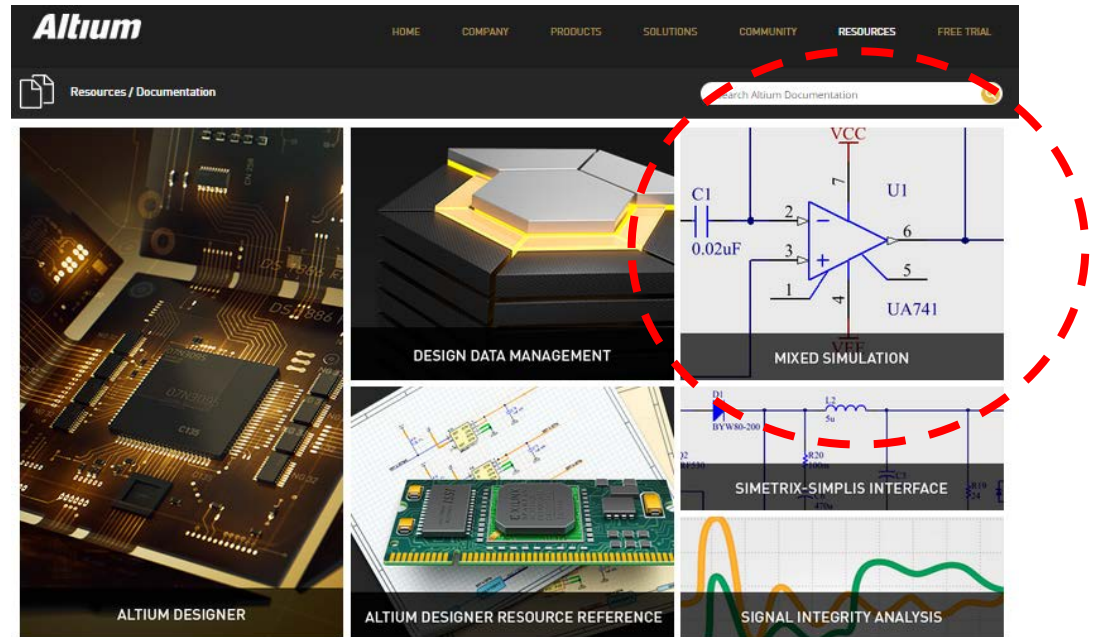
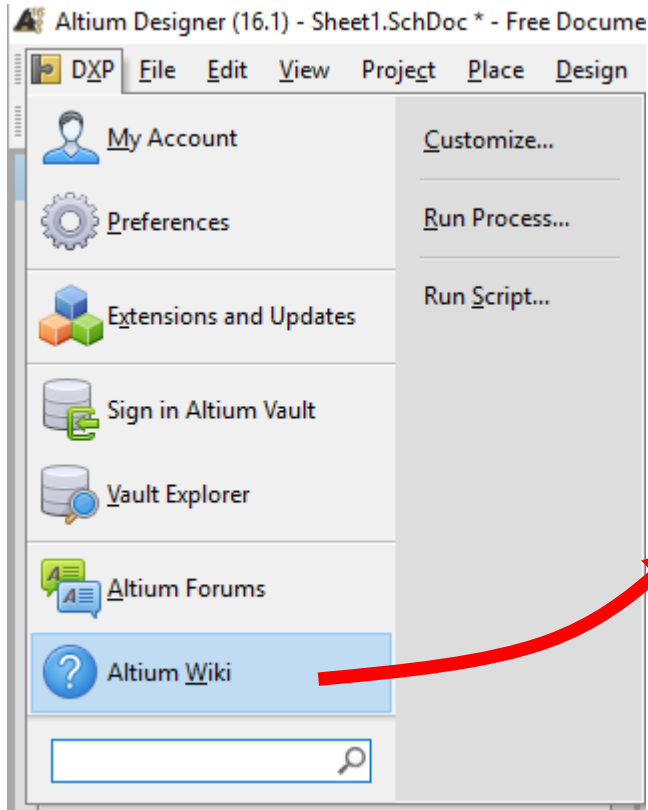
This downloads a
.zip file for the complete
library

Altium Vault

Altium's cloud library (repository of models)
Also includes real-time supply chain information



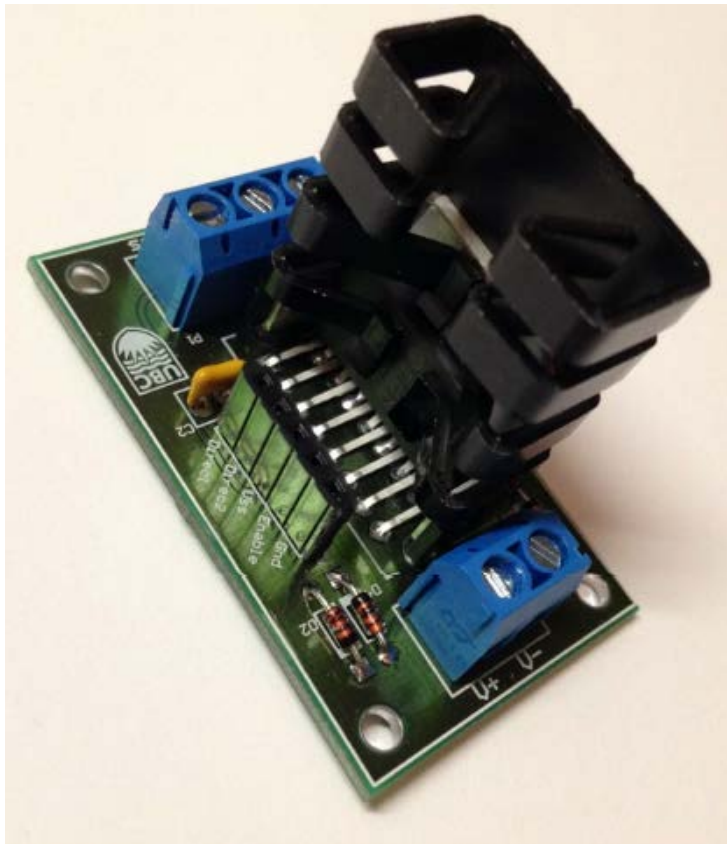
Learning to use Altium



Best training material is on the Altium website
It is updated, but beware that menus and options
slightly change between versions

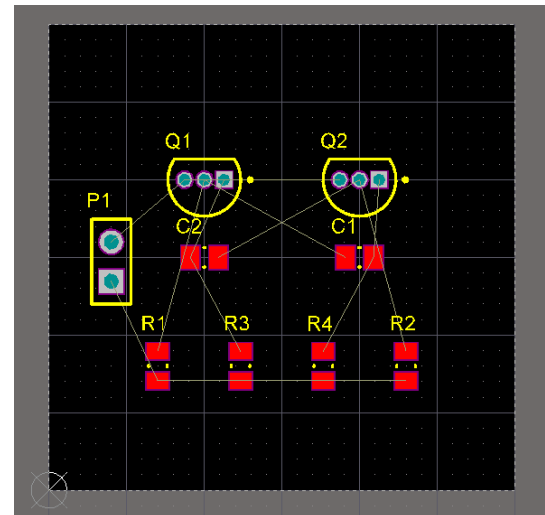
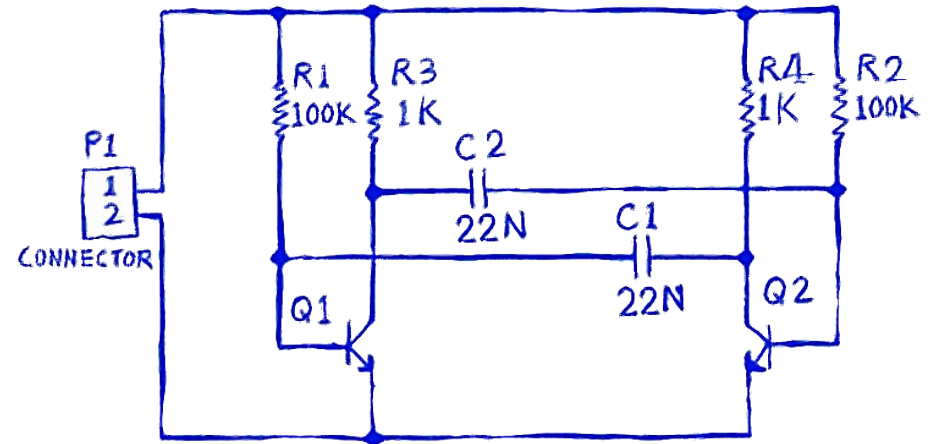
Walk-through example

L298 Motor Driver Board
(by Matt Winship)



[L298 Motor Driver Board Datasheet.pdf](#)

[Altium introductory tutorial](#)



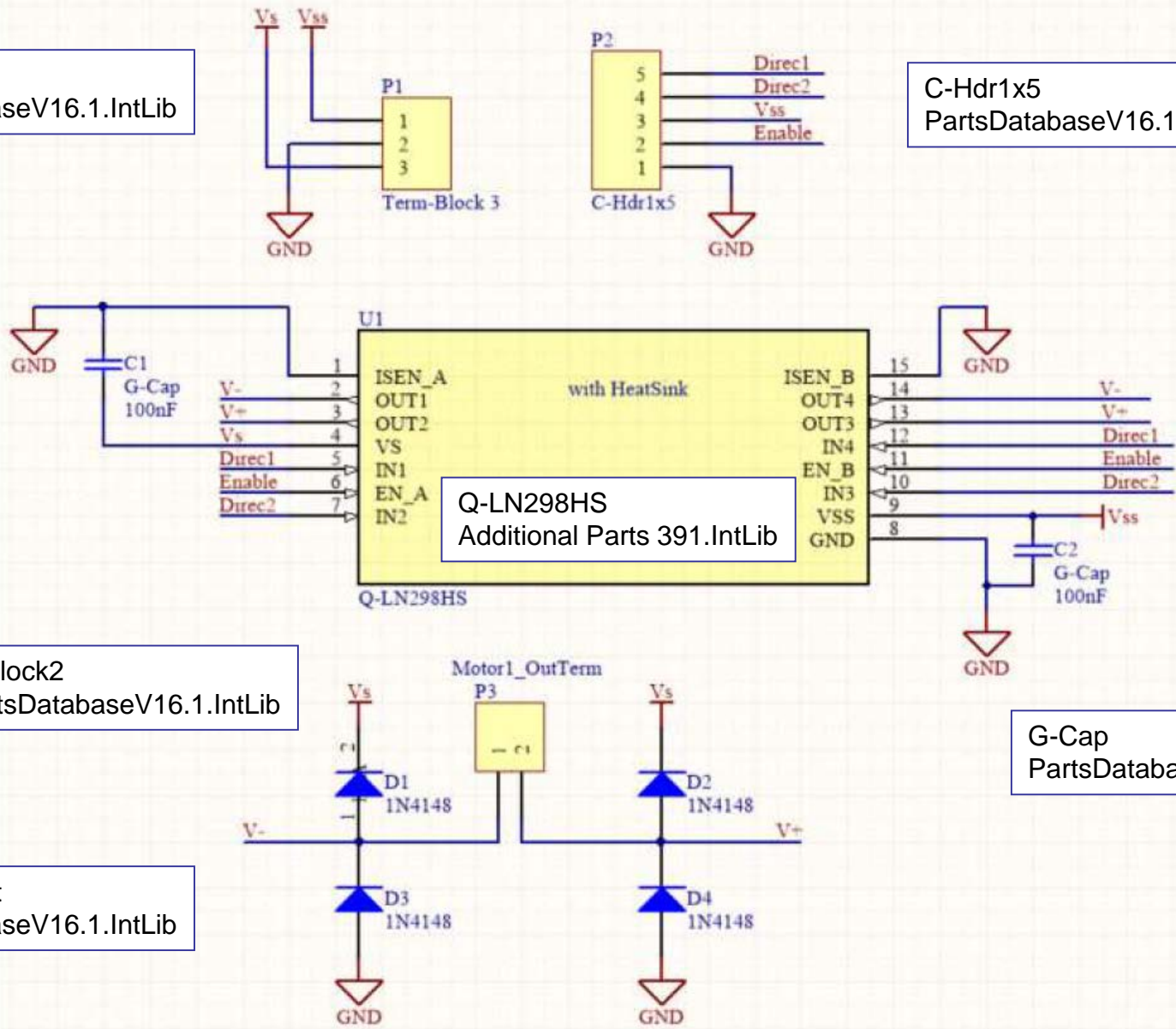
LM298 Motor Driver Board Schematic

1. Load libraries
2. Draw the schematic
Set electrical type for connector pins
3. Compile Project:
Project → Project Options
4. Place 'no ERC' labels if necessary
Modify connection matrix with caution

LM298 Motor Driver Board Schematic

C-Block3
PartsDatabaseV16.1.IntLib

C-Hdr1x5
PartsDatabaseV16.1.IntLib

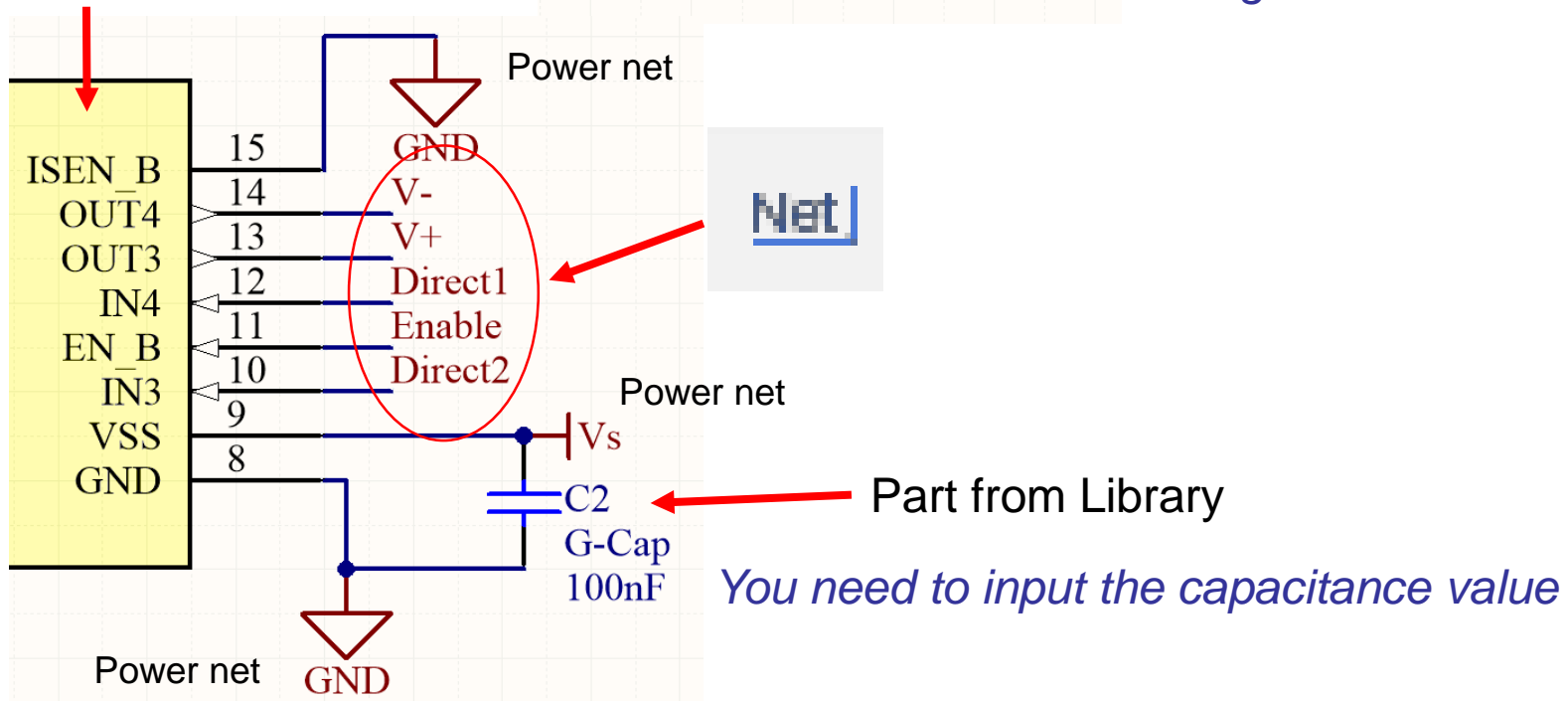
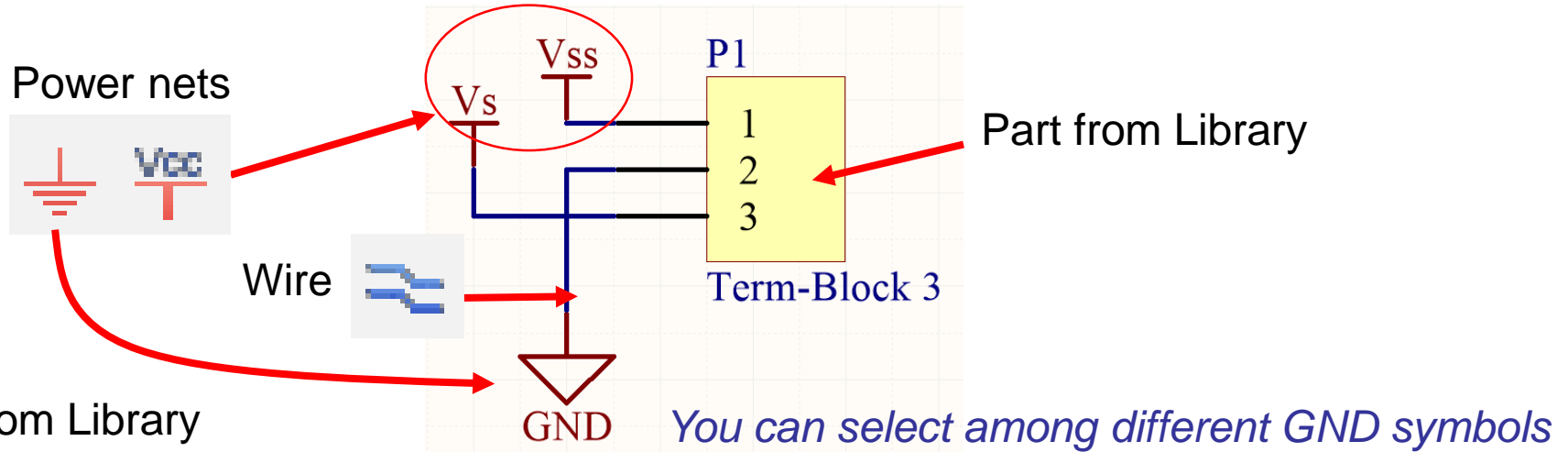


C-Block2
PartsDatabaseV16.1.IntLib

G-Cap
PartsDatabaseV16.1.IntLib

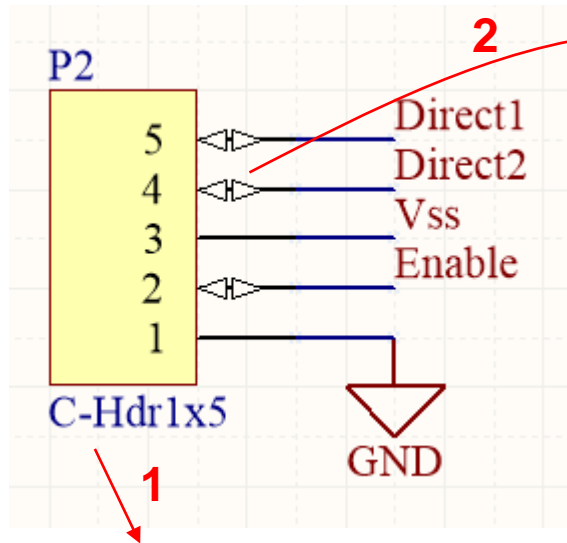
T-DiodeRect
PartsDatabaseV16.1.IntLib

Drawing the schematic



Set the electrical type of pins

On the Q-LN298HS Symbol, pins Direc1, Direct2, and Enable are inputs
You need to set the pins of connector P2 to Output, or I/O, to provide a compatible electrical type net



Pin Properties

Logical Parameters

Display Name Visible

Designator Visible

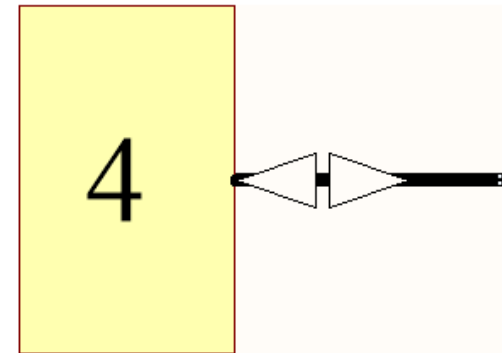
Electrical Type

Description

Hide Connect To

Part Number

Select pin, change electrical type



Properties

Graphical

Location X Y

Orientation

Mode

Lock Pins Mirrored

Show All Pins On Sheet (Even if Hidden)

Local Colors

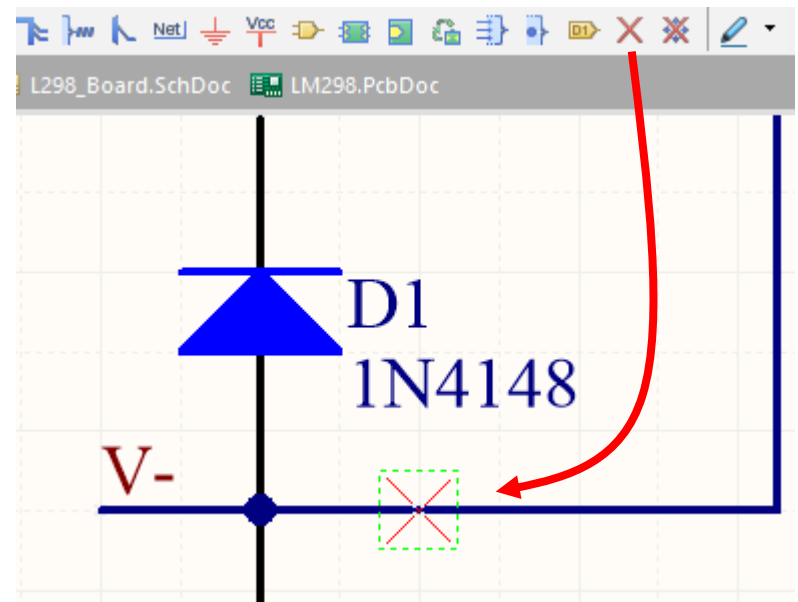
Unlock pins

Compile Project

- Project >> Compile Project

Class	Document	Source	Message
[Error]	LM298.SchDoc	Compiler	Net V- contains multiple Output Pins (Pin U1-2,Pin U1-14)
[Error]	LM298.SchDoc	Compiler	Net V+ contains multiple Output Pins (Pin U1-3,Pin U1-13)

- This error is caused by having 2 pins of the LM298 connected to V- and 2 pins connected to V+
- In this case this was done intentionally
- To ignore this error place a No ERC label on the net



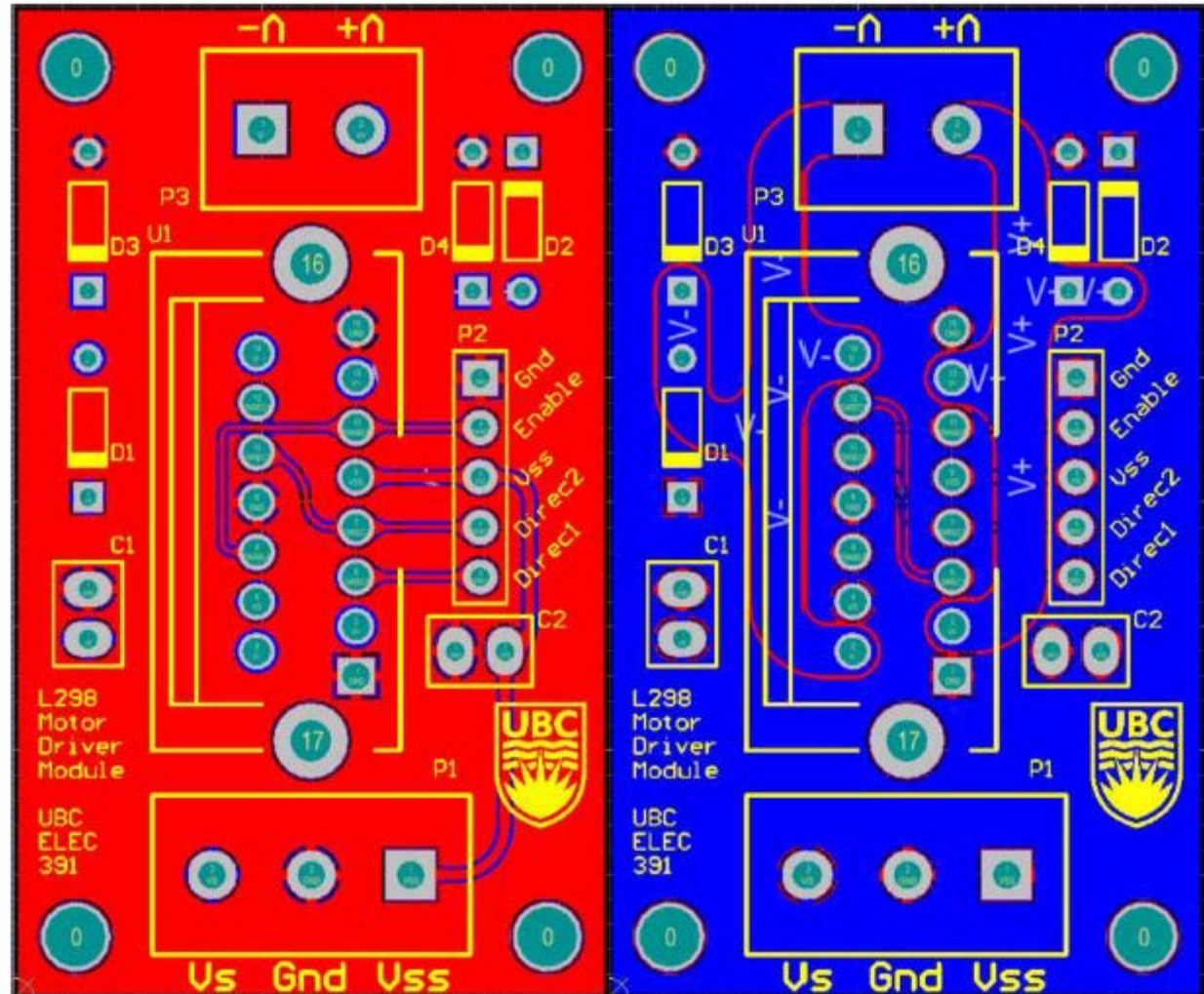
Wiring Tips

- Left-click or <Enter> to anchor the wire at the cursor position.
- <Backspace> (←) to remove the last anchor point.
- <Spacebar> to toggle the direction of the corner.
- <Shift+Spacebar> to cycle through all possible corner modes.
- Right-click or <Esc> to exit wire placement mode.
- To graphically edit the shape of a wire, Click once to select it first, then Click and hold on a segment or vertex to move it.
- Whenever a wire crosses the connection point of a component, or is terminated on another wire, a junction will automatically be created.
- A wire that crosses the end of a pin will connect to that pin, even if you delete the junction.
- To move a placed component and drag connected wires with it, hold down the Ctrl key while moving the component, or select Move » Drag.

LM298 Motor Driver Board Layout

Board Layout

- Size 1.2" x 2.1"
- 2 layers
- Mounting holes
- Thick traces for V- and V+
- Power planes for Vs and GND



Top Metal

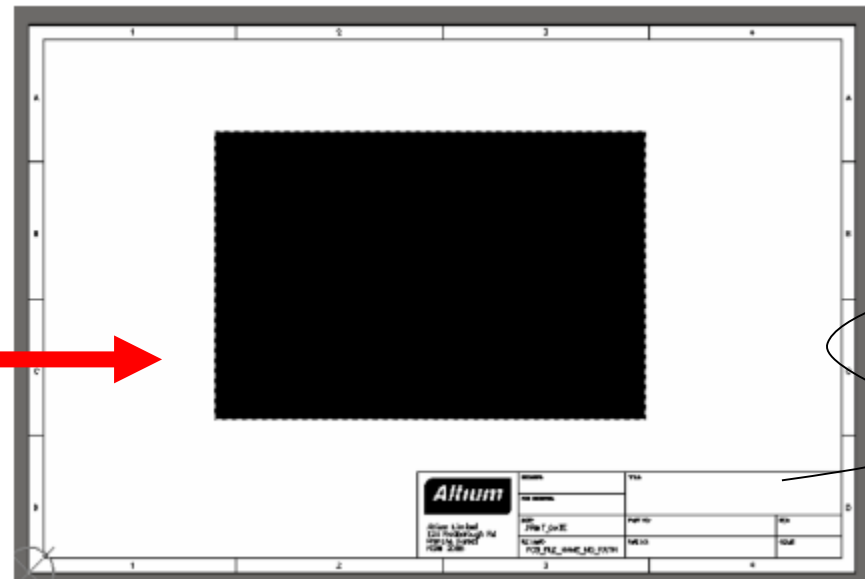
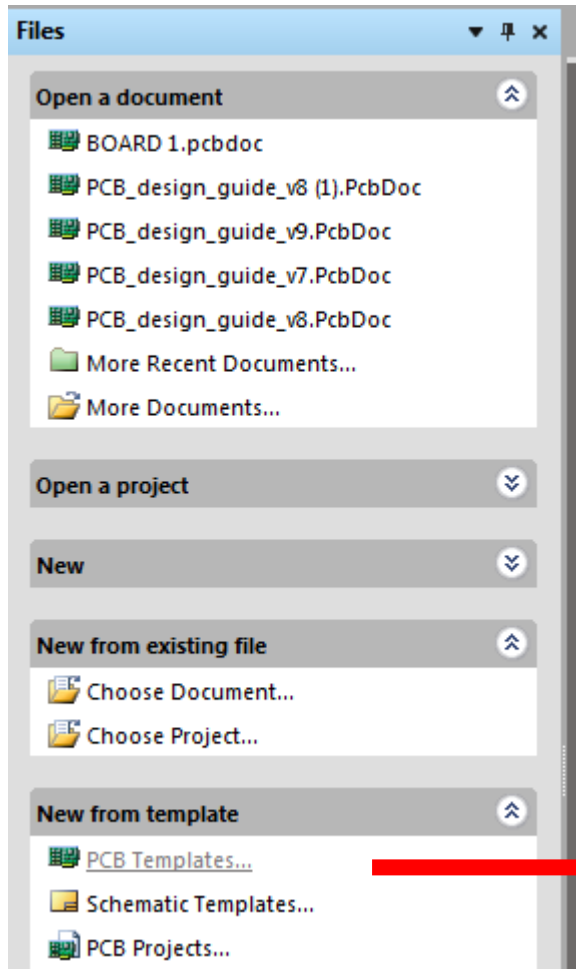
Bottom Metal

2 starting points for PCB design

1. From a companion schematic package
 - Prepare project schematics
 - Import schematic design
 - Component footprints are added automatically
 - Connectivity is indicated with rats nests
 - Net names are imported from the schematic
2. Directly from the PCB editor
 - You need to select and place manually each component footprint from a library
 - No rats nest – connectivity
 - You must assign nets manually (at least GND)

Creating a New Board from a template

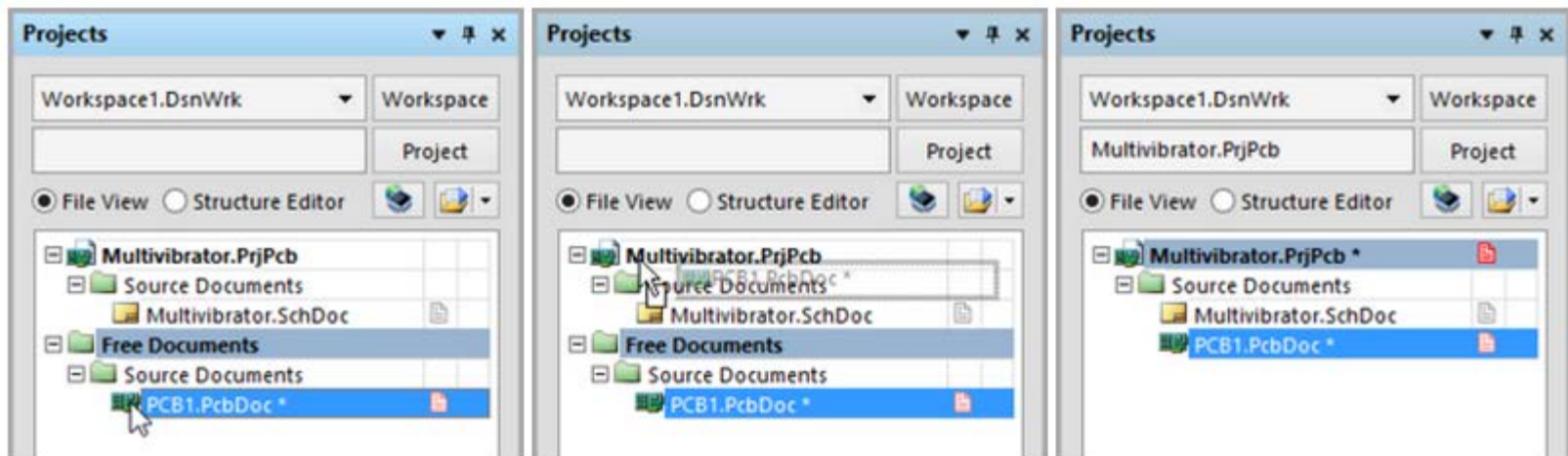
- Files Panel:
 - New from template
 - select the A4.PcbDoc template
 - Save as ... same name and directory as SchDoc file



Mechanical 16

Adding PCB file to project

- Make the PCB board part of the project

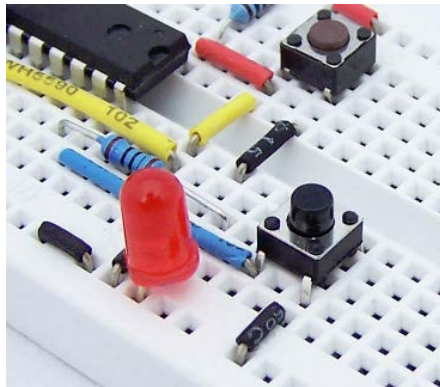


- Rename the file
- Save the PcBDoc file and the project

First things first ... choosing working units

- Imperial (inches)

- 1/1000th of an inch = 1 mil = 1thou
- 100mils (0.1") is a common dimension



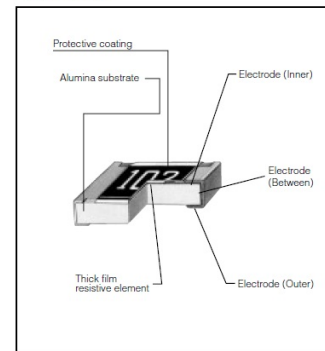
- Metric (mm)

- 1 mm ≠ 1mil !
- Common unit in SM parts

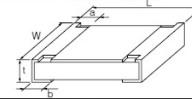
Panasonic

Thick Film Chip Resistors

Construction



Dimensions in mm (not to scale)



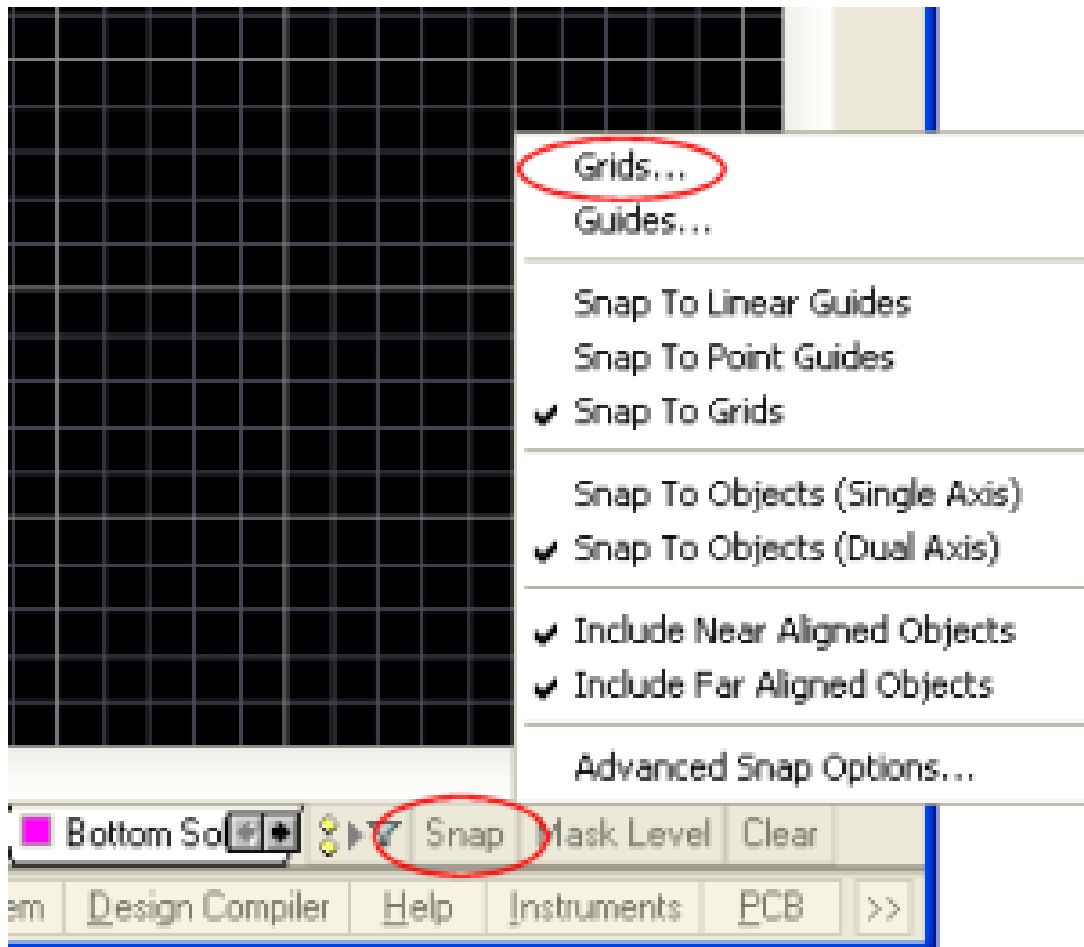
Type (inches)	Dimensions (mm)					Mass (Weight) (g/1000 pcs.)
	L	W	a	b	t	
ERJ6S (01005)	0.40 ^{+0.02}	0.20 ^{+0.02}	0.10 ^{+0.02}	0.10 ^{+0.02}	0.13 ^{+0.02}	0.04
ERJ6G (02011)	0.60 ^{+0.03}	0.30 ^{+0.03}	0.10 ^{+0.03}	0.15 ^{+0.03}	0.23 ^{+0.03}	0.15
ERJ6G (0402)	1.00 ^{+0.04}	0.50 ^{+0.04}	0.20 ^{+0.04}	0.25 ^{+0.04}	0.35 ^{+0.04}	0.8
ERJ6G (0603)	1.60 ^{+0.06}	0.80 ^{+0.06}	0.30 ^{+0.06}	0.30 ^{+0.06}	0.45 ^{+0.06}	2
ERJ6G (0805)	2.00 ^{+0.08}	1.25 ^{+0.08}	0.40 ^{+0.08}	0.40 ^{+0.08}	0.60 ^{+0.08}	4
ERJ6G (1206)	3.20 ^{+0.12}	1.60 ^{+0.12}	0.50 ^{+0.12}	0.50 ^{+0.12}	0.60 ^{+0.12}	10
ERJ14 (1210)	3.20 ^{+0.20}	2.50 ^{+0.20}	0.50 ^{+0.20}	0.50 ^{+0.20}	0.60 ^{+0.20}	16
ERJ12 (1812)	4.50 ^{+0.20}	3.20 ^{+0.20}	0.50 ^{+0.20}	0.50 ^{+0.20}	0.60 ^{+0.20}	27
ERJ12Z (2010)	5.00 ^{+0.20}	2.50 ^{+0.20}	0.60 ^{+0.20}	0.60 ^{+0.20}	0.60 ^{+0.20}	27
ERJ1T (2512)	6.40 ^{+0.20}	3.20 ^{+0.20}	0.65 ^{+0.20}	0.60 ^{+0.20}	0.60 ^{+0.20}	45

- Remember: 100mils = 2.54mm

- To switch units in Altium Press <Q>

First things first ... setting the snap grid

- PCBs are grid based objects

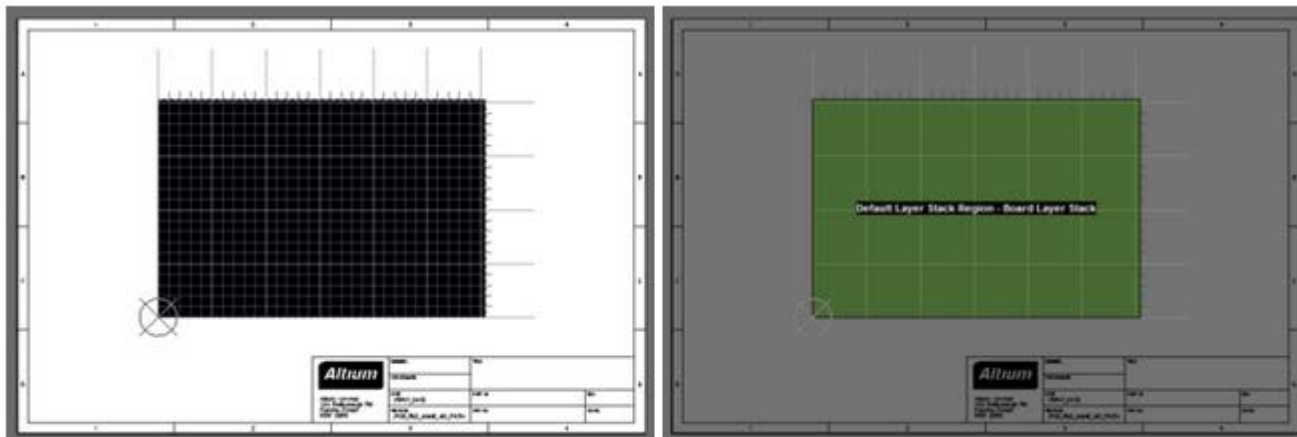


Unified Cursor-Snap System

- Selecting a suitable snap grid:
 - <Ctrl>+<G>
 - Start with a coarse grid to define board size

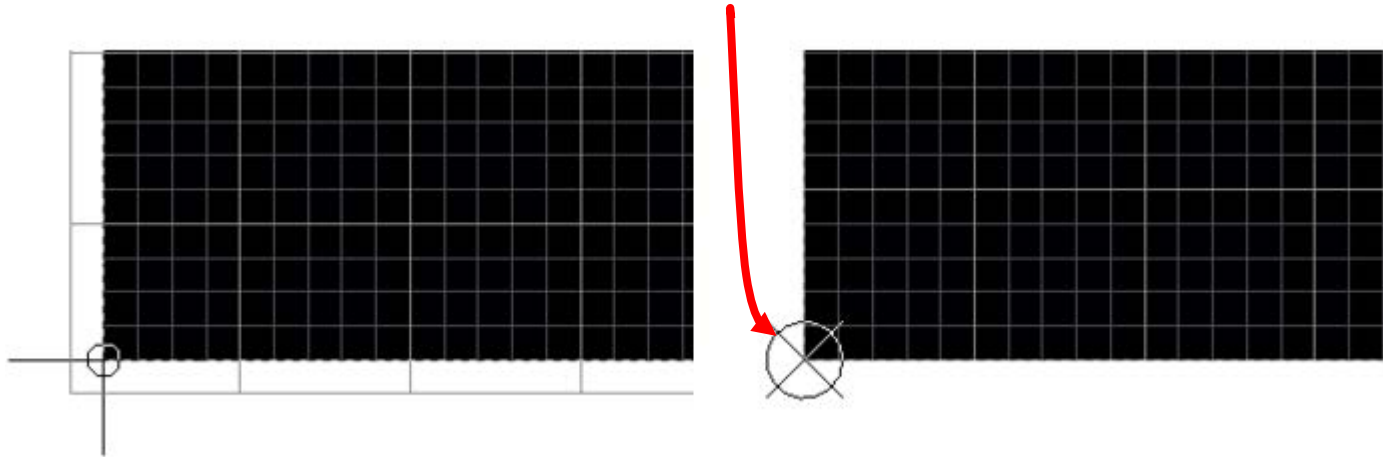
First things first ... redefining the board shape

- Viewing modes:
 - Board Planning Mode (1)
 - **Design » Edit Board Shape** (resize to 1.2" x 2.1")
 - **Design >> Move Board Shape** (Relocate the origin)
 - 2D Layout Mode (2)
 - 3D Layout Mode (3).



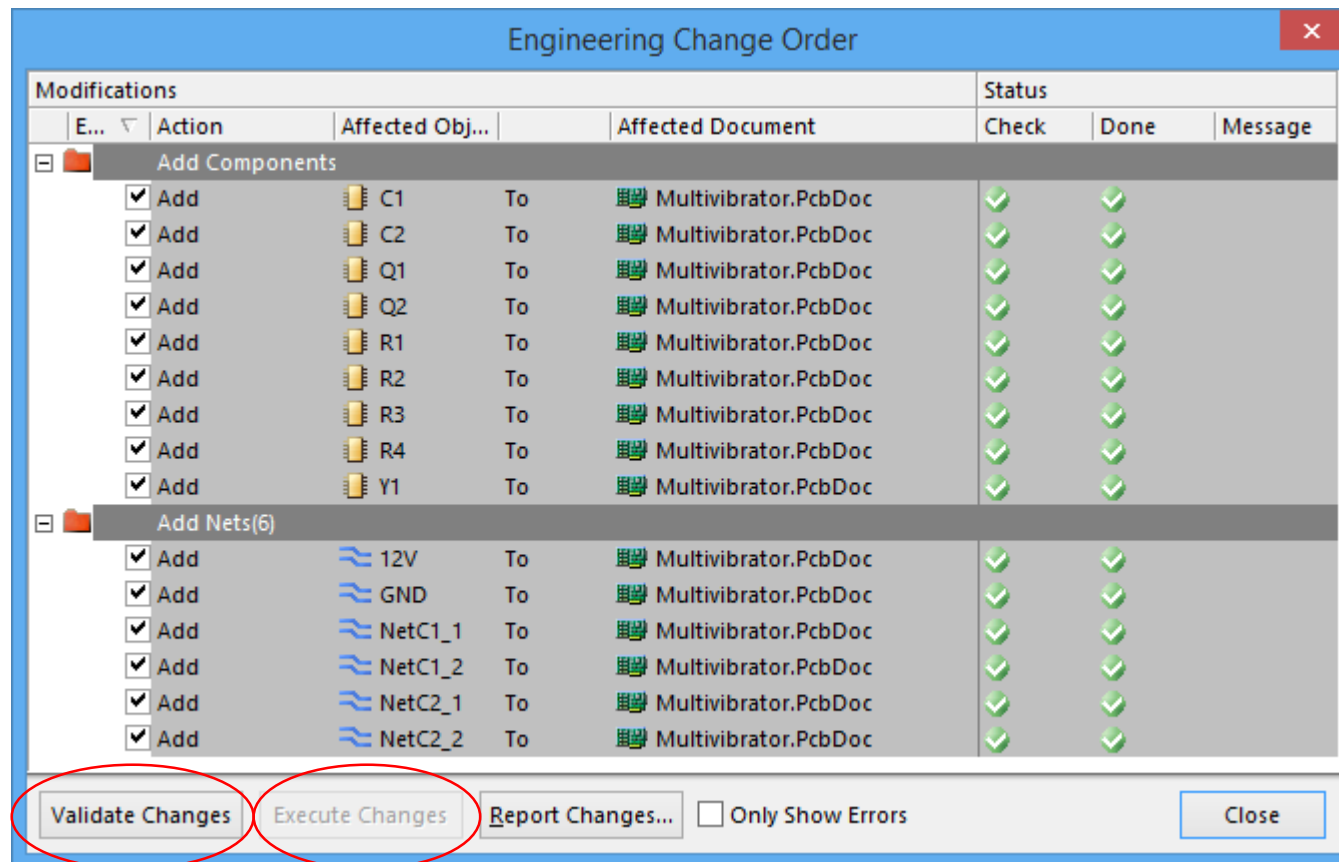
First things first ... setting the board origin

- Absolute origin (lower left corner)
- User-defined relative origin
 - Edit >> Origin >> Set



Design transfer

- Design transfer
 - On Schematic file
 - Design >> Update PCB Document ...



Design transfer

L298_Board.SchDoc L298_Board.PcbDoc

Rat's nests indicate connectivity as per schematic (Net names are assigned to part terminals)

All parts in the schematic with their selected footprints

Top Layer Bottom Layer Mechanical 1 Top Overlay Bottom Overlay Top Paste Bot Snap Mask Level

Configuring the Display Layers

- Design » Board Layers and Colors

View Configurations

Select PCB View Configuration

Name	Kind
Altium Standard 2D	2D simple
Altium Transparent 2D	2D simple
Tutorial	2D simple
Altium 3D Black	3D
Altium 3D Blue	3D
Altium 3D Brown	3D
Altium 3D Color By Layer	3D
Altium 3D Dk Green	3D
Altium 3D Lt Green	3D
Altium 3D Red	3D
Altium 3D White	3D

Path
C:\Users\robertor\AppData\Roaming\Altium\Altium Designer (24F8ECA1-33DC-412A-808C-0336F88BC8A6)\View Configurations\Altium Standard 2D.config_2dsimple

[Explore Folder ...](#)

Description
Altium Standard 2D

Actions

[Create new view configuration ...](#)

[Save view configuration](#)

[Save As view configuration ...](#)

[Load view configuration ...](#)

[Rename view configuration ...](#)

[Remove view configuration...](#)

2D Color Profiles Layer Pairs ...

Board Layers And Colors Show / Hide View Options Transparency

Signal Layers (S)	Color	Show	Internal Planes (P)	Color	Show	Mechanical Layers(M)	Color	Show	Enable	Single Layer Mode	Linked To Sheet
Top Layer (T)	Red	<input checked="" type="checkbox"/>				Mechanical 1	Magenta	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Bottom Layer (B)	Blue	<input checked="" type="checkbox"/>				Mechanical 13	Magenta	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
						Mechanical 15	Green	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
						Mechanical 16	Black	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Only show layers in layer stack Only show planes in layer stack Only show enabled mechanical Layer

[All On](#) [All Off](#) [Used On](#) [All On](#) [All Off](#) [Used On](#) [All On](#) [All Off](#) [Used On](#)

Mask Layers (A)	Color	Show	Other Layers (O)	Color	Show	System Colors (Y)	Color	Show
Top Paste	Grey	<input type="checkbox"/>	Drill Guide	Dark Red	<input type="checkbox"/>	Default Color for New Nets	Blue	<input checked="" type="checkbox"/>
Bottom Paste	Dark Red	<input type="checkbox"/>	Keep-Out Layer	Magenta	<input type="checkbox"/>	DRC Error Markers	Green	<input checked="" type="checkbox"/>
Top Solder	Purple	<input checked="" type="checkbox"/>	Drill Drawing	Red	<input type="checkbox"/>	Selections		<input checked="" type="checkbox"/>
Bottom Solder	Magenta	<input checked="" type="checkbox"/>	Multi-Layer	Grey	<input checked="" type="checkbox"/>	DRC Detail Markers		<input checked="" type="checkbox"/>

[All On](#) [All Off](#) [Used On](#) [All On](#) [All Off](#) [Used On](#)

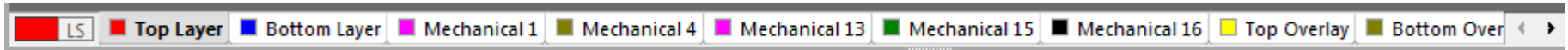
Silkscreen Layers (K)	Color	Show
Top Overlay (E)	Yellow	<input checked="" type="checkbox"/>
Bottom Overlay (R)	Olive	<input checked="" type="checkbox"/>

[All On](#) [All Off](#) [Used On](#)

[All Layers On](#) [All Layers Off](#) [Used Layers On](#) [Selected Layers On](#) [Selected Layers Off](#) [Clear All Layers](#)

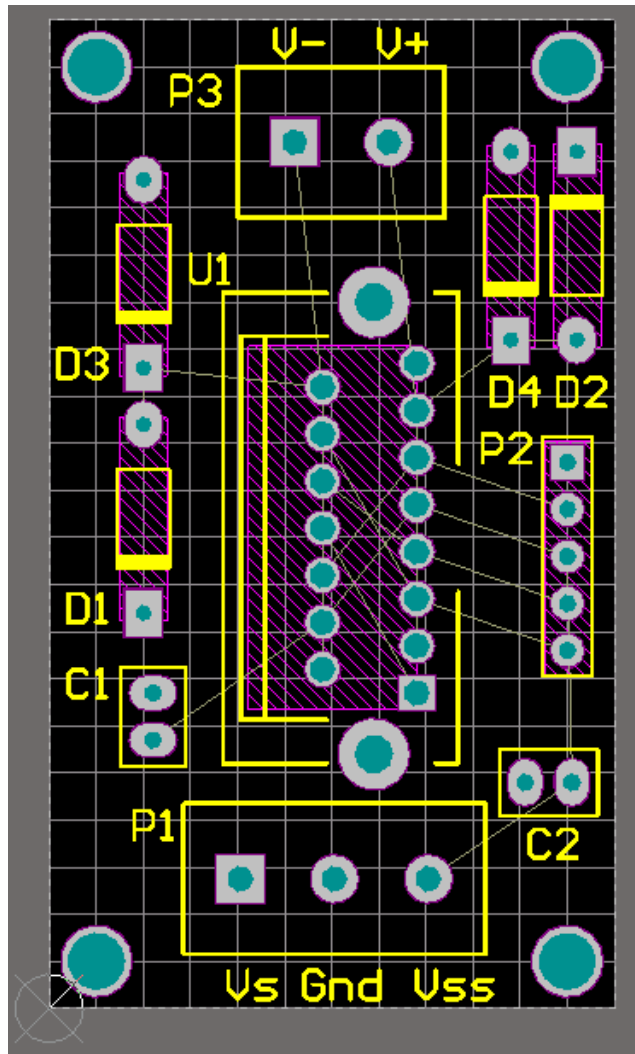
OK Cancel Apply

Configuring the Display Layers

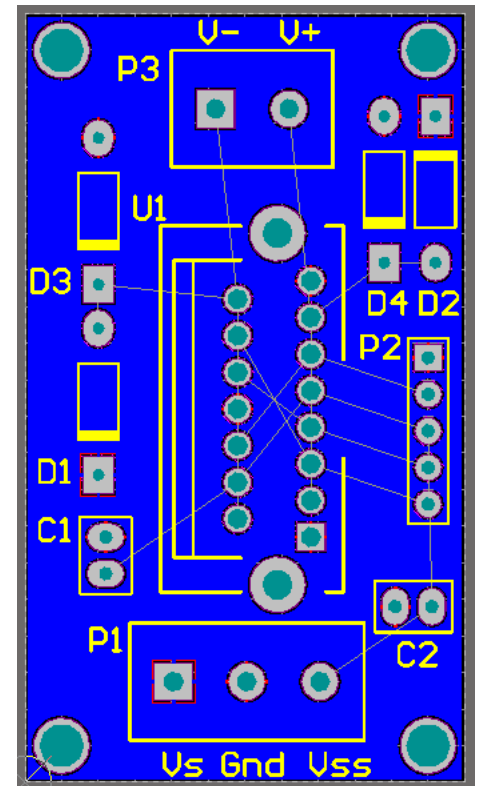
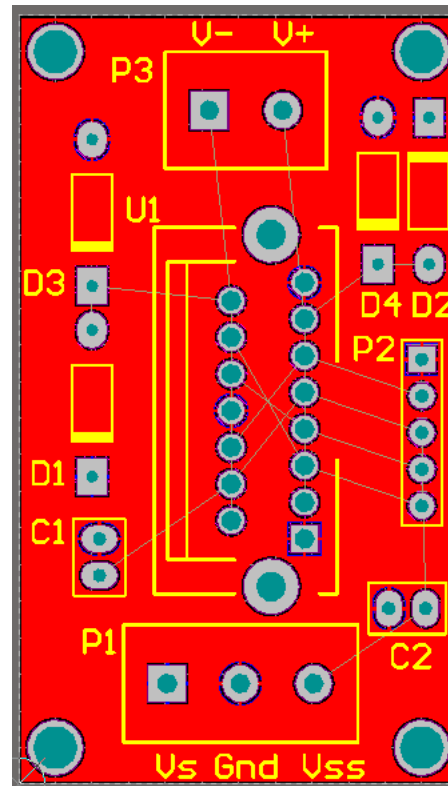


- **Electrical layers**
32 signal layers and 16 internal power plane layers.
- **Mechanical layers**
32 general purpose mechanical layers, used for design tasks such as dimensions, fabrication details, assembly instructions, or special purpose tasks such as glue dot layers. These layers can be selectively included in print and Gerber output generation. They can also be paired, meaning that objects placed on one of the paired layers in the library editor, will flip to the other layer in the pair when the component is flipped to the bottom side of the board.
- **Special layers**
these include the top and bottom silkscreen layers, the solder and paste mask layers, drill layers, the Keep-Out layer (used to define the electrical boundaries), the multilayer (used for multilayer pads and vias), the connection layer, DRC error layer, grid layers, hole layers, and other display-type layers.

Positioning components & routing



Place a plane on top for GND
Place a plane bottom for V_s



122mils mounting holes

Handy shortcuts for routing

- Press * on the numeric keypad while routing to cycle through the available signal layers. A via will automatically be added, in accordance with the applicable Routing Via Style design rule. Alternatively, use **Ctrl+Shift+Roll** shortcuts to move back and forth through the available signal layers.
- **Shift+R** to cycle through the enabled conflict resolution modes, including Push, Walkaround, Hug and Push, and Ignore. Enable the required modes in the **PCB Editor - Interactive Routing** page of the *Preferences* dialog.
- **Shift+S** to cycle single layer mode on and off, ideal when there are many objects on multiple layers.
- **Spacebar** to toggle the corner direction (for all but any angle mode).
- **Shift+Spacebar** to cycle through the various track corner modes. The styles are: any angle, 45°, 45° with arc, 90° and 90° with arc. There is an option to limit this to 45° and 90° in the **PCB Editor - Interactive Routing** page of the *Preferences* dialog.

Design Rules

- Design >> Rules

Rule	Constrain	Query
Electrical, Clearance	Min clearance = 7mil	All
Routing, Width*	Min width = 7mils Max width = 500mils Preferred = 10mils	All
Routing, Width_IO	Min width = 7mils Max width = 500mils Preferred = 100mils	Advanced (Query) (InNet('V+') OR InNet('V-'))
Width_Vss	Min width = 7mils Max width = 500mils Preferred = 20mils	Net Vss

Custom Routing design rules

The screenshot shows the 'PCB Rules and Constraints Editor [mil]' window. The left pane shows a tree view of design rules, with 'Width_1' selected under the 'Routing' category. A context menu is open over 'Width_1', showing options like 'New Rule...', 'Duplicate Rule', 'Delete Rule...', 'Report...', 'Export Rules...', and 'Import Rules...'. The main area shows the configuration for 'Width_1' with a name field containing 'Width_1', a comment field, and a unique ID 'EWBDPXHU'. Below this, there are sections for 'Where The Object Matches' (set to 'All') and 'Constraints'. A diagram of a yellow track with a fillet shows 'Preferred Width 10mil' and 'Max Width 10mil'. The 'Constraints' section has three radio buttons: 'Check Tracks/Arcs Min/Max Width Individually' (selected), 'Check Min/Max Width for Physically Connected Copper (tracks, arcs, fills, pads & vias)', and 'Characteristic Impedance Driven Width'. There is also a checkbox for 'Layers in layerstack only' which is checked. At the bottom, there is a table titled 'Attributes on Layer'.

Attributes on Layer			Layer Stack Reference		Absolute Layer	
Min Width	Preferred Size	Max Width	Name	Index	Name	Index
10mil	10mil	10mil	10mil Top Layer	32	TopLayer	1
10mil	10mil	10mil	10mil Bottom Layer	33	BottomLayer	32

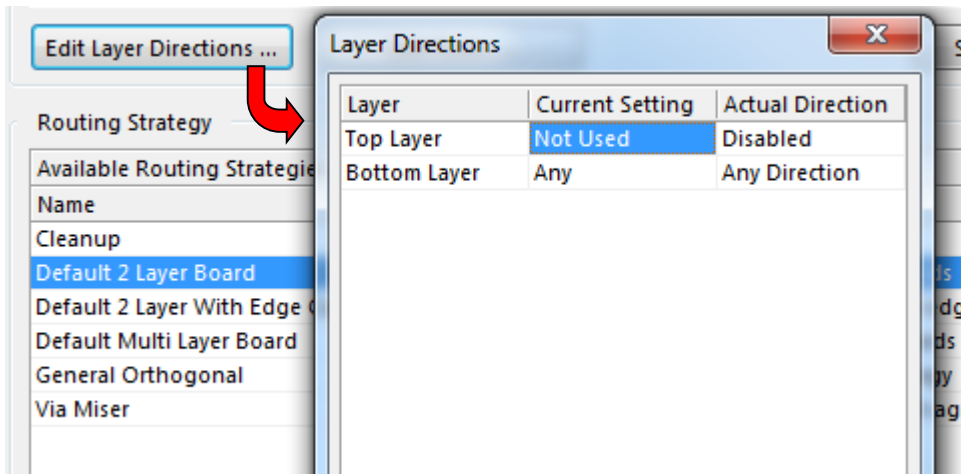
Rename to "Width_IO"

Use 'Custom Query' to set"
Belongs to net V+
OR
Belongs to V-

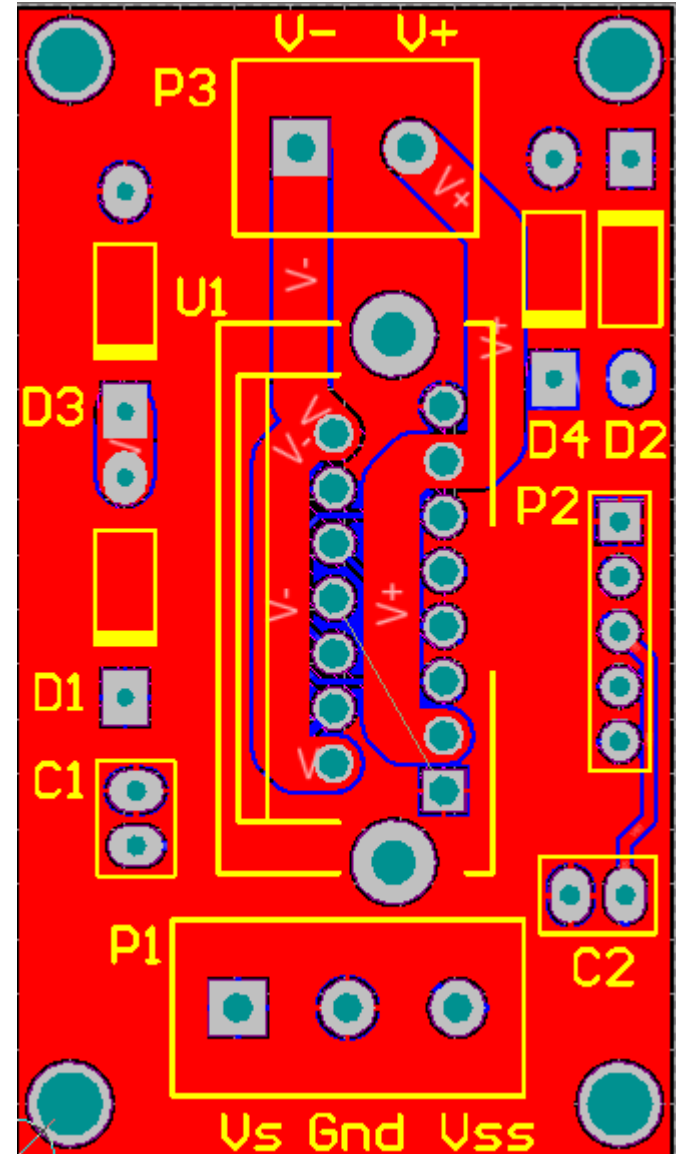
Set rule execution
priority

Auto route

- Tools » Un-Route » All
- Auto Route » All



- You can also set single layer routing

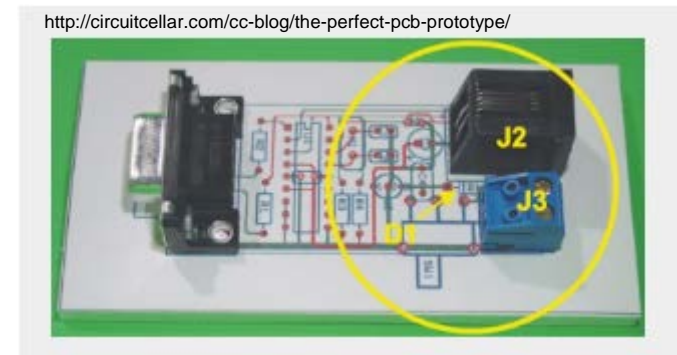




PCB Design Best Practices

Best Practices: Estimating board size

- Before starting layout it is good to have an idea of the target size of the PCB board and all other relevant dimensions.
- It is very helpful to have the components at hand to plan the floor-plan.
- An old good trick of the trade is to print the PCB layout at a 1:1 scale, place the printout on a foam and stick on the through hole components.

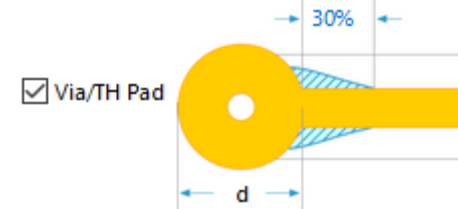


Best Practices: Floor planning

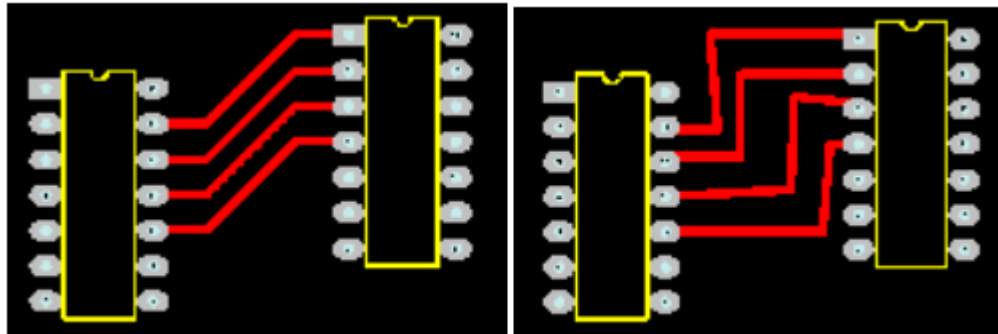
- Choose your units and set the grid
- Carefully plan the placement of components
 - Place analog and digital sections apart
 - Group components into 'functional blocks'
 - Place ICs in the same direction
 - Align ICs, resistors, labels, capacitors etc.
 - Place de-caps close by their ICs
 - Place Op-amp resistors near the Op-amp
 - Plan for mounting holes and heat sinks
- Aim for symmetry when possible
- Do use Design Rule check

Best Practices: Routing strategy

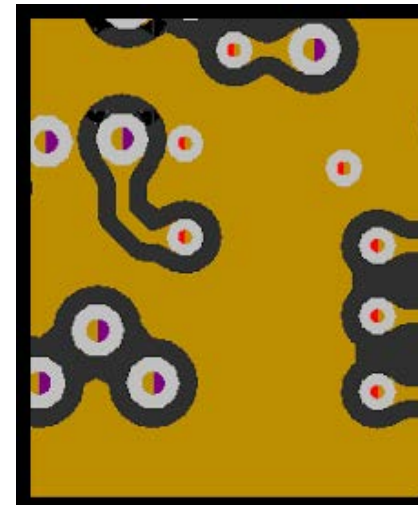
- On two sided boards keep traces perpendicular as much as possible
- Avoid 90 degree bends in tracks (?) (reduced chances of acid traps)
- Keep traces as short as possible
- Always connect a trace to the center of the pad
- Use teardrops (Tools >> tear drops), and use vias to avoid lockout
- Do not place vias under SMD pads
- Layout first all critical traces
 - e.g. CLK, diff pairs, controlled length
- Polygons as fills:
 - Connect to GND (EMC), or do not leave 'dead copper'
- Rout nicely



[Ref 3]

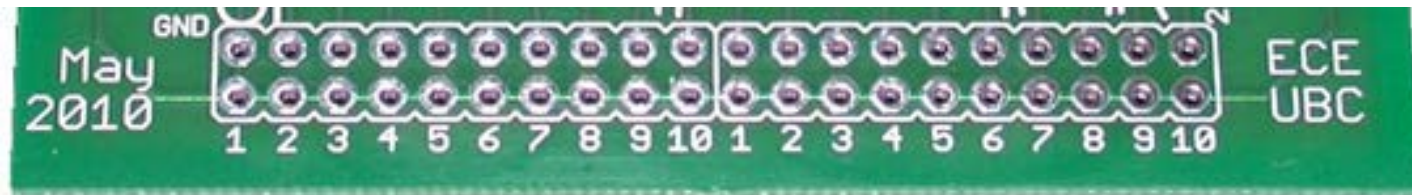


An example of GOOD routing (Left) and BAD routing (Right)



Best Practices: Labelling

- Always sign your design: add date, version, and name of board
- Label all relevant inputs and outputs
- Default sizes for comments and designators are 60mils x 10mils
- If you have silkscreen on both sides add a 'TOP' label to the top overlay.



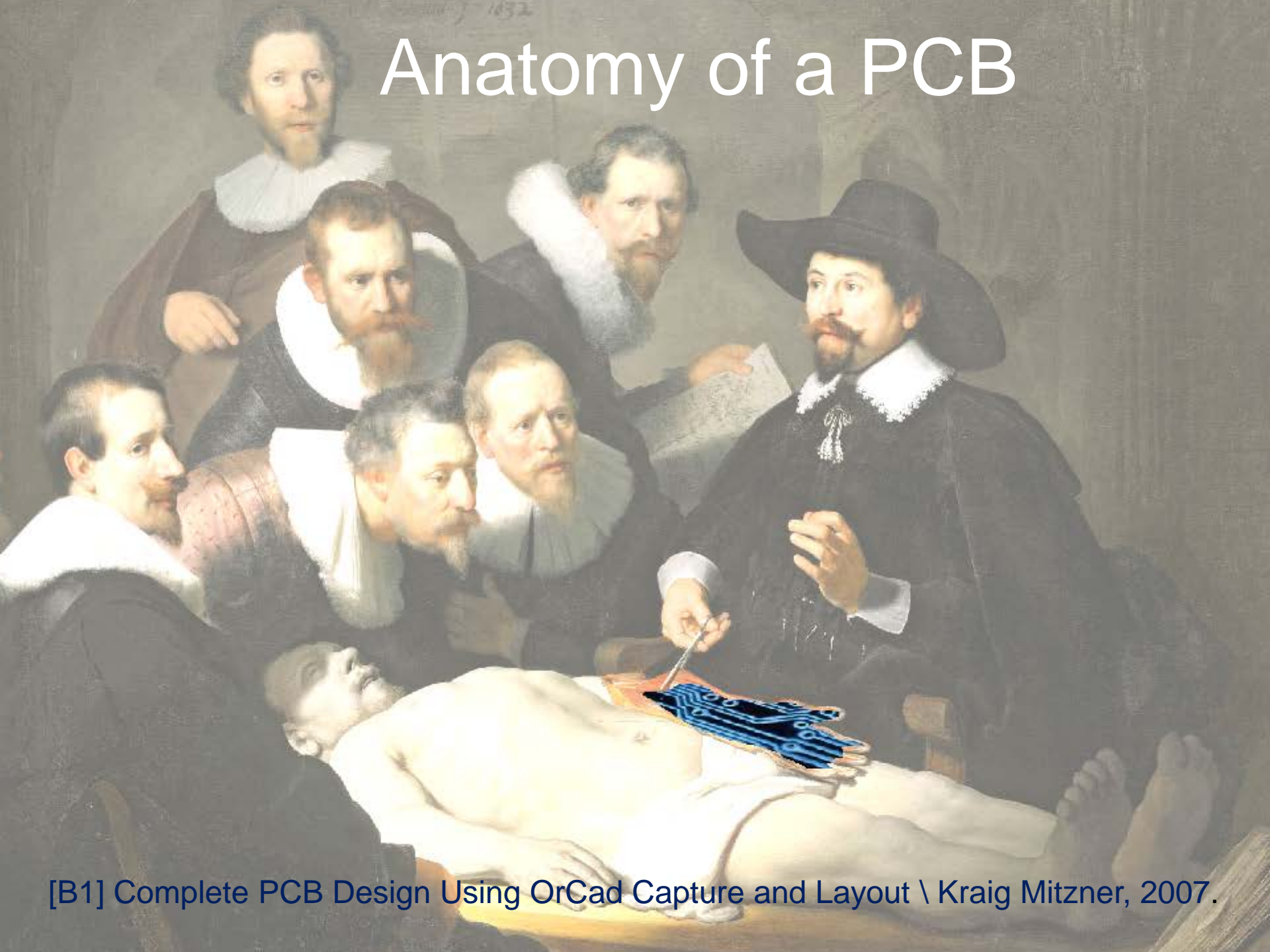
Best Practices: Finishing touches

- Add mounting holes
- Run: Reports >> Board Information
 - Board specification → to confirm board size
 - Non-plated hole size
 - Plated hole size
- Using the hole size editor:
 - Minimize the total number of holes sizes
 - Verify that all vias are the same size (if possible)
- Verify that there are no unwanted leftovers on any Mechanical layer

Online resources

1. [Ten best practices of PCB design – EDN Magazine, Edwin Robledo & Mark Toth](#)
2. [Circuit Board Layout Techniques – Texas Instruments, Chapter 17 of Op-amps for everyone](#)
3. [PCB Design Tutorial – David L. Jones](#)

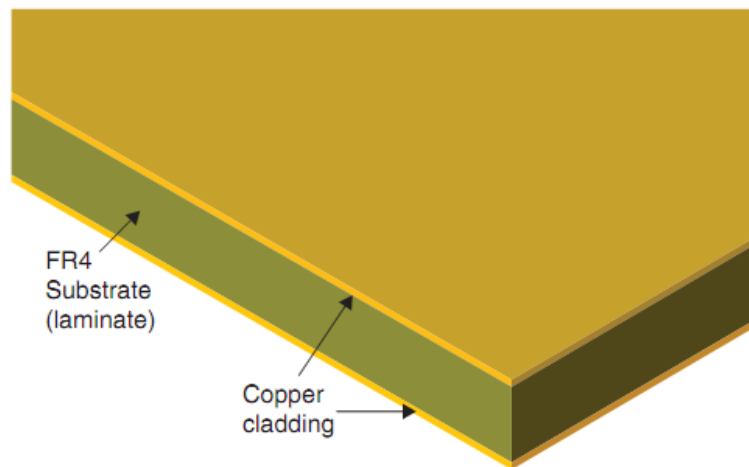
Anatomy of a PCB



[B1] Complete PCB Design Using OrCad Capture and Layout \ Kraig Mitzner, 2007.

PCB Anatomy: Laminate

- Laminate (substrate)
 - Rigid board of insulating material
 - Available in different thicknesses & materials
 - Covered with copper foil or cladding
 - Provides structural support and insulation to circuit components
 - Most commonly used material type is FR4, 62-63mils (1.6mm) thick



Cu thickness measured in weight oz/ft²

½ oz → 0.7mils

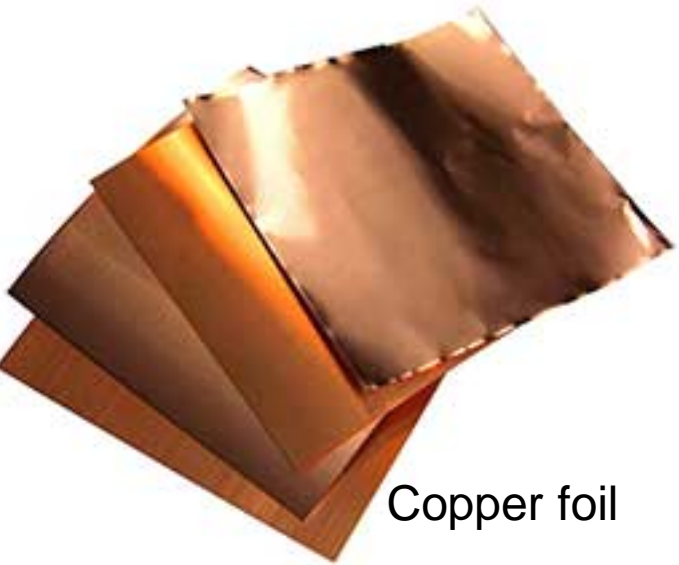
1 oz → 1.4mils

2 oz → 2.8mils

1mil = 25µm

Figure 1-2 A double-sided copper clad FR4 substrate.

PCB Anatomy: Laminate



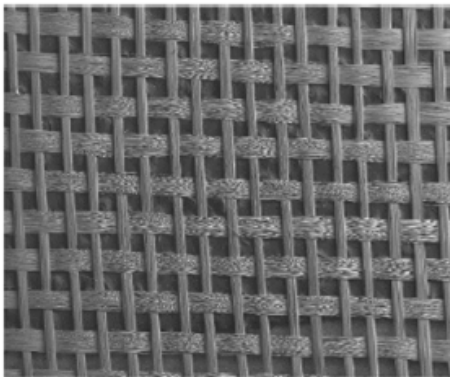
Copper foil



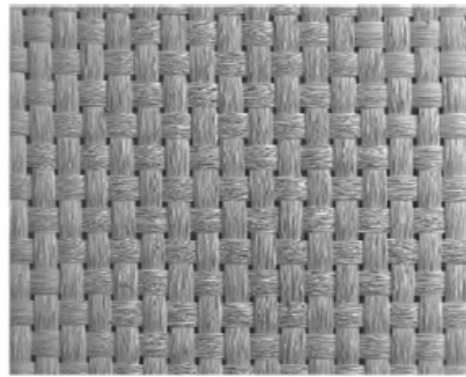
Prepeg



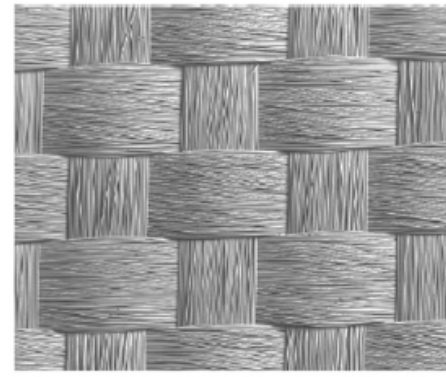
Copper clad



1080



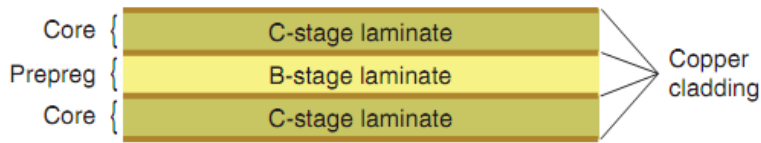
2116



7628

Common glass weaves

PCB Anatomy: Layer Stack-up



Ref [B1] *Figure 1-3 Cores and prepreg.*



Design >> Layer Stack Manager ...

Layer Stack Manager

Save Load Presets 3D Layer Pairs

Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)
Top Overlay	Overlay					
Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5	
Top Layer	Signal	Copper	1.4			
Dielectric1	Dielectric	None	62	FR-4	4.8	
Bottom Layer	Signal	Copper	1.4			
Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5	
Bottom Overlay	Overlay					

PCB Anatomy: Traces / Tracks

- Copper traces are patterned either by:
 - Photolithography: requires photomasks
 - Laser: used to draw patterns on photoresist
 - Mechanical milling: Cu is removed to isolate the traces.
- Trace width and thickness determines:
 - Ampacity (current carrying capacity)
 - Characteristic impedance for RF designs
- Manufacturing limitations:
 - Minimum trace width and gap (e.g. 7/7)

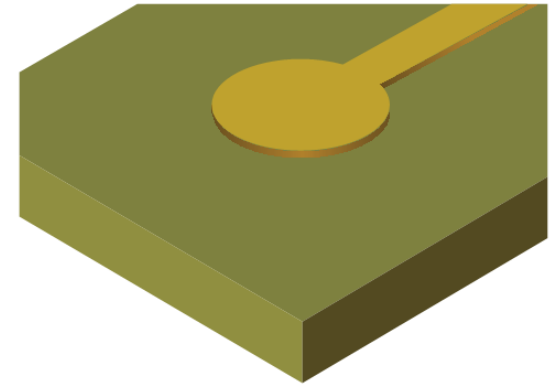


Figure 1-11 Copper pad and trace after etching and resist stripping.

Negative view:
Copper planes, Drill
holes, Solder Masks

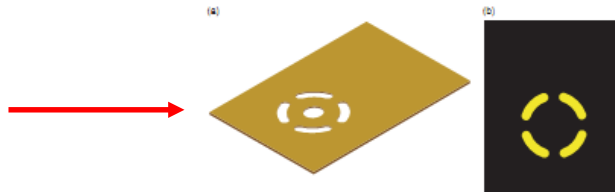


Figure 1-18 Copper in a plane layer (negative view without drill info). (a) Copper plane with thermal relief. (b) Negative view in Layout.

Teardrops:

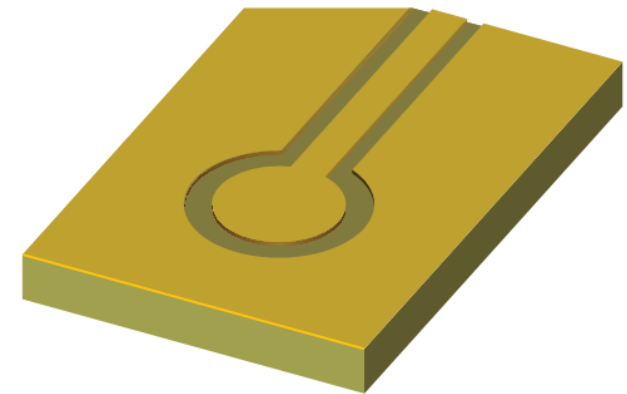
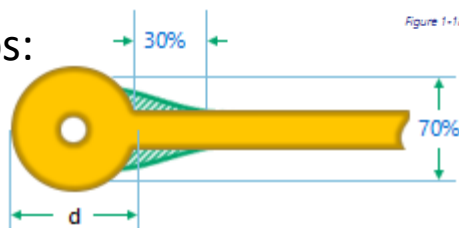
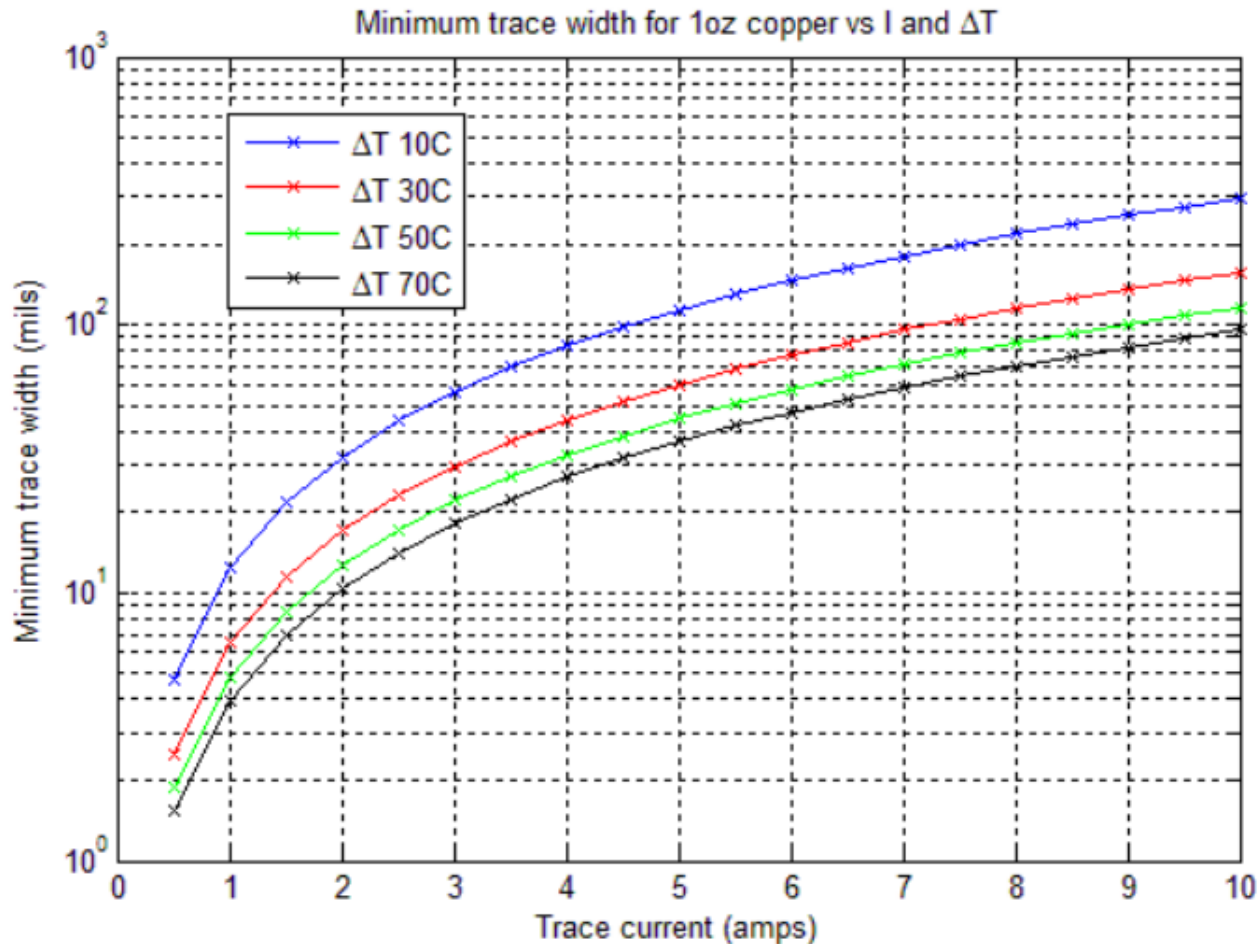


Figure 1-12 A mechanically milled trace.

PCB Anatomy: Trace width

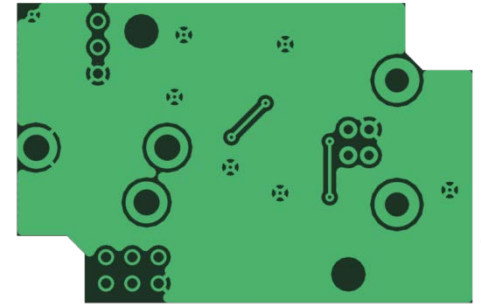


Use the following online trace width calculator:

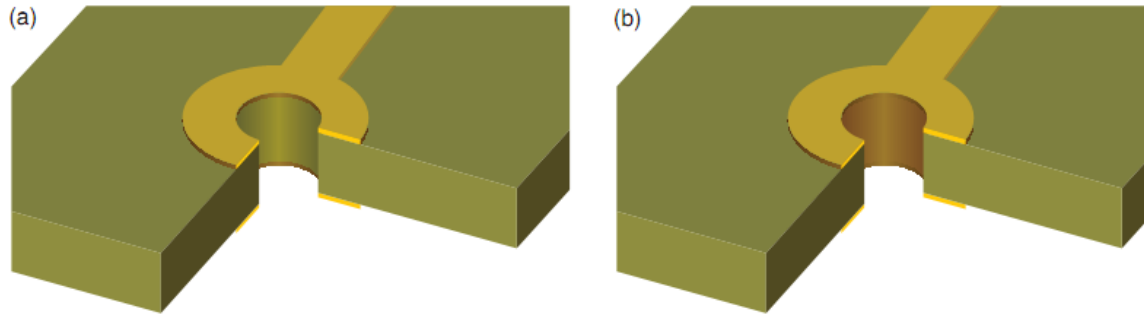
<http://circuitcalculator.com/wordpress/2006/01/31/pcb-trace-width-calculator>

PCB Anatomy: Vias

- Connection between layers is accomplished with via holes
- After the holes are drilled, their inner walls are plated
- Top and bottom traces are patterned after plating



Source: wikipedia.org: Thermal pad



Thermal relief is needed when connecting a via to a copper plane

Figure 1-13 Holes are drilled into the board and then copper plated. (a) A nonplated through-hole. (b) A plated through-hole.

PWR and GND planes are commonly inner layers

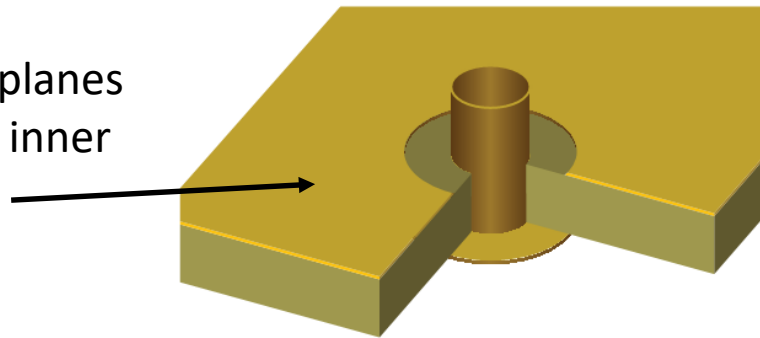


Figure 1-15 A clearance area provides isolation between a plated hole and a plane.

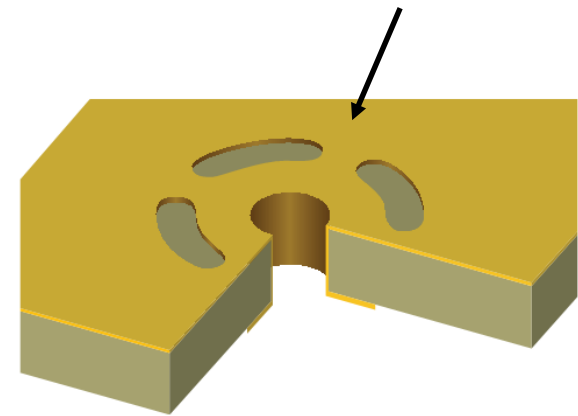


Figure 1-14 A connection to a plane layer through a thermal relief.

PCB Anatomy: Vias

- Types of via holes:
 - Plated and un-plated through-hole, blind, buried

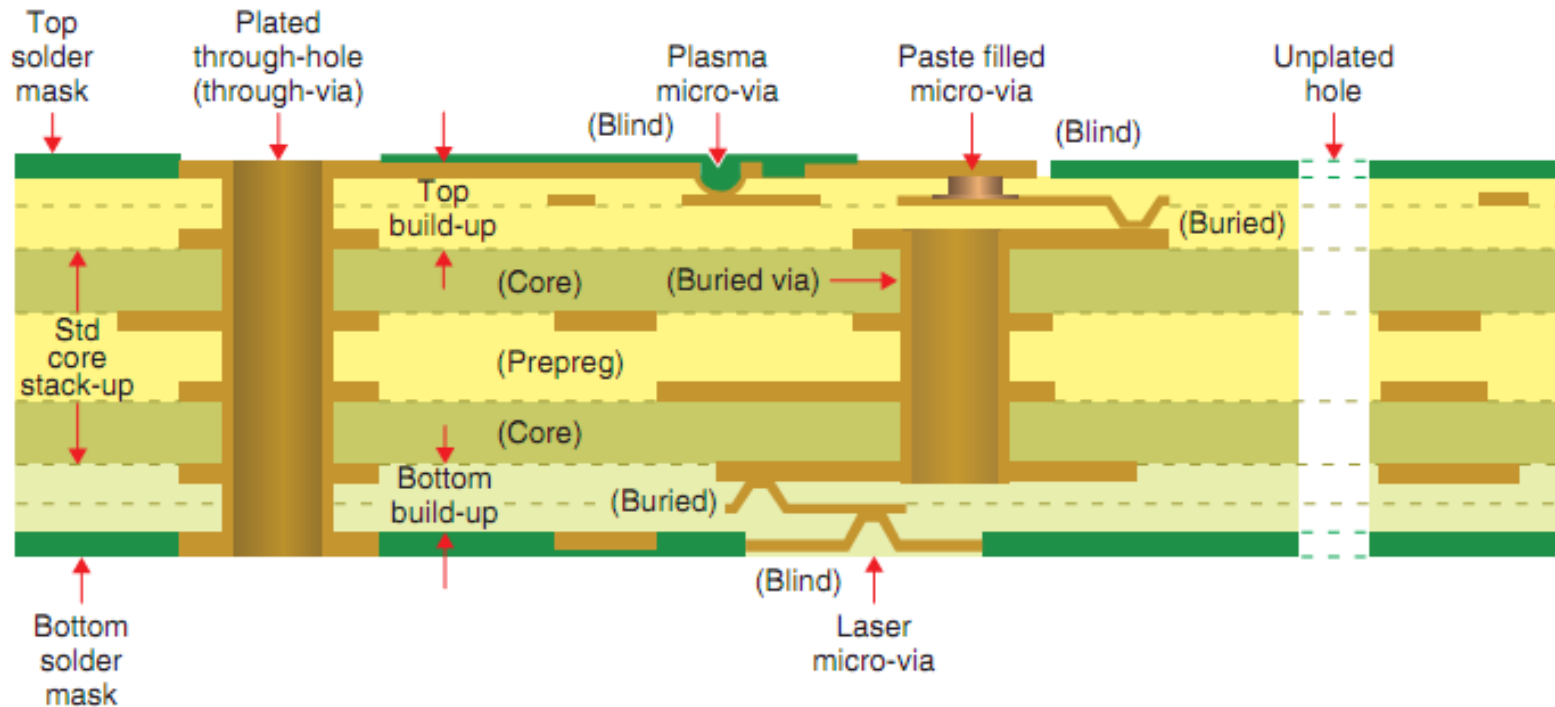
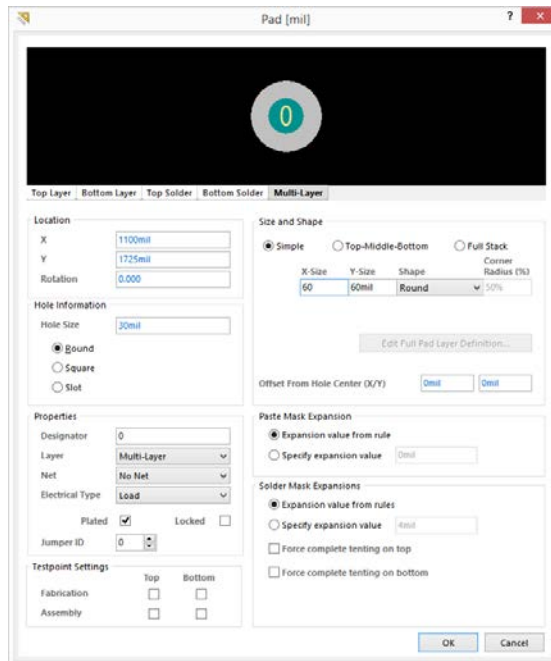


Figure 1-5 A built-up, multitechnology, PCB stack-up.

PCB Anatomy: Holes

Holes can be:

- Vias, multi-layer pads, mounting holes, or cuts
- Plated or non plated



Altium pad properties dialog

With pads

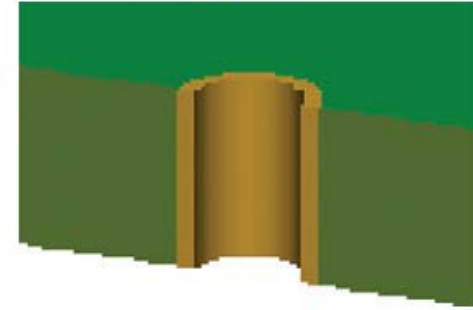
Without pads

Plated

2a

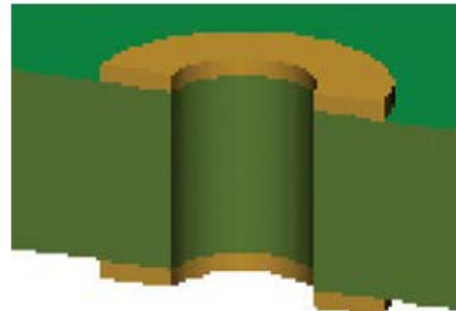


2c



Nonplated

2b



2d

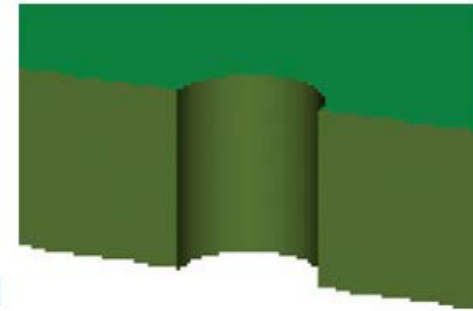


Table 8-2 Basic hole types

You must specify whether a hole is plated or non plated during the design process

Plating reduces hole size by 0.003"

PCB Anatomy: Pads

- Pads: contact areas for soldering components, test points, and solder traps
- Pads can have any shape
- Single layer pads: Top/bottom layer, common for SMT, end launch connectors
- Multi-layer pads: for through hole components
- Footprints are a collection of pads

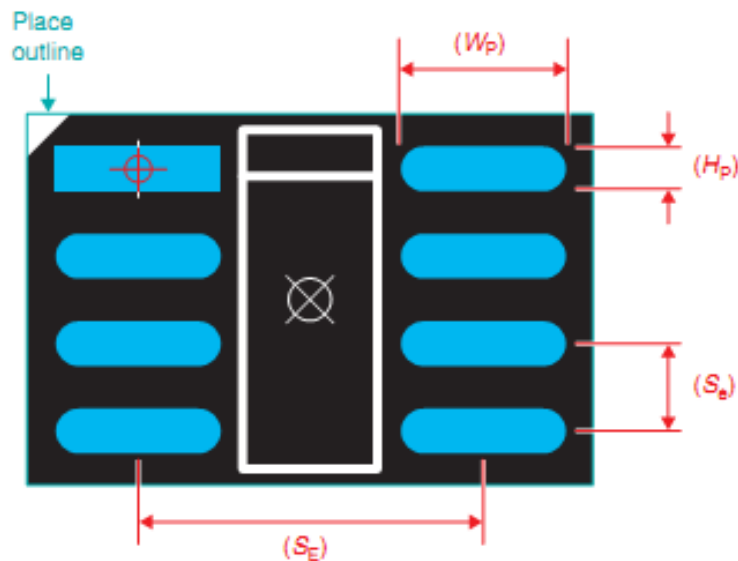


Figure 5-7 Footprint dimensions (typical convention).

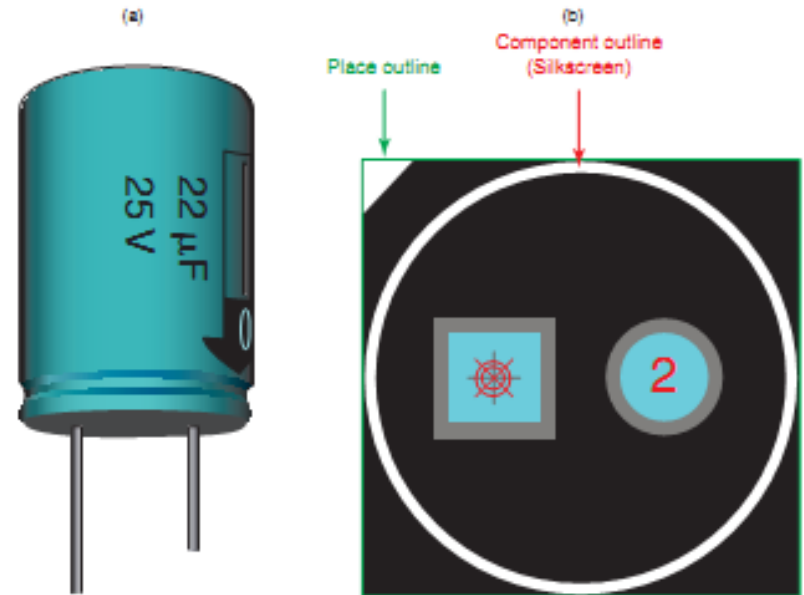


Figure 5-12 Radial-leaded through-hole device. (a) Axial-leaded capacitor. (b) Layout axial footprint

PCB Anatomy: Solder mask

- Solder mask or solder resist:
 - Thin polymer layer deposited on top and bottom layers
 - Protects outer layers from oxidation and prevents solder bridges
 - Allows for wave or reflow soldering of components
 - Holes are opened with photolithography wherever components will be soldered
 - Default color is green, but any other color is possible

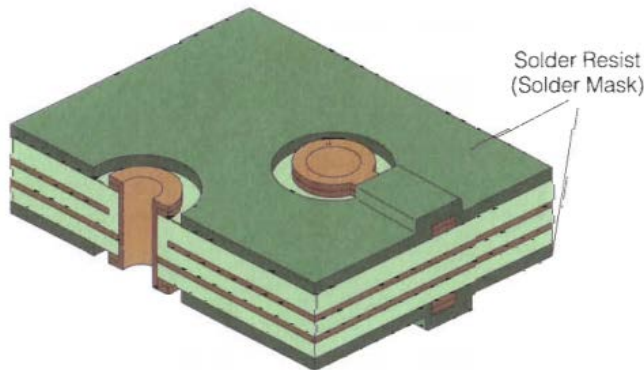


Illustration ML-14. *Apply solder resist.* The specified resist (either dry film, liquid photoimageable, or screen printed) is applied to the surfaces of the PCB or panel.

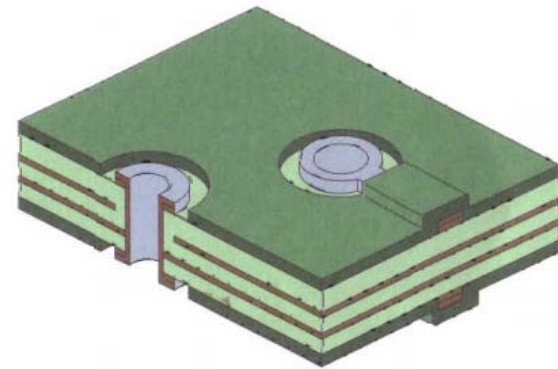
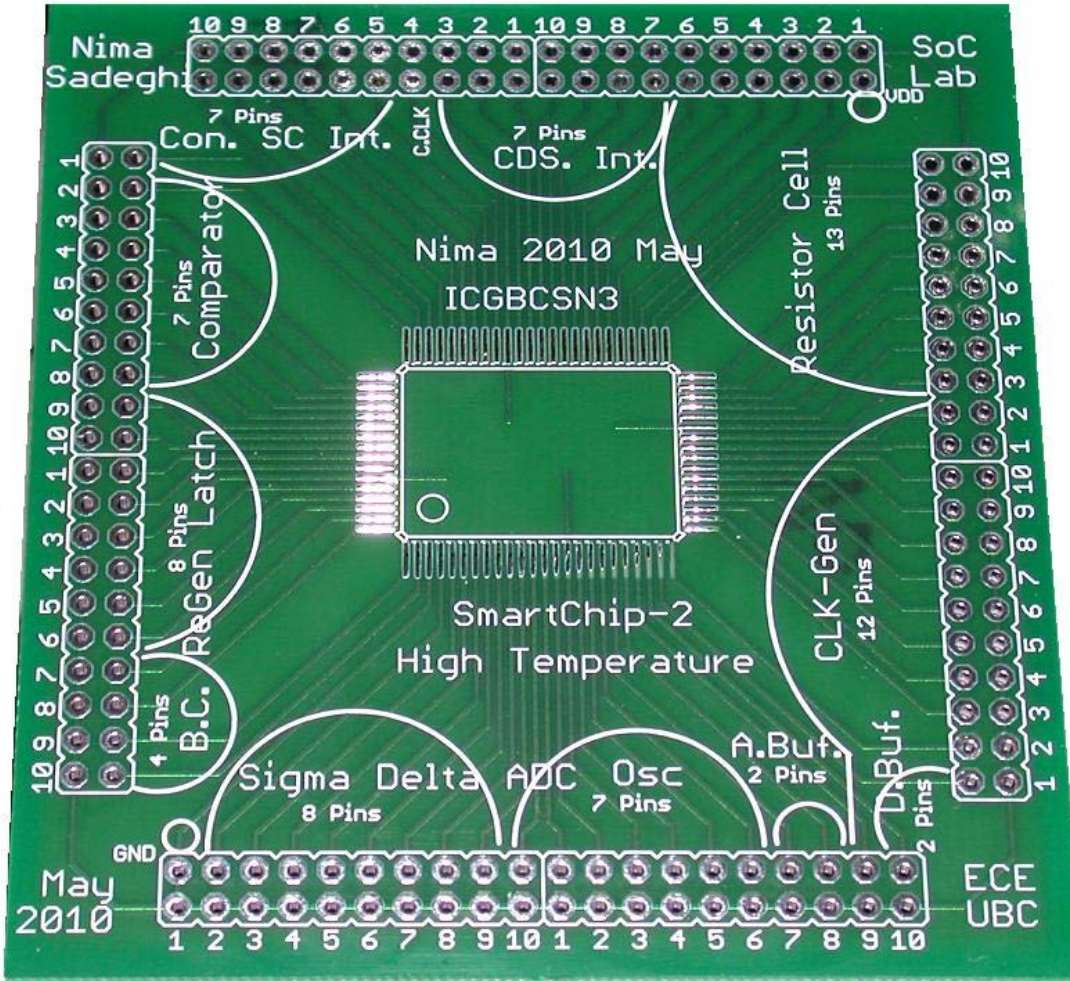


Illustration ML-15. *Solder coat.* Solder (tin/lead) is applied to the exposed copper areas, and the excess solder is removed.

Source: Printed Circuit Board Basics: An Introduction to the PCB Industry, by: Michael Flatt

PCB Anatomy: Legend / Silkscreen / Overlay



- Legend or silkscreen:
 - Applied on top of the solder resist
 - Can be applied to one or both outer layers
 - Default color is white but any other color is possible

Tip: add (Top) and (Bottom)

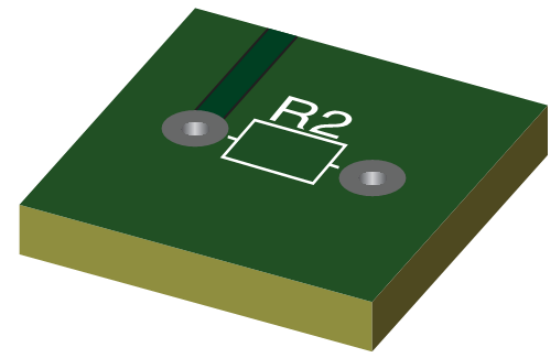
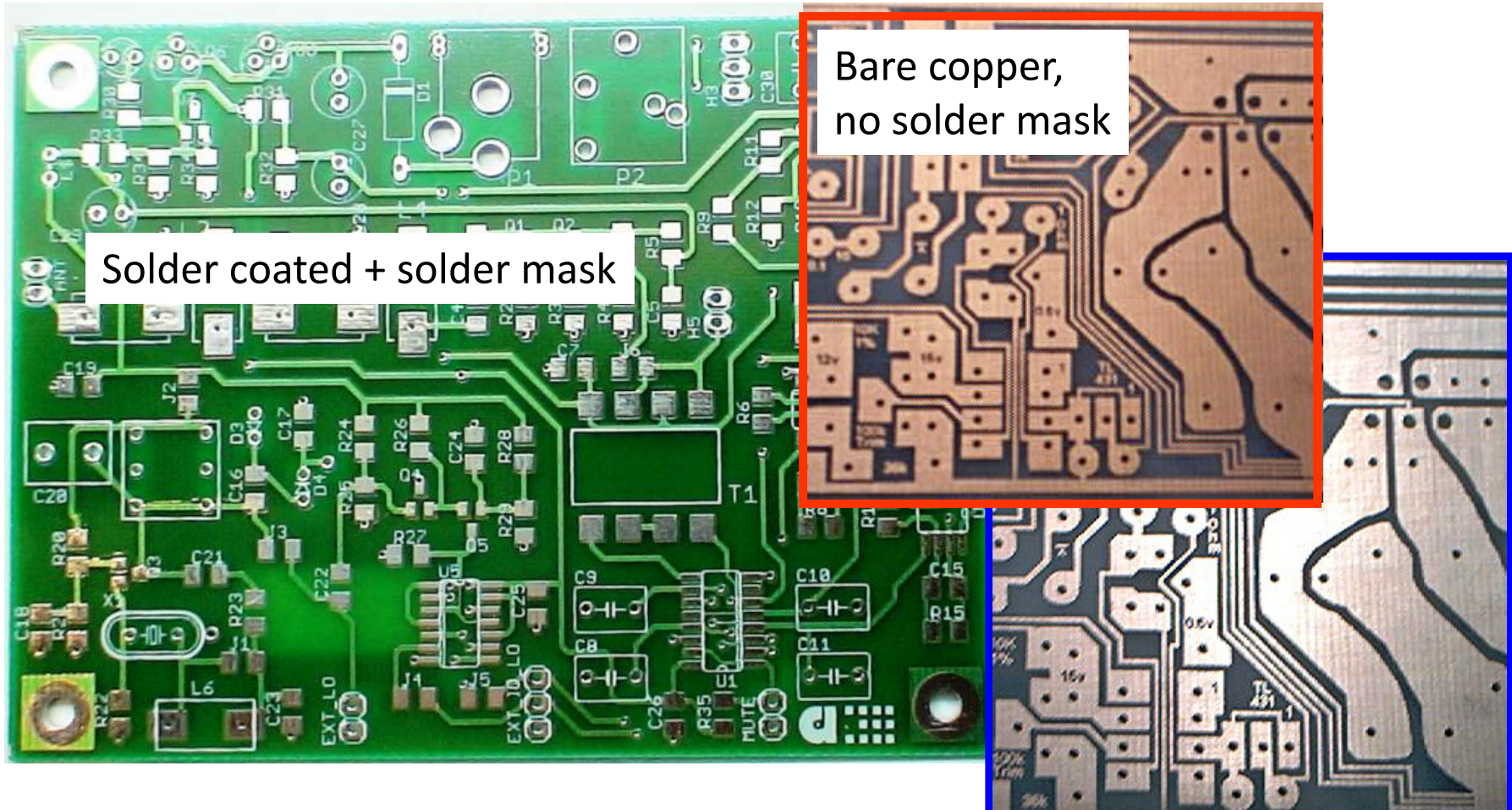


Figure 1-16 Final layers are the soldermask (green) and silk screen (white).

PCB Anatomy: Surface finishing / thinning



There are different types of finishes, eg:

HASL (tin), ENIG (Nickel and Gold), Silver immersion

Solder coated + no solder mask

PCB Anatomy: Mechanical Layers

- Multi-purpose layers
- E.g. Altium supports 32 Mechanical layers: M1 ... M32
- Typically
 - M1 Board outline
 - M2 PCB manufacturing info
 - M11-M12 Top and bottom layer dimensions
 - M13 Top layer 3D models and mechanical outlines
 - M14 Bottom layer 3D models and mechanical outlines
 - M15 Top layer assembly information
 - M16 Bottom layer assembly information

PCB Basic Terminology

- **Laminate / Substrate**
 - Material (FR4, Rogers)
 - Thickness (62-63mil, 16mm)
 - Prepeg, Core, Foil, Clad
 - Stack-up
- **Traces / tracks**
 - Width & gap
 - Ampacity
 - Characteristic impedance
- **Vias & Hole**
 - Types of vias
 - Plated vs non-plated holes
 - Thermal relief
 - Annular ring
- **Pads**
 - Multi-layer, single layer
 - Tear drop
- **Components /Parts**
 - Footprints
 - Symbols
 - Libraries
- **Layers**
 - Mechanical, board outline
 - Top metal, Bottom metal
 - Inner layers / Planes
 - Top / Bottom Solder Mask
 - Legend / Silkscreen / Top overlay
 - Top / Bottom pads
 - Multi-layer
- **Surface Finish**
 - HASL, ENIG
- **Fabrication CAM files**
 - Gerber, 274X
 - Excellon NC drill files