FEC and Convolutional Codes

Channel Codes

Channel coding refers to adding redundancy in the form of parity bits to messages. The parity bits allow for detection and/or correction of errors introduced by the channel.

Block Codes

A block code consists n bits containing k data bits and $n-k$ parity bits. This is called an (n,k) code.

Exercise 1: How many different valid code words does an (n,k) code have? How many different code words (including those with errors) could be received?

The *Hamming Distance*, d is the number of bits that differ between two code words. The performance of a code is generally determined by the minimum (Hamming) distance between code words. A block code can detect up to $d-1$ errors and correct up to $\lfloor (d-1)/2 \rfloor$ errors.

Exercise 2: What is the Hamming distance between the codewords 11100 and 11011?

The *rate* of a code is the ratio of information bits to total bits, or k/n. This is a measure of the efficiency of the code. Typically there is a tradeoff between the error-correcting ability (minimum distance) and the rate of a code.

FEC Coding and Minimum Distance Decoding

It is possible to correct errors with certain block codes. These types of codes are called Forward Error Correcting (FEC) codes.

Conceptually, a receiver can correct errors by choosing the valid codeword that has the smallest Hamming distance from the received codeword. This is because codewords with fewer errors are more likely to happen than those with more errors.

Exercise 3: A block code has two valid codewords, 101 and 010. What is the minimum distance d? How many errors can be detected? Corrected? The receiver receives the codeword 110. What is the Hamming distance between the received codeword and each of the valid codewords? What codeword should the receiver decide was sent?

However, with large codewords it is not possible to do a simple exhaustive search through all possible codewords to find the one with the minimum distance. There is a large field of study devoted to the design of codes which can be efficiently decoded.

One very common type of error-detecting block codes are cyclic redundancy check (CRC).

Error Correcting Codes

Forward Error Correcting (FEC) are codes that include enough parity bits with each message that the receiver can correct received code words that contain less than a given number of errors.

When the FEC code is well-matched to the error rate and to the types of errors likely to be encountered, the use of FEC results in higher throughput and better power efficiency.

Higher throughput results because blocks that contain correctable errors do not need to be retransmitted.

Exercise 4: If a rate-$1/2$ FEC code is used, what fraction of frames must contain correctable errors for the use of FEC to result in a net improvement in throughput?

Better power efficiency results if the same post-correction error rate can be achieved by transmitting at a lower (E_b/N_0). This reduction in the required E_b/N_0 to achieve a certain error rate is called the "coding gain".

Exercise 5: A system without coding needs to transmit at 1W to transmit 1 Mb/s at an error rate of 10^{-3}. When a rate-$1/2$ code is used the power to transmit the necessary 2Mb/s of data and parity bits decreases to 500mW. What is the channel bit rate in each case? What is the information rate in each case? What is E_b? What is the coding gain?

Although it is possible to use block codes to implement FEC, the trend until recently has been to use convolutional codes for communication systems. This was mainly because of the existence of a relatively simple and efficient decoding algorithm for convolutional codes called the Viterbi algorithm.

Convolutional Codes

A rate k/n convolutional code is implemented by reading a certain number of bits into a shift register

and outputting a number of modulo-2 sums of these bits as shown below[1]

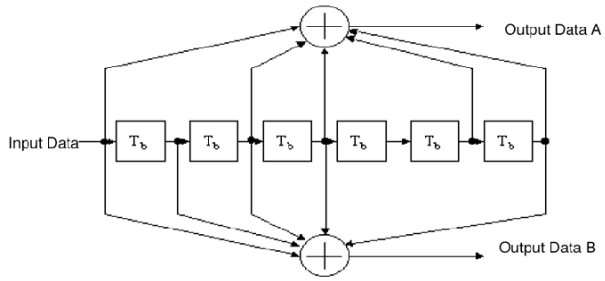

Figure 18-8—Convolutional encoder (k = 7)

If there are n output bits for each k input bits the rate of the code is k/n. The "constraint length," (K) of the code is the number of bits that can affect each output bit and is equal to the length of the shift register plus one (because the input bit is also used in computing the output).

Exercise 6: Assuming one bit at a time is input into the encoder in the diagram above, what are k, n, K and the code rate?

Viterbi Algorithm

Most FEC decoders for convolutional codes use an algorithm called the Viterbi algorithm (VA). This algorithm is a "maximum likelihood" decoder because it chooses the bit sequence with the minimum distance from the received sequence.

The VA uses the "trellis" structure of the code to avoid exponential increase in decoding complexity with message length. Instead, the complexity is proportional to 2^K where K is the constraint length.

A convolutional encoder with $K-1$ shift register bits can be in one of 2^{K-1} states. Each input bit causes the encoder state to change to one of two other states depending on the value of the input bit. The trellis structure refers to this state transition diagram for the encoder. The VA keeps track of the probabilities that the transmit encoder is in each of the possible states and the most likely sequence of bits leading up to that state.

Implementations are readily available as software, FPGA components, synthesizable HDL and ICs.

Although many different convolutional codes are possible, there are certain standard codes that are used by many different systems. Hardware implementations are typically only available for these codes. The most common convolutional code is the rate-1/2 code with a constraint length of 7 shown above.

Higher-rate codes can be derived from the basic rate-1/2 code by not transmitting some of the bits. This is called "puncturing." The same decoder hardware can be used by feeding the decoder a value representing "unknown" (an "erasure") in place of the missing parity bits.

Exercise 7: Consider the encoder above. If the only the bits corresponding to the outputs A, A and B, and B are transmitted corresponding to every three input bits, what is the code rate of this punctured code?

Modern FEC Codes

Two other FEC codes have become popular in recent years because their error-correcting performance approaches the Shannon Limit.

Turbo Codes use two different codes to encode the data. The decoder uses the information from one code to help with decoding of the other code. Then that information is used to help decode the first code. The procedure is repeated iteratively until there are no errors (determined by a CRC) or a limit is reached. A common problem with Turbo Codes is an error floor.

Low Density Parity Check (LDPC) codes are block codes with sparse (few 1's) parity check matrices. This means that each parity bit is a function of only a few message bits.

Most FEC decoders use "soft-decision" decoding algorithms that operate on the probabilities that particular bits are zeros or ones rather than operating on binary "hard decisions".

Reed Solomon Codes

The Reed-Solomon code is a block FEC code that is widely used. RS codes operate on non-binary Galois fields, typically GF(256). It is able to correct a certain number of 8-bit word errors, regardless of the number of bit errors in each word. For this reason Reed-Solomon codes are efficient for channels that have bursty errors that cause multiple errors to fall within the same 8-bit word.

[1] Taken from the 802.11 standard.