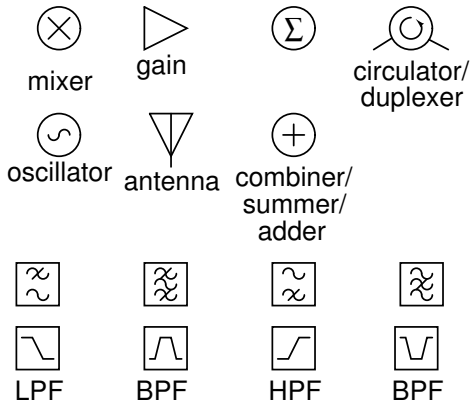
RF Design - Receiver Architectures

Receiver Architectures

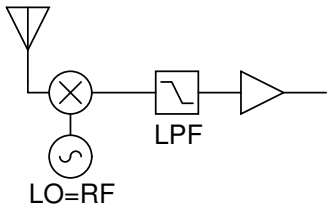
Block Diagrams

Some symbols that are commonly used in RF block diagrams are shown below:



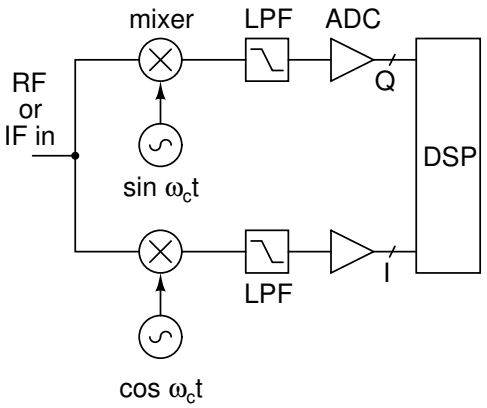
Zero-IF Receiver

This is known as a direct-conversion, homodyne or zero-IF receiver. This receiver uses a local oscillator to mix the RF signal directly to baseband:



The only tunable component in this architecture is the local oscillator. This provides simplicity and flexibility. Since there are no tuned bandpass circuits, the receiver can cover a wide range of frequencies simply by changing the LO frequency. The bandwidth can be changed by changing the baseband filter bandwidth.

If the receiver requires phase as well as amplitude information a quadrature down-converter that converts the IF (or RF) signal to separate in-phase and quadrature baseband components is used:



This is the architecture used by the SDR radios we've used in the labs.

Exercise 1: A zero-IF receiver is tuned to a center frequency of 100 MHz. The input contains a signal at 101 MHz. What components are present at the input, after the mixers and after the low-pass filters? Give the frequencies, amplitudes and phases of the components.

However, this architecture has some practical disadvantages related to the non-ideal performance of the analog mixers and oscillators.

If the LO outputs have a DC component, this will appear as a baseband component at DC which is equivalent to the RF carrier frequency.

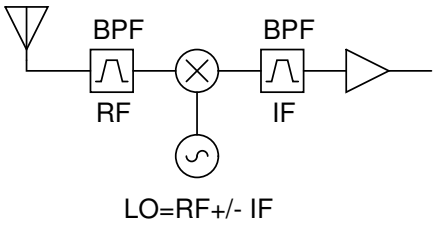
Cancellation of images (at negative frequencies) requires that the I and Q branches have equal gains. Unequal gains will result in images across the carrier frequency.

Exercise 2: What is the baseband spectrum if we add the I and Q branches above? What is the spectrum if the two branches have unequal gains? What if a DC offset is added to a mixer output?

It is impractical to manufacture amplifiers and mixer that match across a range of voltage, temperature and process variations. Thus quadrature down-converters have "trimming" DACs that adjust the gains and DC offsets to compensate for these variations. Algorithms running on embedded microcontrollers (or as part of the SDR software) adjust the DACs to zero out any DC offset and ensure I-Q gain balance.

Superheterodyne Receiver

The superheterodyne receiver uses a local oscillator to mix the RF signal to an intermediate frequency (IF) where a channel-select IF filter rejects adjacent-channel signals. This is followed by gain before the IF signal is demodulated. A bandpass or band-reject filter can be used before the mixer to improve image rejection.



Exercise 3: Assume the RF frequency is 100 MHz, the IF frequency is 1 MHz and the signal bandwidth is 100 kHz. Draw the frequency components at the RF input (desired frequency and an image), LO output, and at IF before and after the IF filter.

Although it requires an additional mixer stage, this architecture allows the majority of the amplification to be done after the IF filter. This means that only the desired signal is being amplified and the IF gain can be set to the minimum value required. This can improve the cascade noise figure and IP3 compared to a direct-conversion receiver.

Low IF Receiver

Another option is to convert the RF or IF signal to a low-frequency IF signal, digitize this signal and do the quadrature down-conversion digitally.

This is a compromise between the superheterodyne and the zero-IF and combines the two block diagrams above. The IF signal is at a frequency that is low enough for the DAC to sample but high enough that images can be rejected by a band-pass filter.

The quadrature down-conversion is implemented digitally with arbitrary accuracy and avoids many issues with the analog quadrature down-converters such as gain imbalance, phase quadrature errors, DC offsets in the mixers and leakage.

The disadvantages of this approach are that a more complex down-converter is required to obtain adequate image rejection for low IF frequencies (see below) and that the A/D converter sample rate must be at least twice the rate required by the analog quadrature down-converter.

Direct RF Sampling Receiver

If the ADC rate is sufficiently high relative to the RF frequency, it's possible to sample the RF signal directly. Since ADC clock rates of several GHz are currently possible, this is now possible for cellular frequencies.

Exercise 4: Draw the block diagram of an RF-sampling receiver.

For this type of receiver all the signal processing is done digitally: generation LO signals, mixing, filtering, decimation, etc.

The power consumption of such high-rate conversion and signal processing is relatively high so this approach is used when the flexibility and ability to cover multiple bands simultaneously is more important than power efficiency.