Solutions to Assignment 3

April 16: Reformatted and added note on use of t_{SETUP} in `set_output_delay` *in Question 1(g).*

Question 1

(a) The following pins are inputs: CS (pin 7), SDI (pin 13), and SCLK (pin 14).

(b) The following pins are outputs: INT1 (pin 8), INT2 (pin 9) and SDO (pin 12).

(c) See table 1 for the table of timing specifications.

(d) A `create_clock` SDC statement that defines a 50 MHz clock named `clock50` present at an input port named `clock`:

```
create_clock -name clock50 -period 20 \
   [get_ports clock]
```

(e) A `create_generated_clock` SDC statement that defines a 2 MHz clock named `clock2` assigned to an internal target pin in your design called `spiclk` and derived from a source at the input port `clock`:

```
create_generated_clock -divide_by 25 -name clock2 \
   -source [get_ports clock] [get_pins spiclk]
```

(f) A `set_input_delay` SDC statement that specifies the propagation delay equal to the maximum value of t_{SDO} for an input port named `miso` clocked by a clock signal `clock2` is given below. This value will be added to the data arrival time to ensure that the setup time requirement of internal registers clocked by `clock2` will be met.

```
set_input_delay -clock clock2 \
   -max 40 [get_ports miso]
```

(g) A `set_output_delay` SDC statement that defines a maximum output delay equal to t_{SETUP} for an output output port called `mosi` clocked by a clock called `sclk` is given below.

Since this value is added to the latest data arrival time, this value should be set to the negative of the setup time (-5ns) to ensure the latest data arrival time is 5ns earlier than it would be otherwise. Since question specifies a `-max` value equal to t_{SETUP}, either +5 or -5 values were marked as correct.

```
set_output_delay -clock sclk \
   -max 5 [get_ports mosi]
```

symbol	from	to	req/resp	max/min	value (ns)
t_{SCLK}	SCLK	SCLK	req	min	200
t_{DELAY}	$\overline{CS}$	SCLK	req	min	5
t_{QUIET}	SCLK	$\overline{CS}$	req	min	5
t_{DIS}	$\overline{CS}$	SDO	resp	max	10
$t_{CS,DIS}$	$\overline{CS}$	$\overline{CS}$	req	min	150
t_S	SCLK	SCLK	req	min	$0.3\times t_{SCLK}$
t_M	SCLK	SCLK	req	min	$0.3\times t_{SCLK}$
t_{SETUP}	SDI	SCLK	req	min	5
t_{HOLD}	SCLK	SDI	req	min	5
t_{SDO}	SCLK	SDO	resp	max	40

Table 1: Table for Question 1(c).