Solutions to Assignment 2

Question 1

1. For the example BCIT ID (A00123456) the test value is $0+0+1+2+3+4+5+6 = 21_{10} =$ 2'b0001_0101.

2. The sequence of logic levels (0 and 1) to be transmitted are: idle=1, start bit=0, data=1010 1000, and stop bit=1.

3. The source code for the System Verilog testbench is shown below.

4. The screen capture of your console output showing the "passed" or "failed" result output is:

```
VSIM 4> run -all
# passed: data= 21
# ** Note: $stop    : C:/
#    Time: 96330 ns  Iter
```

5. A screen capture of the simulation waveforms is shown in Figure 1.

```
// asg2tb.sv - UART receiver testbench
// Ed Casas  2018-3-14
// ELEX 7660 201810 Assignment 2

module testbench ;

   logic clk_50m, rxclk_en, txclk_en,
         rx, rdy, rdy_clr ;
   logic [7:0] data ;

   baud_rate_gen b0 (.*) ;
   receiver r0 (.clken(rxclk_en),.*) ;

   int testvalue = 21 ;

   initial begin
      $dumpfile("asg2.vcd") ;
      $dumpvars ;
      // reset
      rx = 1 ;
      rdy_clr = 1 ;
      repeat(2) @(posedge clk_50m) ;
      rdy_clr = 0 ;

      // serial waveform
      rx = 1 ; #8.7us ; // idle
      rx = 0 ; #8.7us ; // start bit
      for ( int i=0 ; i<8 ; i++ ) begin
         rx = ( testvalue & (1<<i) ) ? 1 : 0 ;
         #8.7us ;
      end
      rx = 1 ; #8.7us ; // stop bit

      // check results
      wait(rdy) ;

      if ( data != testvalue )
        $display("failed: data=%d", data) ;
      else
        $display("passed: data=%d", data) ;

      #8.7us ;

      $stop ;

   end

   // clock
   initial begin
     clk_50m = 0 ;
      forever
        #10ns clk_50m = ~clk_50m ;
   end

endmodule
```

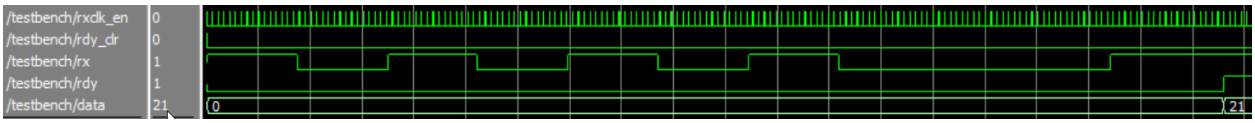

Figure 1: Sample simulation waveforms.