ELEX 7660 : Digital System Design
Term 201810

MIDTERM EXAMINATION - PART 1
12:30 AM – 1:20 PM
February 20, 2018

This exam has two (2) questions on four (4) pages. The marks for each question are as indicated. There are a total of 14 marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Books and notes are allowed. No electronic devices other than calculators are allowed.

This exam paper is for:

Exam 1 A00123456

Each exam is equally difficult.
Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

Question	Mark	Max.
1		9
2		5
Total		16

Question 1 (9 marks)

The following declarations and initializations appear in a System Verilog module:

```
logic [7:0] a = 8'h08 ;
logic [3:0] b [3:0]  = '{ 4'bxxxx, 4'h1, 4'd2, 4'b0011 } ;
logic signed [7:0] c = 8'b1 ;
```

Evaluate the expression in the first column in each row in the following table and write the size (in bits), and the value (in binary). If the size is more than 8 bits, you need only show the least-significant 8 bits.

expression	size (bits)	value (in binary, 8 or fewer l.s. bits)
`4'sb1000 >>> 3`		
`^c`		
`1 && 2`		
`b[0][1:0]`		
`2*c`		
`c[0] ? b[2] : b[1]`		
`{a[0],b[0]}`		
`{4{c[0]}}`		
`a|c`		

Question 2 (5 marks)

Consider the following System Verilog simulation:

```
module midterm1 ;

   logic clk=0 ;
   logic [7:0] x, y=1 ;

   initial begin
      $dumpfile("midterm1-2.vcd");
      $dumpvars ;
      for ( int i=0 ; i<6 ; i++ ) begin
         #1us clk = ~clk ;
      end
      $finish ;
   end

   always_ff@(posedge clk)
     begin
        y <= x ;
     end

   always_comb begin
      x = y + y ;
   end

endmodule
```

(a) Draw the `clk` waveform on the graph above. Mark transitions between values (using ⎍ or ⎺_). Label the transition times in microseconds. *Hint: the simulation ends when* `$finish` *is executed.*

(b) Draw the `x` waveform on the graph above. Mark transitions between values (e.g. using ⟩⟨). Show the value of `x` between the transitions in decimal (e.g. ⟩5⟨).

(c) Draw the `y` waveform on the graph above. Show the transitions and the value of `y` between the transitions.

– This page intentionally left blank. –

ELEX 7660 : Digital System Design
Term 201810

MIDTERM EXAMINATION - PART 1
12:30 AM – 1:20 PM
February 20, 2018

This exam has two (2) questions on four (4) pages. The marks for each question are as indicated. There are a total of 14 marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Books and notes are allowed. No electronic devices other than calculators are allowed.

This exam paper is for:

Exam 2 A00123456

Each exam is equally difficult.
Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

Question	Mark	Max.
1		9
2		5
Total		16

Question 1 (9 marks)

The following declarations and initializations appear in a System Verilog module:

```
logic [7:0] a = 8'h08 ;
logic [3:0] b [3:0]  = '{ 4'bxxxx, 4'h1, 4'd2, 4'b0011 } ;
logic signed [7:0] c = 8'b1 ;
```

Evaluate the expression in the first column in each row in the following table and write the size (in bits), and the value (in binary). If the size is more than 8 bits, you need only show the least-significant 8 bits.

expression	size (bits)	value (in binary, 8 or fewer l.s. bits)
`1 && 2`		
`{4{c[0]}}`		
`b[0][1:0]`		
`4'sb1000 >>> 3`		
`^c`		
`{a[0],b[0]}`		
`c[0] ? b[2] : b[1]`		
`2*c`		
`a|c`		

Question 2 (5 marks)

Consider the following System Verilog simulation:

```
module midterm1 ;

   logic clk=0 ;
   logic [7:0] x, y=2 ;

   initial begin
      $dumpfile("midterm1-1.vcd");
      $dumpvars ;
      for ( int i=0 ; i<6 ; i++ ) begin
         #1us clk = ~clk ;
      end
      $finish ;
   end

   always_ff@(posedge clk)
     begin
        y <= x ;
     end

   always_comb begin
      x = y + y ;
   end

endmodule
```

(a) Draw the `clk` waveform on the graph above. Mark transitions between values (using ⎍ or ⎺_). Label the transition times in microseconds. *Hint: the simulation ends when* `$finish` *is executed.*

(b) Draw the `x` waveform on the graph above. Mark transitions between values (e.g. using ⟩⟨). Show the value of `x` between the transitions in decimal (e.g. ⟩5⟨).

(c) Draw the `y` waveform on the graph above. Show the transitions and the value of `y` between the transitions.

– This page intentionally left blank. –