Introduction to Digital Design with Verilog HDL

Exercise 1: What changes would result in a 3-input OR gate?

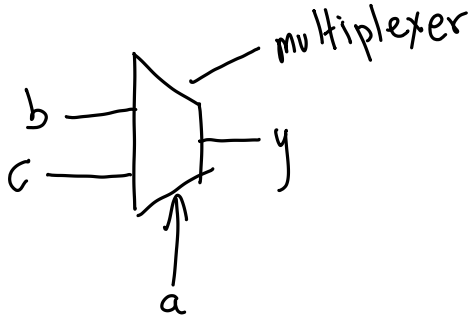
```
// AND gate in Verilog

module ex1 ( input logic a, b, c,
             output logic y ) ;

   assign y = a & b ;   a | b | c ;

endmodule
```

Exercise 2: What schematic would you expect if the statement was `assign y = a ? b : c ;`?



Exercise 3: What change might produce a 4-bit 4-to-1 multiplexer controlled by a 2-bit `sel` input?

```
                              [1:0]
module ex3 (input logic sel,
            input logic [3:0] a, b, c, d
            output logic [3:0] y) ;

   always_comb begin
      if ( sel ) y <= a ;
      else y <= b ;
   end

endmodule
```

if (sel == 2'b00)
  y = a
....

Exercise 4: If the signal `i` is declared as `logic [2:0] i;`, what is the 'width' of `i`? If `i` has the value 6 (decimal), what is the value of `i[2]`? Of `i[0]`?

i is 3 bits (2...0)

6 = 1 1 0

i[2] = 1

i[0] = 0

Exercise 5: What are the values in decimal of the constants in the code above?

```
0: d = 8'hc0 ;
1: d = 8'b1111_1001 ;
2: d = 'ha4 ;
default: d = 176 ;
```

192

F9 = 249

A = 164

176

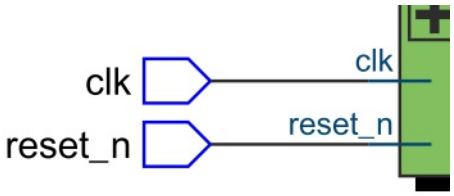
Exercise 6: What is the output in binary when the input is `a=2'b10`

2_{10}

A4 = 1010 0100

Exercise 7: Which ports are mapped by `.*` in the instantiation of `ex5`?

```
ex5 ex5_0 ( .*, .x(count) ) ;
```



Exercise 8: Write the module declaration for ex7.

in ex7: input [3:0] n
output [7:0] seg.

```
ex7 ex7_0 ( .n(count), .seg ) ;
```

```
output logic [7:0] seg ) ;

logic [3:0] count ;
```

```
module ex7 ( input [3:0] n,
             output [7:0] seg) ;
```

Exercise 9: Where in the code is the Device Under Test (DUT) instantiated?

```
ex5 ex5_0 (.*);
```

port connections
instance name
module name