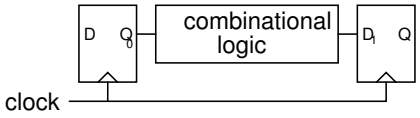
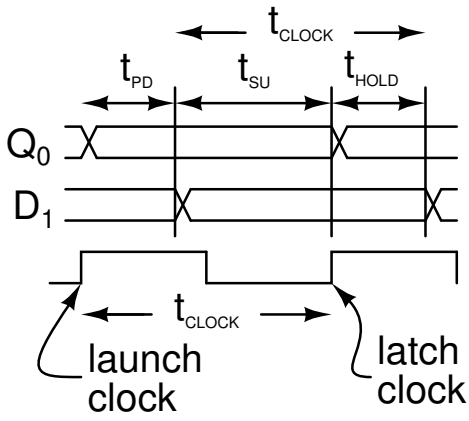
Timing Basics

In a previous lecture we considered that digital circuits are composed of flip-flops and registers with combinational logic between their outputs and inputs:



If the propagation delay and clock period are known, we can establish the setup and hold times:

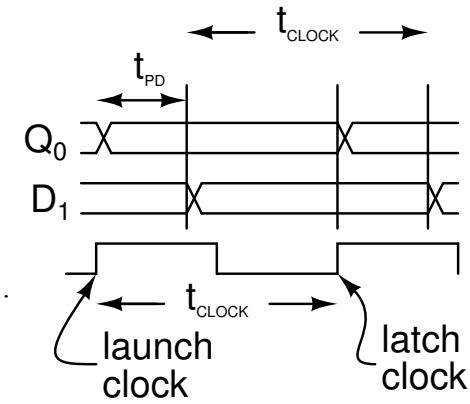


Exercise 1: Based on the diagram above, what is the setup time – the time from the input being valid to the latching clock edge?

Exercise 2: Based on the diagram above, what is the hold time – the time from the latching clock edge to the input changing?

These are the actual setup and hold times. A flip-flop will require minimum setup and hold times to ensure correct operation. The amount by which this minimum is exceeded is called the *slack*.

Exercise 3: Draw minimum setup and hold times on the diagram below that are smaller than the actual setup and hold times. Indicate the slack times.



The minimum hold time requirement is usually zero.

Exercise 4: What is the minimum allowable propagation delay for a circuit that uses flip-flops with a zero minimum hold time?

A timing analyzer computes the setup and hold slack time for every combinational logic path between a flip-flop output and input and flags those that are negative (i.e. where the requirement is not met).