Common HDL Constructs (Part 2)

For efficient logic design it is necessary to be able to visualize the hardware that would be generated by an HDL description. This lecture describes some common HDL constructs and their corresponding hardware implementations.
After this lecture you should be able to convert back and forth between simple digital logic circuits and the corresponding Verilog descriptions.
[This part of the lecture presents schematics and asks you to derive the corresponding HDL construct.]

Write the Verilog HDL corresponding to each of the following schematics: