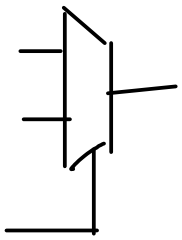
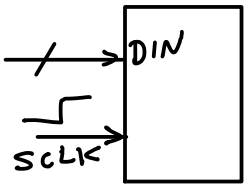
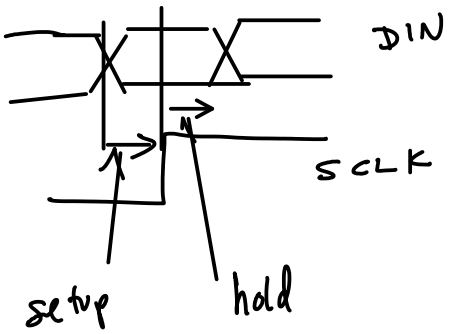
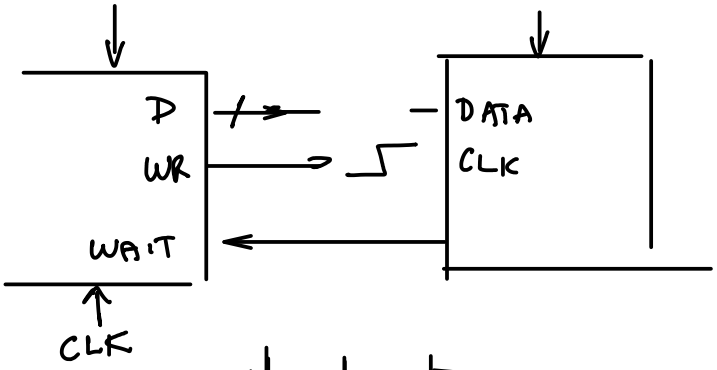
Timing Analysis

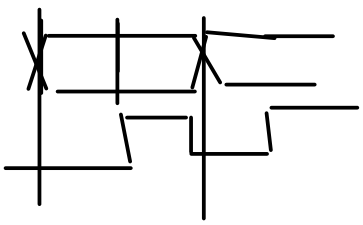
Exercise 1: Which of the three basic specifications (delay, setup and hold times) would apply to a multiplexer? When writing a control port on a chip?



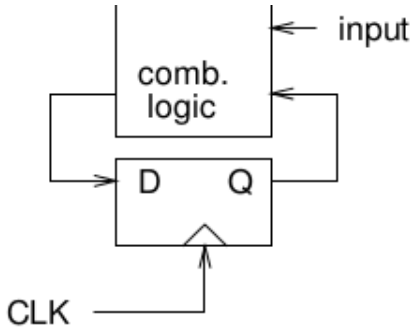


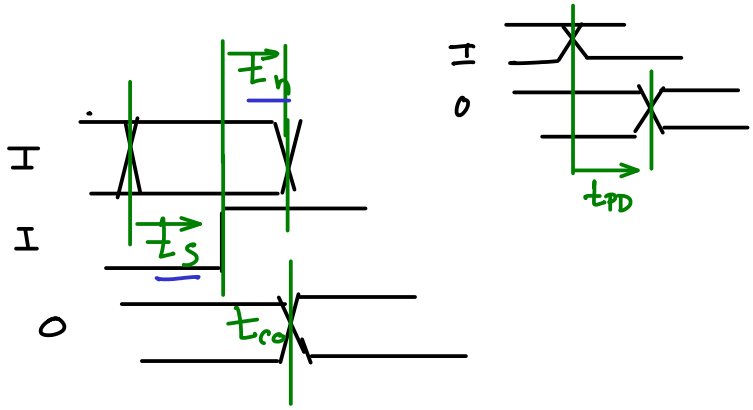






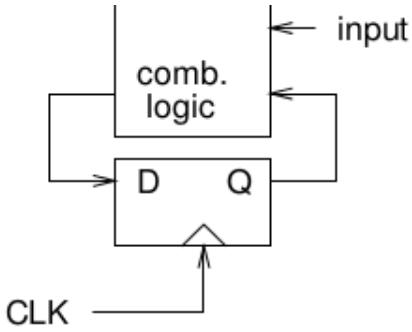
Exercise 2: Draw separate timing diagrams for the flip-flop and the combinational circuit. Assume the flip-flops require a minimum setup time, t_s, of 20ns and a minimum hold time, t_h of 0 ns. Assume the maximum clock-to-output propagation delay for the flip-flop is $t_{CO} = 5$ ns (again, with no minimum). Assume that the maximum propagation delay through the combinational logic circuit is guaranteed to be a maximum of $t_{PD} = 20$ ns, and there is no minimum for t_{PD}. Label the timing diagrams with each of these specifications.





Exercise 3: Draw a timing diagram for the complete circuit. It should include the clock CLK, the flip-flop's output, Q, and its input, D. Indicate cause–effect relationships between the signal edges using arrows.

Derive expressions for each timing requirement in terms of the clock period and guaranteed timing specifications for a clock frequency of 10 MHz. Substitute the actual values and compute the remaining margin. Will this circuit operate properly as far as timing is concerned? What if the hold time requirement was 5 ns?

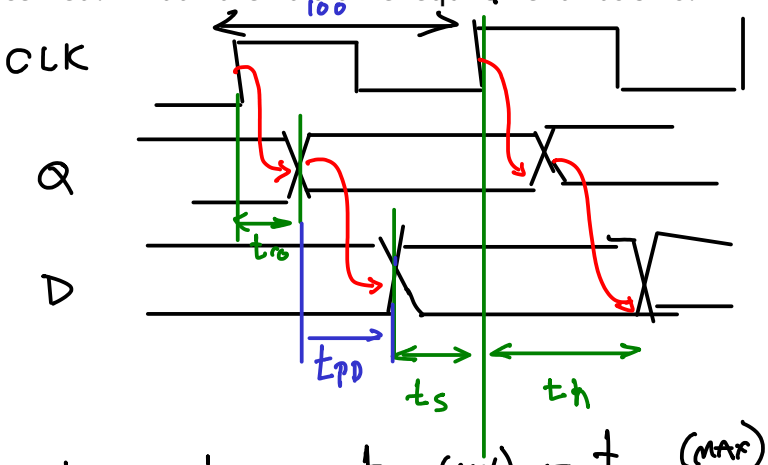


$t_{pd} = 20ns$

$t_h = 0$

$t_{co} = 5$

$t_s = 20$



$$t_s = t_{cycle} - t_{co\,(MAX)} - t_{PD\,(MAX)}$$
$$= 100 - 5 - 20 = 75ns.$$

$$t_h = t_{co\,(MIN)} + t_{PD\,(MIN)} =$$