Verilog Statements

Exercise 1: Should each of the following nets (or variables) be declared `wire` or `reg`?

```
module test (a,b,c,d,q) ;
dff d0 (clk,d,q) ; // assume only q is an output
assign d = a & b ;
always@* clk = a & c ;
endmodule
```

reg (assigned in procedure (always))

all others are wire (not assigned in procedure)

wand

wor

tri

in Verilog this is a "wand" resolution function.

	0	1	z	x
0	0	0		
1	0	1		
z				
x