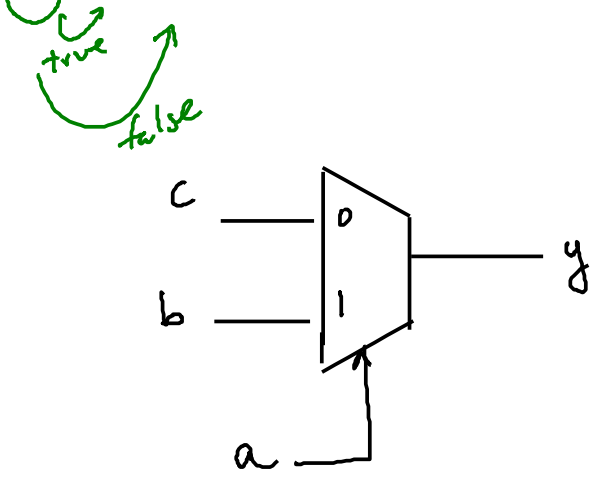
Exercise 1:What changes would result in a 3-input OR gate?

```
input logic a, b, c,

y = a | b | c;
```

Exercise 2:What schematic would you expect if the statement was assign y = a ? b : c ;?



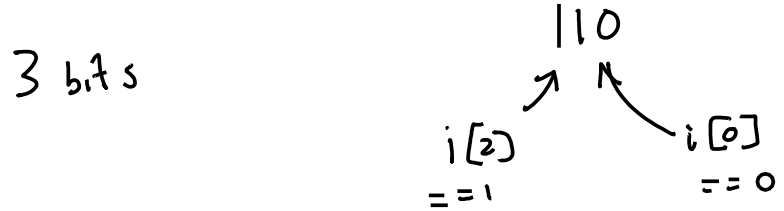
Exercise 3: What change might produce a 4-bit 3-to-1 multiplexer controlled by a 2-bit sel input?

```
module ex3 (input logic sel,
            input logic [3:0] a, b,
            output logic [3:0] y) ;

   always_comb begin
      if ( sel ) y = a ;
      else y = b ;
   end

endmodule
```

Exercise 4: If the signal i is declared as logic [2:0] i;, what is the 'width' of i? If i has the value 6 (decimal), what is the value of i[2]? Of i[0]?

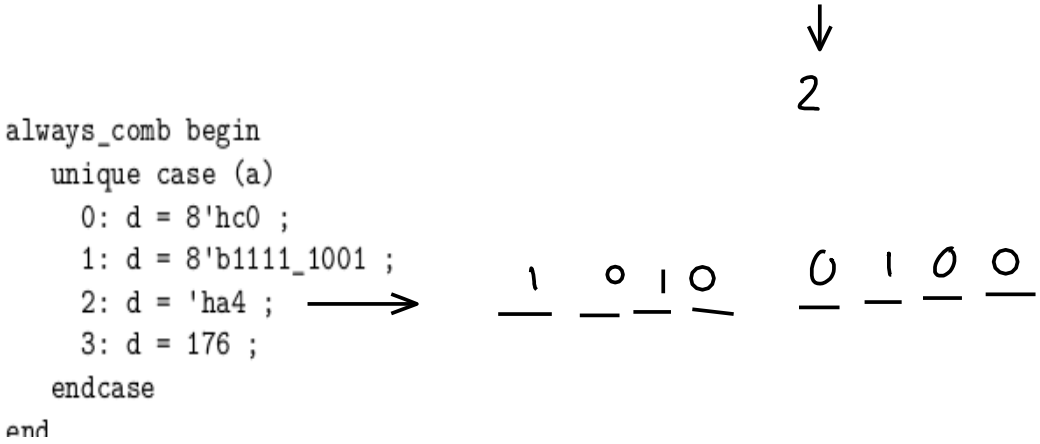


Exercise 5: What are the values in decimal of the constants in the code above?

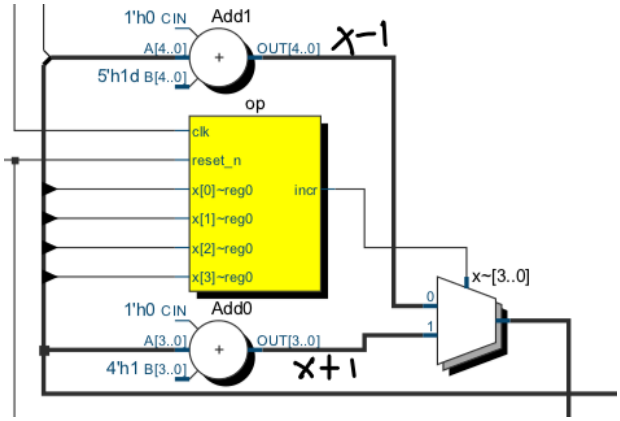
```
0: d = 8'hc0 ;
1: d = 8'b1111_1001 ;
2: d = 'ha4 ;
3: d = 176 ;
```

Exercise 6: What is the output in binary when the input is a=2'b10

```
always_comb begin
   unique case (a)
     0: d = 8'hc0 ;
     1: d = 8'b1111_1001 ;
     2: d = 'ha4 ;
     3: d = 176 ;
   endcase
end
```

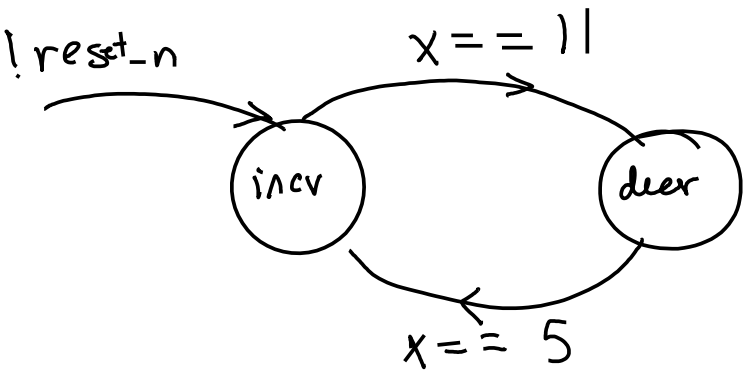


Exercise 7: Label the x+1 and x-1 buses.



Exercise 8Draw the state transition diagram for the op register.

```
always_comb begin
   if ( ! reset_n )       next = incr ;
   else if ( x == 4'd05 ) next = incr ;
   else if ( x == 4'd11 ) next = decr ;
   else                   next = op ;
end
```



Exercise 9Which ports are mapped by .* in the instantiation of ex5?

```
ex5 ex5_0 ( .*, .x(count) ) ;
ex7 ex7_0 ( .n(count), .seg ) ;

module ex5 ( input logic reset_n, clk,
             output logic [3:0] x ) ;
```

Exercise 10Write the module declaration for ex7.

```
module ex7 (input logic [3:0] n, output logic [7:0] seg);
```

Exercise 11: What is the minimum number of clock cycles required to transfer one data word over an interface with `ready/valid` handshaking? Maximum?

min = 1

max = ∞