

Introduction to Digital Design with Verilog HDL

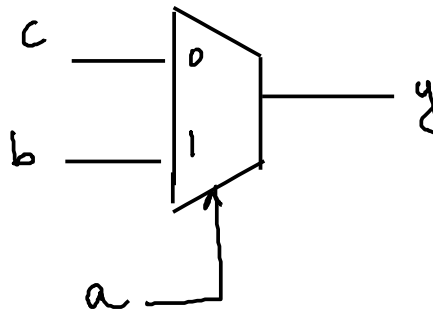
Exercise 1: What changes would result in a 3-input OR gate?

input logic $a, b, c,$

$$y = a | b | c ;$$

Exercise 2: What schematic would you expect if the statement was `assign y = a ? b : c ;`?

Handwritten annotations:
A green circle highlights the `a` in the code. A green arrow labeled "true" points from the circle to the `b` in the code. Another green arrow labeled "false" points from the circle to the `c` in the code.



Exercise 3 What change might produce a 4-bit 3-to-1 multiplexer controlled by a 2-bit sel input?

```

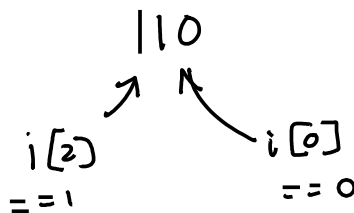
module ex3 (input logic sel,
            input logic [3:0] a, b, c,
            output logic [3:0] y);
    always_comb begin
        if (sel == 0) y = a;
        else if (sel == 1) y = b;
        else y = c;
    end
endmodule

```

Handwritten annotations:
 - Above 'sel': '5' and 'b0cb d'
 - Above 'sel' in the code: '[1:0]' with an arrow pointing to 'sel'
 - Above 'a, b, c': '4'
 - Above 'y) ;': '4'
 - Next to 'if (sel == 0)': '5'
 - Next to 'if (sel == 1)': '1'
 - Next to 'else y = c;': 'else'
 - Next to 'y = a;': 'y = a;'
 - Next to 'y = b;': 'y = b;'
 - Next to 'y = c;': 'y = c;'
 - Next to 'end': 'end'
 - Next to 'endmodule': 'endmodule'

Exercise 4 If the signal i is declared as logic [2:0] i;, what is the 'width' of i? If i has the value 6 (decimal), what is the value of i[2]? Of i[0]?

3 bits



Exercise 5 What are the values in decimal of the constants in the code above?

```

0: d = 8'hc0 ;    C 0 = 12 x 16 = 192
1: d = 8'b1111_1001 ;    F 9 = 15 x 16 + 9 = 249
2: d = 'ha4 ;    A 4 = 10 x 16 + 4 = 164
3: d = 176 ;    176

```

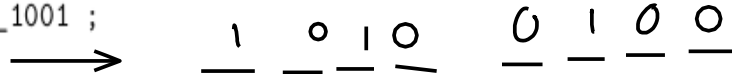
Exercise 6 What is the output in binary when the input is $a=2'b10$

↓
2

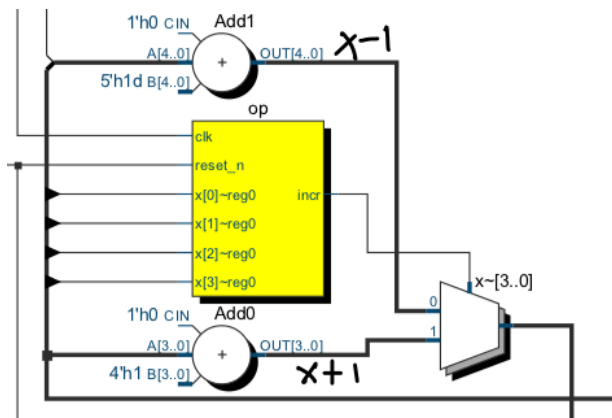
```

always_comb begin
  unique case (a)
    0: d = 8'hc0 ;
    1: d = 8'b1111_1001 ;
    2: d = 'ha4 ;
    3: d = 176 ;
  endcase
end

```



Exercise 7 Label the $x+1$ and $x-1$ buses.

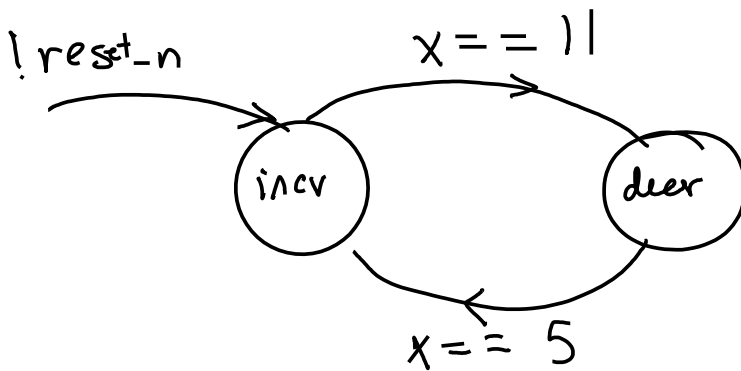


Exercise 8 Draw the state transition diagram for the op register.

```

always_comb begin
  if ( ! reset_n )      next = incr ;
  else if ( x == 4'd05 ) next = incr ;
  else if ( x == 4'd11 ) next = decr ;
  else                  next = op ;
end

```



Exercise 9 Which ports are mapped by .* in the instantiation of ex5?

```

ex5 ex5_0 ( .*, .x(count) ) ;
ex7 ex7_0 ( .n(count), .seg ) ;

```

→ reset_n, clk

```

module ex5 ( input logic reset_n, clk,
             output logic [3:0] x ) ;

```

Exercise 10 Write the module declaration for ex7.

```
module ex7 (input logic [3:0] n, output logic [7:0] seg);
```

Exercise 11: What is the minimum number of clock cycles required to transfer one data word over an interface with ready/valid handshaking? Maximum?

min = 1
max = ∞