ELEX 7660 : Digital System Design
Term 201710

MIDTERM EXAMINATION - PART 2
1:30 PM – 2:20 PM
February 28, 2017

This exam has two (2) questions on five (5) pages. The marks for each question are as indicated. There are a total of 18 marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Books and notes are allowed. No electronic devices other than calculators are allowed.

This exam paper is for:

Exam 1 A00123456

Each exam is equally difficult.
Answer your own exam.

Do not start until you are told to do so.

Name: _____

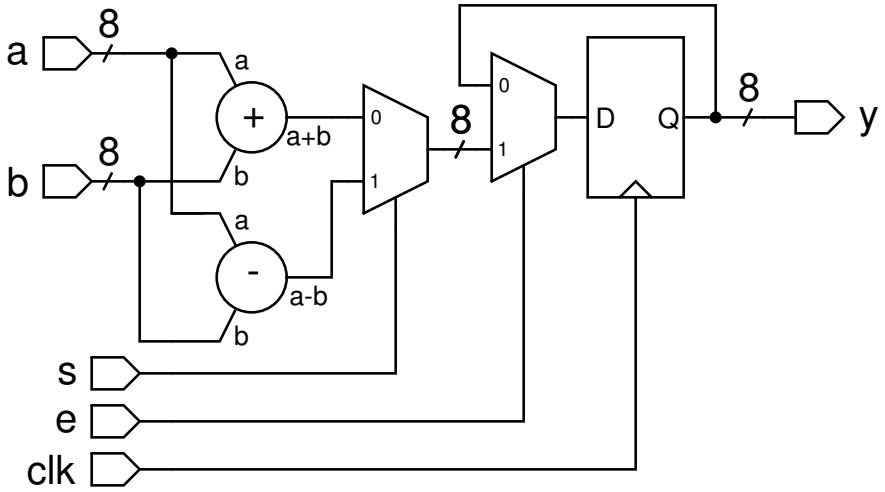
BCIT ID: _____

Signature: _____

Question	Mark	Max.
1		9
2		9
Total		18

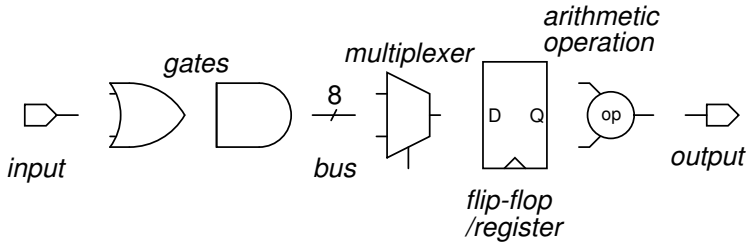
Question 1 (9 marks)

Write a System Verilog module that models the schematic shown below on the facing page. Use `logic` signal types throughout. Include all code from `module` to `endmodule`. Where the order of declarations or statements is not significant you may use any order.



Question 2 (9 marks)

Using the following symbols:



draw a schematic for the following Verilog module on the facing page. Label the inputs and outputs. Indicate the bus width if it's more than 1 bit.

```
module mkmini
  ( output logic [15:0] a,
    input  logic [15:0] d,
    output logic [15:0] mini,
    input logic reset, clk ) ;

   logic [15:0] a_next ;
   logic [15:0] mini_next ;

   always@(posedge clk) begin
      mini <= mini_next ;
      a <= a_next ;
   end

   always_comb begin
      if ( reset )
        mini_next = '1 ;
      else
        mini_next = d < mini ? d : mini ;

      if ( reset )
        a_next = '0 ;
      else
        a_next = a + 1'd1 ;
   end
endmodule
```

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Exam 2 A00123456

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Signature: _____

Question	Mark	Max.
1		9
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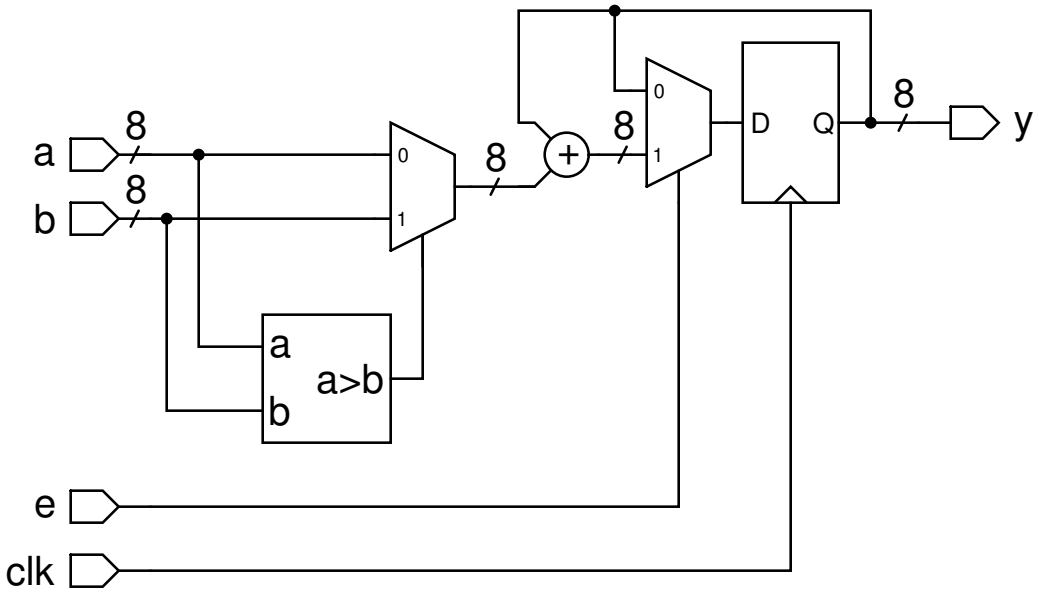
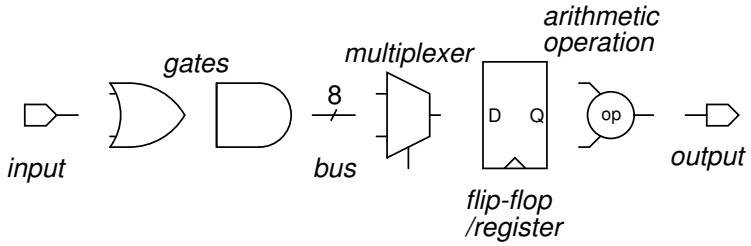


Question 2 (9 marks)

Using the following symbols:



draw a schematic for the following Verilog module on the facing page. Label the inputs and outputs. Indicate the bus width if it's more than 1 bit.

```
module mksum
  ( output logic [15:0] a,
    input  logic [15:0] d,
    output logic [15:0] sum,
    input logic reset, clk ) ;

   logic [15:0] a_next ;
   logic [15:0] sum_next ;

   always@(posedge clk) begin
      sum <= sum_next ;
      a <= a_next ;
   end

   always_comb begin
      sum_next = reset ? '0 : sum + d ;

      if ( reset )
        a_next = '0 ;
      else
        a_next = a + 1'd1 ;
   end

endmodule
```

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