ELEX 7660 : Digital System Design
Term 201710

MIDTERM EXAMINATION - PART 1
12:30 AM – 1:20 PM
February 27, 2017

This exam has two (2) questions on four (4) pages. The marks for each question are as indicated. There are a total of 16 marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Books and notes are allowed. No electronic devices other than calculators are allowed.

This exam paper is for:

Exam 1 A00123456

Each exam is equally difficult.
Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

Question	Mark	Max.
1		9
2		7
Total		16

Question 1 (9 marks)

The following declarations and initializations appear in a System Verilog module:

```
logic signed [7:0] a = 8'h80 ;
logic [3:0] b [3:0]  = '{ 4'bxxxx, 4'h1, 4'd2, 4'b0011 } ;
logic [3:0] c        = '1 ;
```

For each row in the following table, write in the size (in bits) and the value (in binary) of the expression in the first column. If the size is more than 8 bits, you need only show the least-significant 8 bits.

expression	size (bits)	value (binary, 8 or fewer l.s. bits)
`a+1`		
`b[2]==c`		
`a[0] ? 0 : 2`		
`b[1]`		
`b[0] ==? 4'bxxx1`		
`a >>> 1`		
`&c`		
`{2{a[7:4]}}`		
`c && a`		

Question 2 (7 marks)

Consider the following System Verilog simulation:

```
module midterm2 ;

   logic clk='0 ;
   logic [3:0] x=4'b0, y=4'b0 ;

   initial
     begin
        repeat(4) begin
           #1us ; //delay
           clk = ~clk ;
        end
        $finish ;
     end

   always_ff@(posedge clk)
     begin
        x <= x + 1 ;
        $display(x) ;
     end

   always_comb
     begin
        if ( x & 1 )
          y = 0 ;
        else
          y = x + 1 ;
     end

endmodule
```

(a) Draw the `clk` waveform on the graph above. Mark transitions between values (using ⎍ or ⎺_). Label the transition times in microseconds. *Hint: the simulation ends when* `$finish` *is executed.*

(b) Draw the `x` waveform on the graph above. Mark transitions between values (e.g. using ⨯). Show the value of `x` between the transitions in decimal (e.g. ⨯ 5 ⨯).

(c) Write the values printed by the `$display()` system task:

(d) Draw the `y` waveform on the graph above. Show the transitions and the value of `y` between the transitions.

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This exam paper is for:

Exam 2 A00123456

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Name: _____

BCIT ID: _____

Signature: _____

Question	Mark	Max.
1		9
2		7
Total		16

Question 1 (9 marks)

The following declarations and initializations appear in a System Verilog module:

```
logic signed [7:0] a = 8'h80 ;
logic [3:0] b [3:0]  = '{ 4'bxxxx, 4'h1, 4'd2, 4'b0011 } ;
logic [3:0] c        = '1 ;
```

For each row in the following table, write in the size (in bits) and the value (in binary) of the expression in the first column. If the size is more than 8 bits, you need only show the least-significant 8 bits.

expression	size (bits)	value (binary, 8 or fewer l.s. bits)
`a+1`		
`b[0] ==? 4'bxxx1`		
`a[0] ? 0 : 2`		
`{2{a[7:4]}}`		
`&c`		
`a >>> 1`		
`b[1]`		
`c && a`		
`b[2]==c`		

Question 2 (7 marks)

Consider the following System Verilog simulation:

```
module midterm1 ;

   logic clk='0 ;
   logic [3:0] x=4'b1, y=4'b0 ;

   initial
     begin
        repeat(4) begin
           #1us ; //delay
           clk = ~clk ;
        end
        $finish ;
     end

   always_ff@(posedge clk)
     begin
        x <= x + 2 ;
        $display(x) ;
     end

   always_comb
     begin
        if ( x & 1 )
          y = x + 1 ;
        else
          y = 0 ;
     end

endmodule
```

(a) Draw the `clk` waveform on the graph above. Mark transitions between values (using ⎍ or ⎺_). Label the transition times in microseconds. *Hint: the simulation ends when* `$finish` *is executed.*

(b) Draw the `x` waveform on the graph above. Mark transitions between values (e.g. using ⨯). Show the value of `x` between the transitions in decimal (e.g. ⨯ 5 ⨯).

(c) Write the values printed by the `$display()` system task:

(d) Draw the `y` waveform on the graph above. Show the transitions and the value of `y` between the transitions.

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