Solutions to Assignment 3

Question 1

The pin functions described in Section 5, the timing specifications given in Section 6.6 and the timing diagrams given in Figures 2 and 3 from the TI ADC128S022 ADC data sheet are shown below.

(a) *For the device*, $\overline{\text{CS}}$ (CSn), DIN and SCLK are inputs. However, *for the FPGA*, DOUT is an input.

(b) *For the device*, DOUT is an output. However, *for the FPGA*, $\overline{\text{CS}}$ (CSn), DIN and SCLK are outputs.

(c) The following table summarizes the 10 timing specifications ("req" means a timing requirement, "resp" means a guaranteed timing response):

symbol	from	to	req./ resp.	min./ max.	value (ns)
t_{CSH}	SCLK	CSn	req	min	10
t_{CSS}	CSn	SCLK	req	min	10
t_{EN}	CSn	DOUT	resp	max	30
t_{DACC}	SCLK	DOUT	resp	max	27
t_{DHLD}	SCLK	DOUT	resp	-	-
t_{DS}	DIN	SCLK	req	min	10
t_{DH}	SCLK	DIN	req	min	10
t_{CH}	SCLK	SCLK	req	min	$0.4t_{SCLK}$
t_{CL}	SCLK	SCLK	req	min	$0.4t_{SCLK}$
t_{DIS}	CSn	DOUT	resp	max	20

(d) SDC timing contraints could be written as follows (tcl substitutes 490, the value of the expression in `[expr...]`, for this argument):

t_{CSH}:

```
set_output_delay -clock [get_ports clk] -reference_pin [get_ports SCLK]
                 -min 10 [get_ports CSn]
```

t_{CSS}:

```
set_output_delay -clock [get_ports clk] -reference_pin [get_ports SCLK]
                -max [expr 500 - 10] [get_ports CSn]
```

t_{DACC}:

```
set_input_delay -clock [get_ports clk] -reference_pin [get_ports SCLK]
                -max 27 [get_ports DOUT]
```

t_{DS}:

```
set_output_delay -clock [get_ports clk] -reference_pin [get_ports SCLK]
                -max [expr 500 - 10] [get_ports DIN]
```

t_{DH}:

```
set_output_delay -clock [get_ports clk] -reference_pin [get_ports SCLK]
                -min 10 [get_ports DIN]
```

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
$\overline{CS}$	1	Digital I/O	Chip select. On the falling edge of $\overline{CS}$, a conversion process begins. Conversions continue as long as $\overline{CS}$ is held low.
V_A	2	Power Supply	Positive analog supply pin. This voltage is also used as the reference voltage. This pin should be connected to a quiet +2.7-V to +5.25-V source and bypassed to GND with 1-µF and 0.1-µF monolithic ceramic capacitors located within 1 cm of the power pin.
AGND	3	Power Supply	The ground return for the analog supply and signals.
IN0 to IN7	4-11	Analog I/O	Analog inputs. These signals can range from 0 V to V_{REF}.
DGND	12	Power Supply	The ground return for the digital supply and signals.
V_D	13	Power Supply	Positive digital supply pin. This pin should be connected to a +2.7-V to V_A supply, and bypassed to GND with a 0.1-µF monolithic ceramic capacitor located within 1 cm of the power pin.
DIN	14	Digital I/O	Digital data input. The ADC128S022's Control Register is loaded through this pin on rising edges of the SCLK pin.
DOUT	15	Digital I/O	Digital data output. The output samples are clocked out of this pin on the falling edges of the SCLK pin.
SCLK	16	Digital I/O	Digital clock input. The specified performance range of frequencies for this input is 0.8 MHz to 3.2 MHz. This clock directly controls the conversion and readout processes.

6.6 Timing Specifications

The following specifications apply for $V_A = V_D = 2.7$ V to 5.25 V, AGND = DGND = 0 V, $f_{SCLK} = 0.8$ MHz to 3.2 MHz, $f_{SAMPLE} =$ 50 ksps to 200 ksps, and $C_L = 50$ pF. Maximum and minimum limits apply for $T_A = T_{MIN}$ to T_{MAX}: all other limits $T_A = 25$°C.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX(1)	UNIT
t_{CSH}	$\overline{CS}$ hold time after SCLK rising edge		10	0		ns
t_{CSS}	$\overline{CS}$ set-up time prior to SCLK rising edge		10	4.5		ns
t_{EN}	$\overline{CS}$ falling edge to DOUT enabled			5	30	ns
t_{DACC}	DOUT access time after SCLK falling edge			17	27	ns
t_{DHLD}	DOUT hold time after SCLK falling edge			4		ns
t_{DS}	DIN set-up time prior to SCLK rising edge		10	3		ns
t_{DH}	DIN hold time after SCLK rising edge		10	3		ns
t_{CH}	SCLK high time		0.4 × t_{SCLK}			ns
t_{CL}	SCLK low time		0.4 × t_{SCLK}			ns
t_{DIS}	$\overline{CS}$ rising Edge to DOUT high-impedance	DOUT falling		2.4	20	ns
		DOUT rising		0.9	20	ns

(1) Data sheet min/max specification limits are specified by design, test, or statistical analysis.

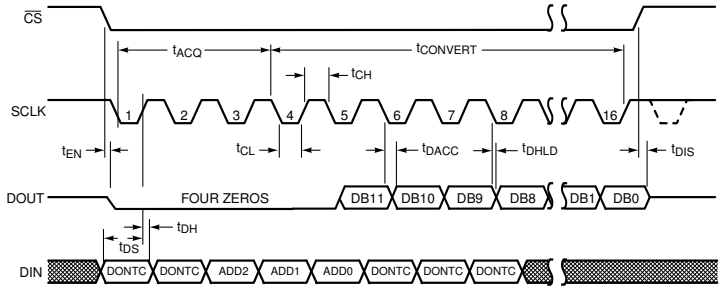

Figure 2. ADC128S022 Serial Timing Diagram

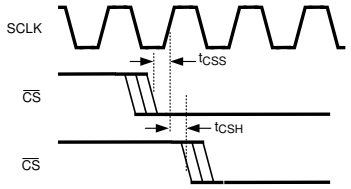

Figure 3. SCLK and $\overline{CS}$ Timing Parameters