Assignment 3

Due Tuesday, April 11. Submit your assignment using the appropriate dropbox on the course web site. Assignments submitted after the solutions are made available will be given a mark of zero.

Question 1

The data sheet for the TI ADC128S022 ADC on the DE0-Nano board is available on the course web site. Using the pin functions described in section 5, the timing specifications given in section 6.6 and the timing diagrams given in Figures 2 and 3, answer the following questions:

(a) Which signals (pins) are inputs?

(b) Which signals are outputs?

(c) A table, showing for each of the 10 timing specifications:

- the specification symbol
- the signal from which the time is measured (starting point)
- the signal to which the specification is measured (ending point)
- whether the specification is a requirement (if the end point is an input) or a guaranteed response (if the end point is an output)
- whether it's a maximum or minimum
- the value in nanoseconds

(d) For each of the timing specifications t_{CSH}, t_{CSS}, t_{DACC}, t_{DS}, and t_{DH}, write an appropriate SDC timing constraint. You may assume your design uses the same signal names as the datasheet (DIN, DOUT, SCLK, CSn) and a 2 MHz SCLK frequency (500 ns period). Show your work.

- if it's a guaranteed response (e.g. a propagation delay or access time), a `set_input_delay` statement.
- if it's a timing requirement (e.g. setup or hold) a `set_output_delay` statement.

In the SDC statements assume SCLK is a signal generated by your design instead of being a true clock and that the clock is a signal named `clk` which you specify as the `-clock` parameter for each constraint. Use the `-reference_pin` parameter to specify the port to which the delay is relative (e.g.`-reference_pin [get_ports SCLK]`).

The syntax for the set_input_delay and set_output_delay are available on-line and in the reference manual.