ELEC 464 : MICROCOMPUTER SYSTEM DESIGN
1996/97 WINTER SESSION TERM 1

Solutions to Assignment 5

Question 1

The CPU has an 8-bit data bus and each device can store 2 bits so 4 devices need to be enabled at a time (i.e. connected in parallel). Each such bank will supply 64 kBytes. Since a total of 128 kBytes is required, two banks are necessary. Figure **??** shows the design of the memory system.

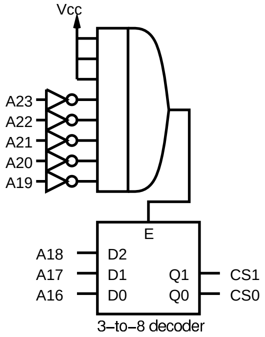
Question 2

The CPU has a 16-bit data bus and each device can store 8 bits so 2 devices need to be enabled at a time (i.e. connected in parallel). The RAM bank will supply 128 k words of 2 bytes each = 256 kBytes and the ROM bank will supply 32 k words = 64 kBytes. Figure **??** shows the design of the memory system.

Question 3

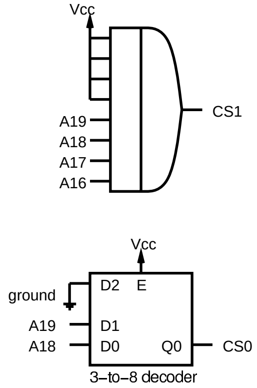
Each bank in question 1 holds 64 kBytes so the LS 16 bits of the address bus must go directly to the chips' address pins. The remaining 8 bits of the 24 bit address bus (A16 to A23) go to the decoder which should select the first bank when the input is 0000 0000 and the second bank when the input is 0000 0001.

The decoder schematic is:



The RAM bank in Question 2 occupies 256 kB of the CPU's address space so the LS 18 bits of the address are used to select a memory location within the RAM chips. The remaining 2 bits of the 20 bit address bus (A19 to A18) are used by the address decoder which should enable the RAM CS signals when the input is 00. The EPROM bank occupies 64 kB of the CPU address space so the LS 16 address bits select a byte in the EPROMs and the remaining 4 bits (A19 to A16) are used by the address decoder. To put the memory at a starting location of $F0000_{16}$ the ERPOM CS must be asserted when the input is 1111.

The decoder schematic is:



VHDL descriptions of the two circuits can be written using if-then-else statements as follows:

```
-- ELEC 464 Assignment 5, Question 1
-- Ed Casas, 1996/10/20
-- address decoder for 2-bank RAM array

entity decoder1 is
   port ( a : in bit_vector (23 downto 0) ;
      cs0, -- selects 64 kB RAM bank at 000000H
      cs1  -- selects 64 kB RAM bank at 010000H
             : out bit ) ;
end decoder1 ;

architecture rtl of decoder1 is
begin

   process(a)
   begin
      if a(23 downto 16) = "00000000" then
         cs0 <= ’1’ ;
         cs1 <= ’0’ ;
      elsif a(23 downto 16) = "00000001" then
         cs0 <= ’0’ ;
         cs1 <= ’1’ ;
      else
         cs0 <= ’0’ ;
         cs1 <= ’0’ ;
      end if ;
```

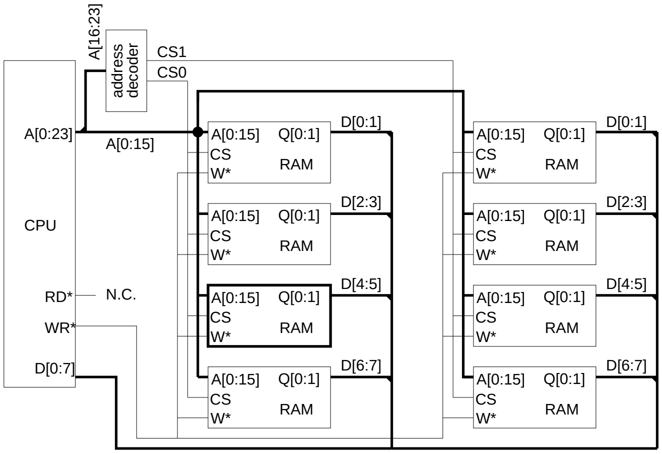


Figure 1: Solution to Question 1.

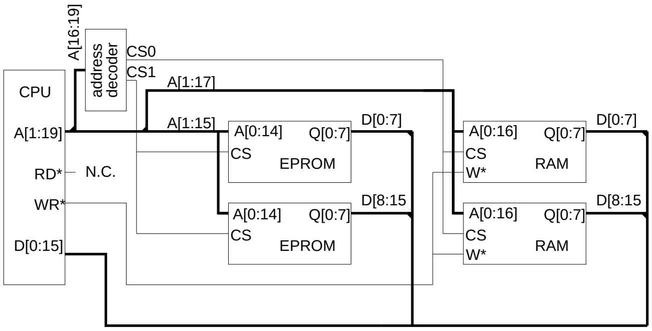
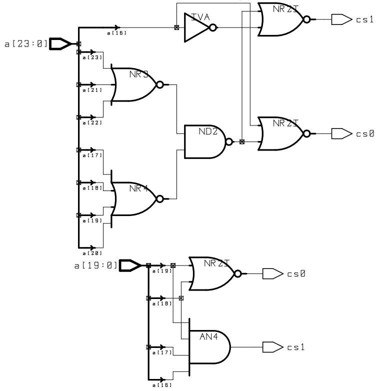


Figure 2: Solution to Question 2.

```
   end process ;

end rtl ;


-- ELEC 464 Assignment 5, Question 2
-- Ed Casas, 1996/10/20
-- address decoder for RAM and EPROM memories

entity decoder2 is
   port ( a : in bit_vector (19 downto 0) ;
      cs0, -- selects 256 kB RAM   at 00000H
      cs1  -- selects  64 kB EPROM at F0000H
             : out bit ) ;
end decoder2 ;

architecture rtl of decoder2 is
begin

   -- RAM decoder
   process(a)
   begin
      if a(19 downto 18) = "00" then
         cs0 <= ’1’ ;
      else
         cs0 <= ’0’ ;
      end if ;
   end process ;
```

```
   -- EPROM decoder
   process(a)
   begin
      if a(19 downto 16) = "1111" then
         cs1 <= ’1’ ;
      else
         cs1 <= ’0’ ;
      end if ;
   end process ;

end rtl ;
```

which produce the following two circuits:


a[23:0]
a[16]
a[23]
a[21]
a[22]
a[17]
a[18]
a[19]
a[20]
IVA
NR3
NR4
ND2
NR2I
NR2I
cs1
cs0
a[19:0]
a[19]
a[18]
a[17]
a[16]
NR2I
AN4
cs0
cs1