Solutions to Assignment 4

Question 1

We choose the least expensive device that meets the requirements. The most important requirements are: (1) one macrocell per bit of state or output, (2) one pin per input or output, (3) the minimum propagation delay, and (4) the number of clocks or sets of independently latched registers.

1. The three parts of this design will require approximately: (a) 12 macrocells, 12 pins, and 0 clocks, (b) 31 macrocells, 11 pins, and 1 clock, and (c) 96 macrocells (24+16+56), more than 16 pins, and 1 clock, for a total of about 139 macrocells, more than 39 pins, and 2 clocks. The highest clock speed is 100 kHz which implies a maximum propagation delay of less than 10 microseconds. This design would probably be implemented using an FPGA.

2. This design only requires 4 macrocells, 3 pins and one clock. A PAL would suffice.

3. This design would require about: 52 macrocells (16 for the register, and 16 for each CPU interface and 4 for the handshaking signals), 36 pins (2 sets of 16 plus 4 pins for handshaking) and one or two clocks (depending on the design). This is beyond the capabilities of a PAL but could be implemented with a typical CPLD.

4. This design requires 2 macrocells and 10 pins (8 inputs and 2 outputs). A PAL would be large enough and it would be possible to find one that met the 10 ns delay requirement.

Question 2

Tables **??** and **??** show how the margins for the various requirements are computed.

Question 3

8088 Requirements

The requirements on the clock inputs can only be met by the design of the clock circuit. This circuit was not specified in the question. If we assume a 1:2 (low:high) clock duty cycle the low time will be 66 ns and the high time will be 133 ns.

Similarly, the rise and fall times will depend on logic family or technology used to generate the clock.

Since the RDY, READY, HOLD (and INTR) signals are not used the requirements on these signals are can be ignored.

The data setup and hold times are the two remaining requirements and they only apply during read cycles. The timing diagram shows that these setup and hold times are measured from the start of bus cycle state T4 which starts on the falling edge of the clock.

However, the 16550 specifications for when the data is valid are delays (t_{RVD} and t_{HZ}) which are relative to the falling and rising edges respectively of RD*. To check whether the setup and hold times will be met it's necessary to convert these delays to the minimum setup and hold times relative to the clock edge at the start of T4. We can do this using the guaranteed timing of the 8088's RD* signal relative to clock edges. RD* goes active t_{CLRL} after the start of T2 and then goes inactive t_{CLRH} after the start of T4. Since there is a delay of exactly two clock periods between the start of T2 and the start of T4 we can derive the guaranteed setup and hold times. Figure **??** shows how the setup and hold times can be derived and Table **??** shows how the margins are computed.

16550 Requirements

Requirements Common to Read and Write Cycles

The timing requirements below relate to latching address and CS values on the trailing edge of ADS*

Requirement		Guaranteed		Margin	Met
Symbol	Value	Expression	Value		(Y/N)
MC68HC11 (2MHz) Requirements					
t_{ACCE} (35)	192	t_{ELQV}	20	172	Y
t_{ACCA} (29)	296	t_{AVQV}	45	251	Y
t_{DHR} (18)	10	t_{GHQZ}	0	-10	N
6290-45 Requirements					
t_{AVAV}	45	t_{cyc}	500	455	Y

Table 1: 68HC11 and 6290 read-cycle requirements.

Requirement		Guaranteed		Margin	Met
Symbol	Value	Expression	Value		(Y/N)
MCM6290-45 Requirements					
t_{AVWL}	0	t_{AVM}	84	84	Y
t_{AVWH}	35	t_{AVM} + PW_{EH}	84 + 222 = 306	271	Y
t_{WLWH}	35	PW_{EH}	222	187	Y
t_{DVWH}	20	PW_{EH} - t_{DDW}(max)	222 - 128 = 94	74	Y
t_{WHDX}	0	t_{DHW}	33	33	Y

Table 2: 6290 write-cycle requirements.

Requirement		Guaranteed		Margin	Met
Symbol	Value	Expression	Value		(Y/N)
t_{DVCL}	30	$2t_{CLCL}$ - t_{CLRL}(max) - t_{RVD}(max)	400 - 165 - 60 = 175	145	Y
t_{CLDX}	10	t_{CLRH}(min) +t_{HZ}(min)	10 + 0 = 10	0	Y

Table 3: 8088 read-cycle requirements.

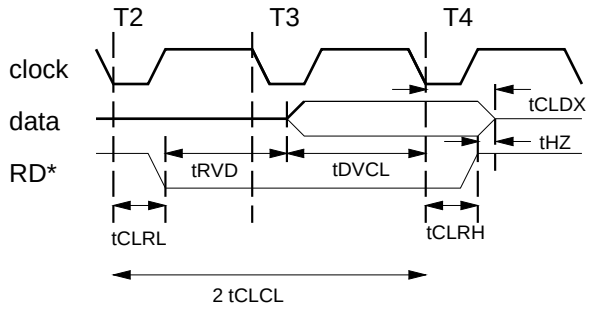

Figure 1: Derivation of guaranteed setup and hold times from delays relative to RD*.

and apply to both read and write cycles. All are requirements since they are minimum delays between signal edges on inputs.

In this design CS is generated by the address decoder. The decoder has a maximum propagation delay of 15 ns (labeled as t_{PD} in the tables) which causes CS to become active a maximum of t_{PD} after the address signals become valid. The following table describes the meanings of the delays and the edge to or from which the delay is measured.

symbol	meaning	ADS* inactive to/from
t_{ADS}	address strobe width	from start of ADS*
t_{AH}	address hold	to address invalid
t_{AS}	address setup	from address valid
t_{CH}	CS hold	to CS invalid
t_{CS}	CS setup	from CS valid

Table **??** shows how the margin is computed for each requirement. As before, the clock low time is assumed to be 66 ns and the high time 133 ns. RC and WC are cycle times and will be the same as the 8088 read and write cycle times (4 bus states for an 8088).

Read Cycle Requirements

Most of the 16550 read cycle requirements are measured between a signal edge and the rising (trailing) edge of the RD* strobe. However, most 8088 guaranteed responses are given with respect to clock edges rather than the RD* output.

For example, the 8088 specifications do not specify a minimum delay between address valid and the falling edge of the RD* strobe, but they do specify that the address will be valid a maximum of 110 ns after the start of T1 (t_{CLAV}) and that RD* will go active (low) a minimum of 10 ns after the start of T2 (t_{CLRL}). From these two guaranteed responses and the fact that the time from the start of T1 to the start of T2 is exactly one clock cycle (t_{CLCL}) we can infer that the minimum time from address valid to the start of the RD* strobe is:

$$t_{CLCL} - t_{CLAV}(\text{max}) + t_{CLRL}(\text{min}).$$

Similarly, there is no 8088 guaranteed response for the minimum delay between the end of the RD* strobe and when the address becomes invalid. However the address will not change until ALE goes high in the next bus cycle (after the start of the next T1) so we can derive the minimum time from the rising edge of RD* to the address invalid as:

$$t_{CLCL} - t_{CLRH}(\text{max}) + t_{CLLH}(\text{min}).$$

Unfortunately, t_{CLLH}(min) is not given, but it's reasonable to assume that ALE will not be asserted before the start of the next T1 and so we can safely assume t_{CLLH}(min) is at least 0.

Note that you can't use t_{RHAV} for this purpose because the address input to the 16550 comes from the address latch, not from the 8088's multiplexed address outputs (after T1 the multiplexed data/address pins contain data rather than address values).

The read cycle requirements and the signal edge to/from which the delays are measured are:

symbol	requirement	RD* inactive to/from
t_{AR}	address setup	from address valid
t_{CSR}	CS setup	from CS valid
t_{RA}	address hold	to address invalid
t_{RCS}	CS hold	to CS invalid
t_{RD}	read strobe width	from start of RD*
t_{RC}	read recovery time	to ADS* active

The margins for these requirements are computed in Table **??**.

Note that the minimum read cycle strobe width (t_{RD}) could also have been derived by subtracting t_{CLRL}(max) and t_{CLRH}(min) from $2t_{CLCL}$ giving a minimum value of 400 - 165 - 10 = 225 ns. Although this value is correct in the sense that it is also a guaranteed response, it is more pessimistic than the value guaranteed by the manufacturer (t_{RLRH}=325 ns). It would be a mistake to use the more pessimistic (derived) value because it might cause you to overdesign your circuit. For example, you might decide to add a wait state on each access to the chip even though it's not really required.

Write Cycle Requirements

The following setup and hold time requirements apply to write cycles and are measured between a signal edge and the rising (trailing) edge of the WR* strobe:

symbol	requirement	WR* inactive to/from
t_{AW}	address setup	from address valid
t_{CSW}	CS setup	from CS valid
t_{WA}	address hold	to address invalid
t_{WCS}	CS hold	to CS invalid
t_{WR}	write strobe width	from start of WR*
t_{DS}	data setup	from data valid
t_{DH}	data hold	to data invalid
t_{WC}	write recovery time	to ADS* active

The margins for these requirements are computed in Table **??**. The first four requirements are computed in a similar fashion, using t_{CVCTX} instead of t_{CLRH}.

Requirement		Guaranteed		Margin	Met
Symbol	Value	Expression	Value		(Y/N)
t_{ADS}	60	t_{LHLL}	133-20 = 113	53	Y
t_{AH}	0	t_{LLAX}	133-10 = 123	123	Y
t_{AS}	60	t_{AVAL}	133-60 = 73	13	Y
t_{CH}	0	t_{LLAX}-t_{PD}	133-10-15 = 118	118	Y
t_{CS}	60	t_{AVAL}-t_{PD}	133-60-15 = 58	-2	N
RC	280	4*t_{CLCL}	800 = 800	520	Y
WC	280	4*t_{CLCL}	800 = 800	520	Y

Table 4: 16550 read- and write-cycle requirements.

Requirement		Guaranteed		Margin	Met
Symbol	Value	Expression	Value		(Y/N)
t_{AR}	30	t_{CLCL} - t_{CLAV}(max) + t_{CLRL}(min)	200 - 110 + 10 = 100	70	Y
t_{CSR}	30	t_{CLCL} - t_{CLAV}(max) + t_{CLRL}(min) - t_{PD}	200 - 110 + 10 - 15 = 85	55	Y
t_{RA}	20	t_{CLCL} - t_{CLRH}(max) + t_{CLLH}(min)	200 - 150 + 0 = 50	30	Y
t_{RCS}	20	t_{CLCL} - t_{CLRH}(max) + t_{CLLH}(min) - t_{PD}	200 - 150 + 0 - 15 = 35	15	Y
t_{RD}	125	t_{RLRH}	400-75 = 325	200	Y
t_{RC}	125	t_{CLCL} - t_{CLRH}(max) + t_{CLLH}(min)	200 - 150 + 0 = 50	-75	N

Table 5: 16550 read-cycle requirements.

Requirement		Guaranteed		Margin	Met
Symbol	Value	Expression	Value		(Y/N)
t_{AW}	30	t_{CLCL} - t_{CLAV}(max) + t_{CVCTV}(min)	200 - 110 + 10 = 100	70	Y
t_{CSW}	30	t_{CLCL} - t_{CLAV}(max) + t_{CVCTV}(min) - t_{PD}	200 - 110 + 10 - 15 = 85	55	Y
t_{WA}	20	t_{CLCL} - t_{CVCTX}(max) + t_{CLLH}(min)	200 - 110 + 0 = 90	70	Y
t_{WCS}	20	t_{CLCL} - t_{CVCTX}(max) + t_{CLLH}(min) - t_{PD}	200 - 110 + 0 - 15 = 75	55	Y
t_{WR}	100	t_{WLWH}	400-60 = 340	240	Y
t_{DS}	30	2t_{CLCL} - t_{CLDV}(max) + t_{CVCTX}(min)	400 - 110 + 10 = 300	270	Y
t_{DH}	30	t_{WHDX}	133-30 = 103	73	Y
t_{WC}	150	t_{CLCL} - t_{CVCTX}(max) + t_{CLLH}(min)	200 - 110 + 0 = 90	-60	N

Table 6: 16550 write-cycle requirements.

Requirements on Unused Signals

t_{MR}	master reset pulse width
t_{XH}	clock high pulse width
t_{XL}	clock low pulse width

The following specifications are requirements (all are minimum delays between two input edges), but the signals are not used in this design so it's not necessary to check whether these requirements are met.

Guaranteed Responses

The following specifications are are maximum delays between an input and an output on the 16550 so

they are guaranteed responses, not requirements.

t_{RDD}	from RD* edge to DDIS valid
t_{RVD}	from RD* active to valid data
t_{HZ}	from RD* inactive to data bus tri-state