Solutions to Mid-Term Exam

Question 1

Requirement		Guaranteed		Margin	Met
Symbol	Val.	Expr.	Val.		
8051 Read Cycle Requirements					
t_{LLDV}	517	t_{AA}	35	482	Y
t_{AVDV}	585	t_{ACS}	25	560	Y
t_{RLDV}	250	t_{AOS}	25	225	Y
t_{RHDZ}	97	t_{ZROS}	30	67	Y

Question 2

State Variables	ALE	Next State
000	0	001
001	0	010
010	0	011
011	0	100
100	0	100
XXX	1	000

State Variables	READY
000	H
001	L
010	H
011	H
100	H

Note that since the state machine changes state on the rising edge of the clock it's changes of state lag those of the CPU by one-half clock cycle.

The assignment of values to the states is arbitrary as long as the controller cycles through 5 states and the READY is low in the state after the state in which ALE was high.

Question 3

To get 32 kBytes total using 8kB by 8 RAMs requires 4 chips.

Two RAMs need to be connected in parallel in order to interface to the 16-bit wide data bus. The CPU's D0 to D7 will connect to one RAM's D0 to D7 and the CPU's D8 to D15 will connect to the other RAM's D0 to D7.

Since the CPU has byte addressing it must use A0 internally to select between the two bytes on the 16 bit data bus. To select from one of the 8k bytes in each RAM, the CPU's A1 to A13 address outputs must connect to each RAM's A0 to A12 address inputs.

The address decoder must therfore decode the CPU's A14 to A23 and generate two chip-selects, CS0 and CS1 (one for each 16-bit-wide bank).