THE UNIVERSITY OF BRITISH COLUMBIA
DEPARTMENT OF ELECTRICAL ENGINEERING
ELEC 464 : Microcomputer System Design (Fall 1996)

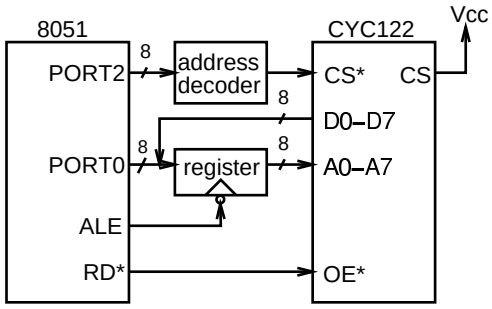
MID-TERM EXAMINATION

10:30 am – 11:20 am
October 29, 1996

This exam has three (3) questions. The marks for each question are as indicated. There are a total of 35 marks. Answer all questions. You may answer the questions in any order. Books, notes and calculators are allowed. You may keep this exam paper.

Question 1 (11 marks)

Partial data sheets for a AMD 8051 microcontroller and a Cypress 256x8 RAM are given in an Appendix. These two devices are connected using the circuit shown below:



The 8051 has a 16-bit address bus and an 8-bit data bus.

The least significant 8 bits of the address are multiplexed with the data bus in the same way as on the 8088. The 8 least significant address bits are output from "Port 0" and are loaded into an 8-bit register on the *falling edge* of the ALE signal. You may assume there is zero propagation delay from the falling edge of ALE until the address appears on the output of the register. The output of the register then drives the address inputs of the RAM.

The most significant 8 bits of the address are output from "Port 2" and drive an address decoder which in turn drives the RAM's active-low chip select, CS*. You may assume the address decoder has zero propagation delay. The RAM's active-high chip select input, CS, is always enabled and thus you may ignore it.

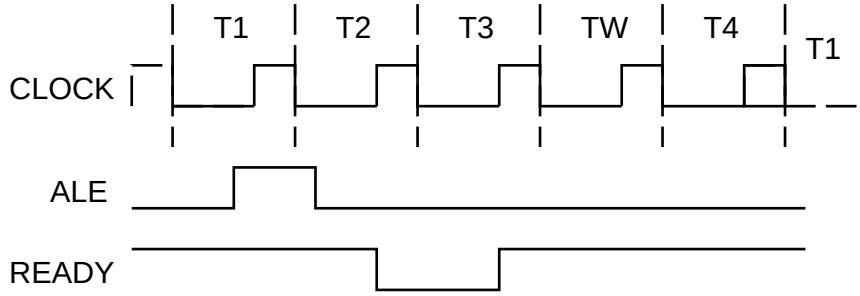
The arrangement described above means that the address inputs to the chip become valid on the falling edge of ALE and the chip select input to the chip becomes when the address becomes valid.

The table below shows four 8051 read-cycle timing requirements that need to be met for the system to operate properly. Obtain expressions for these requirements in terms of the symbols for the timing specifications given in the data sheets. Obtain values for these expressions in nanoseconds. Find the amount by which the requirement is exceeded (in nanoseconds) and state whether the requirement is met or not (Y[es] or N[o]). Give your answer in the form of a table as shown below.

Requirement		Guaranteed		Margin	Met
Symbol	Value	Expression	Value		(Y/N)
8051 Read Cycle Requirements					
t_{LLDV}	517				
t_{AVDV}	585				
t_{RLDV}	250				
t_{RHDZ}	97				

Question 2 (12 marks)

Design a wait-state generator that forces the 8088 CPU to insert one wait state, TW, between states T3 and T4 in the 8088 CPU bus cycle. Your circuit must do this by de-asserting the CPU's READY input on the rising edge of the clock in T2 and then re-asserting READY on the rising edge of the clock in T3 as shown in the following diagram:



Driving the CPU's READY input in this way will cause the CPU to add a wait state and cycle through states T1, T2, T3, TW and T4.

Your circuit will have an ALE (address latch enable) input, a READY (ready) output, and a CLK (clock) input. Your circuit should be a Moore state machine whose state and outputs will change only on the rising edge of the clock. If ALE is asserted on the rising edge of the clock your circuit should assume the CPU is in state T1. If the CPU is in state T4 and ALE is not asserted the circuit should assume that the CPU remains in state T4.

Choose an appropriate number of state variables and the encoding for the state variables and describe the state transition behaviour of the state machine in the form of a table as shown below. The table should have three columns: (1) the values of the state variables for the current state, (2) the value of the ALE input, (3) the values of the state variables for the next state. You may use the value 'X' to indicate a "don't care" value.

State Variables	ALE	Next State

Also give the value of the READY output for each state in the form of a table as shown below.

State Variables	READY

Question 3 (12 marks)

Design a memory system for a Motorola 68000 CPU. This CPU has a 24-bit address bus and a 16-bit data bus. The memory system must contain a total of 32 kBytes of RAM and is to be built using 8k by 8 RAM chips. Assume the processor always accesses 16 bits in parallel although the CPU addresses are the addresses of bytes.

Draw a block diagram showing how the CPU's address and data bus pins connect to the RAM chips' address and data pins. Label the CPU address lines as A23 to A1 and the CPU data lines as D15 to D0. Label the RAM address lines as A12 to A0 and the RAM data lines as Q7 to Q0. You may use the bus notation as described in Assignment 5 (e.g. A[23:20]) to label buses.

Label a pin on each RAM as an active-high chip select line, CS. Add to the diagram a box representing an address decoder with CPU address lines as inputs and chip select signals labeled CS0, CS1, ... as outputs. The address decoder will fully decode memory addresses. Show the *minimum* set of CPU address bus signals which must be connected to the decoder and the *minimum* number of required chip select outputs. Show how these chip select signals are connected to the RAM chips. You need not show the internal details of the address decoder.

The connections in your diagram should be unambiguous. *Hint: use a whole sheet of paper for the diagram and leave plenty of room to draw the connections.*