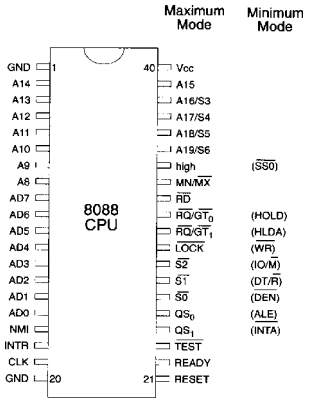
The 8088 Processor Bus

This lecture describes the Intel 8088 processor bus and its read and write cycles.
After this lecture you should be able to state the values of the processor bus signals described below during memory or I/O read and write cycles.

1 8088 CPU Signals



Utility Bus

The two most important pins on the CPU chip are for power supply and ground. Without a clean power supply of the proper voltage the processor will operate erratically or not at all.

The next most important signal is the clock, CLK. Many 8088 systems use an 8284 clock generator chip which includes a crystal-controlled oscillator that generates the required clock signal with a 33% duty cycle and also synchronizes the READY input (see below) to the correct clock edges.

The 8088 can be configured to operate in two different modes depending on the level of a MiN/MaX* input. The minimum mode is designed for simple systems that don't require detailed CPU state information. The maximum mode is used with an 8288 bus controller and allows multiple CPUs to share the same bus.

Reset and Interrupts

The RESET input resets the processor state to a starting state in which IP and all segment registers except CS are set to 0 and CS is set to 0FFFFH. This means the first instruction the processor executes is at address 0FFFF0H.

The NMI and IRQ inputs are used to generate non-maskable and maskable interrupts respectively.

Asserting the NMI input causes the processor to execute the interrupt handler pointed to by the interrupt vector at memory location 8 (interrupt number 2).

If interrupts are enabled then asserting IRQ causes the CPU to carry out an interrupt acknowledge bus cycle which reads an interrupt number from the bus (typically from the interrupt controller chip). The corresponding interrupt vector is then fetched and the corresponding interrupt handler executed as with NMI.

In either case the current instruction is finished before the interrupt is recognized.

Bus Control

If the READY input is de-asserted (brought low) early enough during a bus cycle the 8088 will insert *wait states* (TW) between states T3 and T4 (see below).

The ALE output is used to control the external device that demultiplexes the address and data buses (see below).

The RD*, INTA*, and WR* signals indicate the type of bus cycle being executed (read, interrupt acknowledge or write).

In minimum mode the chip control signals such as IO/M*, RD*, WR* and ALE are used directly. When the CPU is set up for maximum mode these pins provide the CPU state to an external 8288 bus controller chip which decodes the CPU state and generates slightly different control signals.

Address and Data Busses

The 8088 has an 8-bit data bus and a 20-bit address bus. However, the least significant 8 address and data bus signals (AD0 to AD7) are multiplexed. During

the first bus cycle (T1) of an instruction the address is placed on all 20 address/data pins. This address must be *latched* by an external 8-bit transparent latch such as a 74LS373.

The IO/M* signal is used to distinguish between accesses to memory and I/O spaces.

The CPU's ALE (address latch enable) signal is used to control the latch and hold the address after the first bus cycle.

This multiplexing of the address/data buses (and the off-loading of other various functions to external chips such as the 8284 and 8288) allowed the 8088 to be packaged in a 40-pin chip.

2 8088 Bus Cycles

Execution of each 8088 instruction requires one or more *bus cycles*. In a read or write bus cycle a byte is transferred between the CPU and memory or an I/O peripheral. In an interrupt acknowledge bus cycle an interrupt number is read, typically from an interrupt controller chip.

Each bus cycle requires at least 4 *clock cycles*, labeled T1 to T4. Additional clock cycles (*wait states*, labeled TW) can be inserted between T3 and T4. During these clock cycles the CPU is idle. Wait states are used to increase setup and/or hold times for slow memory or peripherals.

Details concerning timing will be covered later in the course.

Read and Write Cycles

Shortly after the start of T1 the address bus (including IO/M*) is set to the correct value. Before the end of T1 ALE is brought low to latch the address on the multiplexed data/address bus.

During T2 data is placed on the data bus by the CPU during a write cycle (i.e. when WR* is asserted) or the memory/peripheral during a read cycle (when RD* is asserted).

State T3 extends the bus cycle to permit longer memory access times during reads and results in longer setup times during writes.

During T4 RD* or WR* are de-asserted and the data on the data bus is latched into memory or the CPU.

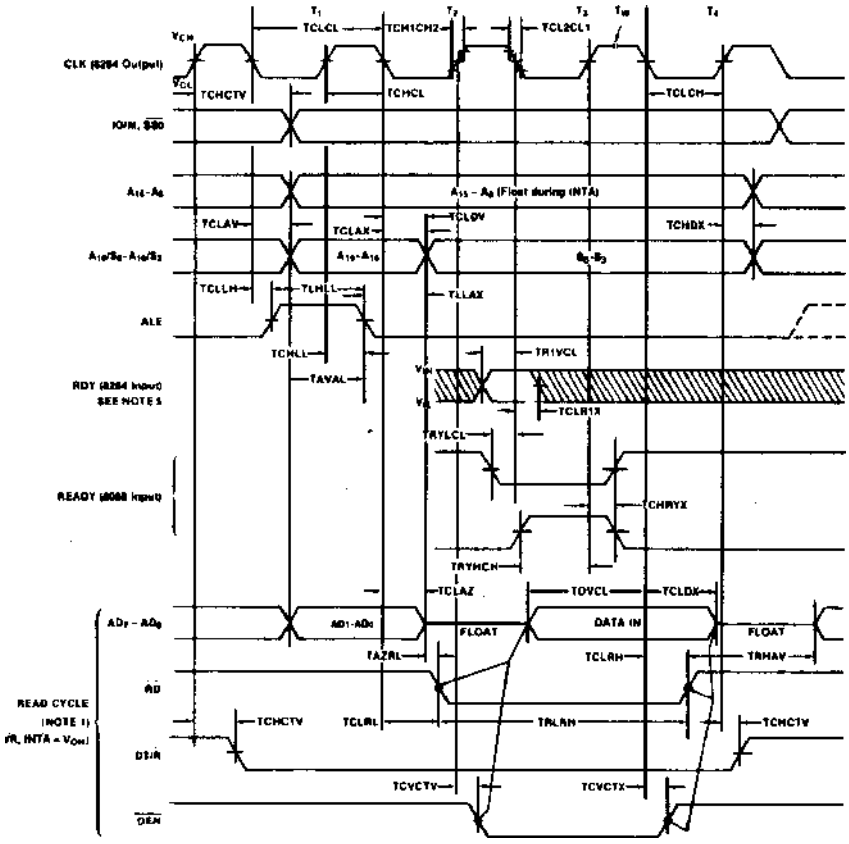
The only difference between memory and I/O read/write cycles is that the IO/M* signal is low during I/O cycles.

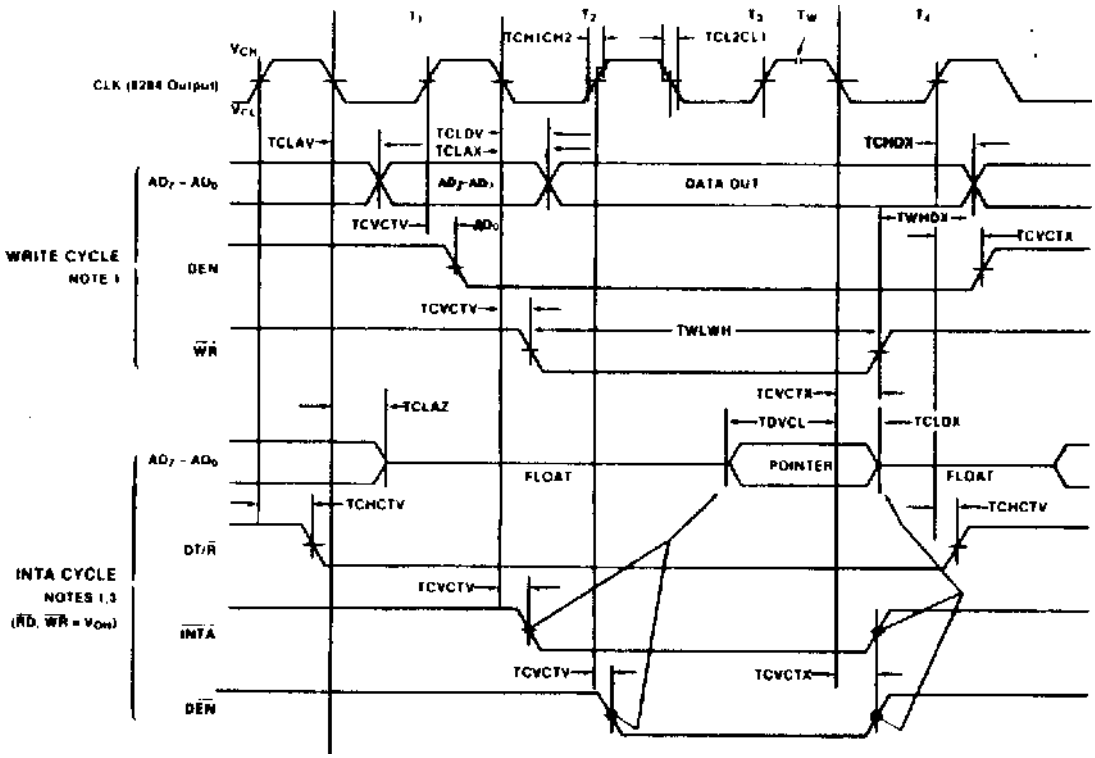
Interrupt Acknowledge Cycle

An interrupt acknowledge cycle is the same as a read cycle except that the address bus is not asserted (it floats) and INTA* is asserted instead of RD*.

Wait States

If the RDY signal is set low before the end of T2 then wait states, TW, are inserted after T3. Wait states will continue to be inserted until RDY is brought high before the middle of T3 or TW. The RDY line is typically synchronized to the clock by the 8284 clock generator.


READ CYCLE
(NOTE 1)
(IR, INTA = VOH)
CLK (8284 Output)
IO/M, SSO
RDY (8284 Input)
SEE NOTES
READY (8088 Input)
ALE
RD
DT/R
DEN
FLOAT
DATA IN
TCLCL
TCHCTV
TCHCL
TCLCH
TCLAV
TCLAX
TCLDV
TCHDX
TCLLH
TLHLL
TLLAX
TCHLL
TAVAL
TR1VCL
TCLR1X
TRYLCL
TCHRYX
TRYHCH
TCLAZ
TDVCL
TCLDX
TAZRL
TCLRH
TRHAV
TCLRL
TRLRH
TCVCTV
TCVCTX


WRITE CYCLE
NOTE 1
INTA CYCLE
NOTES 1,3
(RD, WR = VOH)
CLK (8284 Output)
DEN
WR
DT/R
INTA
TCH1CH2
TCL2CL1
TCLDV
TCLAX
TCLAV
TCHDX
DATA OUT
TWHDX
TCVCTV
TCVCTX
TWLWH
TCLAZ
TDVCL
TCLDX
POINTER
FLOAT
TCHCTV