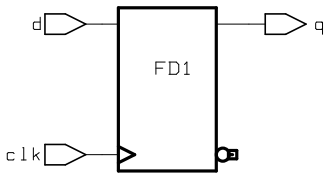
Sequential Logic Design
Synthesized Schematics

This page shows the corrected VHDL descriptions and synthesized schematics for the D flip-flop and 2-bit counter.

D Flip-Flop

```
entity D_FF is
   port ( clk, d : in bit ;
   q : out bit ) ;
end D_FF ;

architecture rtl of D_FF is
begin
process(clk)
begin
   if clk'event and clk = '1' then
      q <= d ;
   end if ;
end process ;
end rtl ;
```



2-bit Counter

```
entity count2 is
   port ( clk : in bit ; count :
      out bit_vector (1 downto 0) ) ;
end count2 ;

architecture rtl of count2 is
   signal current, nexts :
      bit_vector (1 downto 0) ;
begin

   -- combinational logic:
   process(current)
   begin
     -- compute next state and output
     -- from current state and input
     case current is
        when "00" =>
           nexts <= "01" ;
           count <= "00" ;
        when "01" =>
           nexts <= "10" ;
           count <= "01" ;
        when "10" =>
           nexts <= "11" ;
           count <= "10" ;
        when "11" =>
           nexts <= "00" ;
           count <= "11" ;
        end case ;
   end process ;

   -- sequential logic
   process(clk)
   begin
      if clk'event and clk = '
         current <= nexts ;
      end if ;
   end process ;

end rtl ;
```