Exam Review

This lecture summarizes the tasks that were you might be asked to do on the exam and provides examples of possible questions. It includes only those topics covered since the mid-term exam although the final exam will cover all of the material in the course.

Direct Memory Access (DMA)

You should be able to: identify the advantages and disadvantages of using DMA and programmed I/O, select the most appropriate method for a particular application, and describe the sequence of events that takes place during a DMA transfer on the IBM PC.

Exercise: A peripheral transfers 512 bytes to memory using cycle-stealing DMA on an IBM PC-compatible computer. How many times will the CPU's hold-request (HRQ) pin be asserted? How many times will DREQn* be asserted? Will IOW* (I/O write) or IOR* (I/O read) be asserted during the transfers?

Dynamic RAM

You should be able to: (1) describe basic DRAM structure and terminology, (2) interface DRAMs to a CPU bus by multiplexing row and column address lines and forcing refresh cycles, and (3) justify the choice of DRAM or SRAM for a particular application.

Exercise: Would DRAM be a good choice of memory technology for a programmable calculator containing a total of 4 kB of memory? Why or why not?

Every 10 ms a DRAM controller asserts CAS* and then strobes RAS* 1024 times. What type of operation is being performed? If the DRAM's minimum refresh time is specified as 10 ms and the memory arrays are square, how many bits are in each memory array?

Parallel I/O Ports

You should be able to: (1) design simple input, output and bidirectional I/O ports using registers, tri-state buffers and and open-collector buffers; and (2) write 8088 assembly language programs to read and write the individual bits of an I/O port.

Exercise: A peripheral chip whose function is not relevant to this question is to be interfaced to a CPU bus. The chip has a single internal 8-bit write-only register accessed through eight input pins (D0 to D7) and an active-low load strobe (WR*). The chip has a one-bit output (DONE) that is to be readable by the CPU as bit 7.

Assume the CPU bus has the following signals available: an 8-bit bi-directional data bus (DB0 to DB7), a read/write signal (R/W*), and an active-low chip-select signal (CS*) from an address decoder that is asserted when the chip's address is on the address bus.

During a read cycle the CPU expects the data to be valid at some undefined point when R/W* is high. During a write cycle the data on the CPU bus is latched on the rising edge of R/W*. SEL* goes valid before and after the rising edge of R/W*.

Draw a schematic of an interface between an 8-bit CPU bus and this chip that uses only combinational logic gates and tri-state buffers with active-low output-enables in your design.

Serial/Printer/SCSI Interfaces

You should be able to describe the operation and format of data and handshaking signals on an RS-232 interface and the data format on an HDLC synchronous data stream.

You should be able to to be able to write programs to transfer data over a "Centronics" parallel printer interface

You should be able to list some advantages and disadvantages of the SCSI interface and give the values of the signals on the SCSI bus during the various bus phases.

Exercise: An PC reads a 4-byte "sector" from a disk drive with SCSI ID 5 over the SCSI bus. The 6-byte command parameter block is: 08 00 00 00 01 00. The sector contents are: 34 78 55 12. The status code is 00.

List the (logical) values of SEL*, BSY*, DB0*-DB7*, C*/D and I*/O during the transfer during all 4 bus phases. Give your answer in the form of a table with one line for each combination of the above signals. Give the state of the control bus signals as true (T), false (F) or undefined (X) and the data bus signals in hex (all signals are asserted when low). Start and end the table in the bus free state, for example:

SEL	BSY	data	C*/D	I*/O
F	F	X	X	X
F	F	X	X	X