Solutions To Final Exam

Question 1

(a) State Machine Design

The state variable encoding below is the binary representation of the number of consecutive '1's "seen" by the circuit so far. Only six states are required so three variables (a,b,c) are sufficient. A one-hot encoding using six state variables would also be suitable. The table below does not show states that would not be encountered in normal operation.

State Variables			Input	Next State		
a	b	c	din	a	b	c
X	X	X	0	0	0	0
0	0	0	1	0	0	1
0	0	1	1	0	1	0
0	1	0	1	0	1	1
0	1	1	1	1	0	0
1	0	0	1	1	0	1
1	0	1	1	0	0	0

The outputs are zero for all states except the state where five '1's have been "seen" (and therefore the next bit is a stuffed bit).

State Variables			Output
a	b	c	valid
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0

(b) VHDL Code

```
entity unstuff is
   port ( data, clk : in  bit ;
          valid : out bit ) ;
end unstuff ;

architecture rtl of unstuff is
   signal state, nexts : bit_vector (2 downto 0) ;
begin

   -- compute next state
   process(state,data)
   begin
      if data = '0' then
         nexts <= "000" ;
      else
         case state is
            when "000" => nexts <= "001" ;
            when "001" => nexts <= "010" ;
            when "010" => nexts <= "011" ;
            when "011" => nexts <= "100" ;
            when "100" => nexts <= "101" ;
            when "101" => nexts <= "000" ;
            when others => nexts <= "000" ;
         end case ;
      end if ;
   end process ;

   -- latch state on rising clock edge
   process(clk,nexts)
   begin
      if clk'event and clk='1' then
         state <= nexts ;
      end if ;
   end process ;

   -- output
   process(state)
   begin
      if state = "101" then
         valid <= '0' ;
      else
         valid <= '1' ;
      end if ;
   end process ;

end rtl ;
```

Question 2

The table showing the expression and values for the SRAM write cycle timing margins is shown in Table 1. All times in nanoseconds.

Question 3

A schematic of the answer is shown in Figure 1.

Requirement			Guaranteed		Margin	Met
Parameter	Symbol	Min.	Expression	Value		(Y/N)
Write Cycle Requirements						
Write Cycle	t_{WC}	250	t_{cyc}	500	250	Y
Address Setup	t_{AS}	0	t_{AQ}	15	15	Y
Address Hold	t_{AH}	80	t_{cyc} - t_{AVS}(max) + t_{AH}	500 - 125 + 20	315	Y
Data to Write Setup	t_{DSW}	20	t_{cyc} - t_{AVS}(max) - t_{DDQ}(max)	500 - 125 - 110	245	Y
Data from Write Hold	t_{DHW}	10	t_{DHW}	30	20	Y
Write Pulse Duration	t_{WD}	70	t_{cyc} - t_{AVS}(max)	500 - 125	305	Y

Table 1: Answers to Question 2.

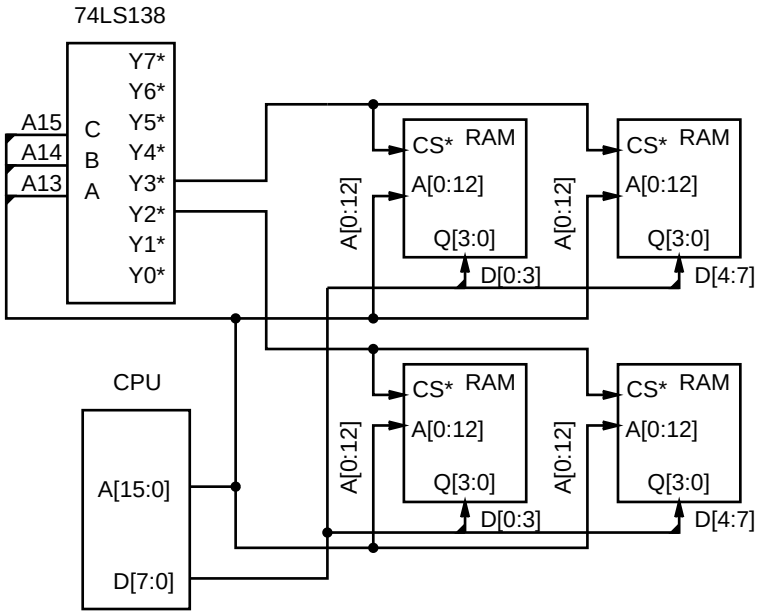

Figure 1: Answer to Question 3.

Question 4

```
;
; ELEC 464 Final Exam, Question 4
; output string to 8250 serial port
; Ed Casas, 96/12/19
;
code    segment public
        assume  cs:code,ds:code
start:  org     100h

; beginning of answer

   mov   bx,offset msg
loop1:
   mov   al,[bx]  ; next character
   cmp   al,00H   ; end of string?
   jz    done
   mov   tmp,al   ; save temporarily
   mov   dx,03FEH ; status register
loop2:
   in    al,dx
   and   al,20H   ; test TBE bit
   jz    loop2    ; wait 'til empty
   mov   al,tmp   ; restore character
   mov   dx,03F8H ; data register
   out   dx,al
   inc   bx       ; next character
   jmp   loop1
done:
   int   20H      ; return to DOS

; end of answer

; the message to print

msg     db     'Hello, world',0
tmp     db      ?

code    ends
        end     start
```