Assignment 5

Due October 21, 1996

This assignment asks you to design two memory systems including address decoding.

Question 1

Draw the schematic of a 128 kByte RAM memory system for an 8-bit CPU using 64k by 2 devices. Assume the CPU has a 24-bit address bus (A0 to A23), an 8-bit data bus (D0 to D7), and RD* and WR* read/write signals. Each memory chip has two bi-directional data pins (Q0 and Q1), address inputs (A0, A1, ...), an active-high chip-select signal (CS) and an active-low write strobe (W*). The RAM's CS inputs should be driven by an address decoding circuit and W* should be driven from the CPU's WR* signal. Show all connections between the CPU, the address decoder and the memory chips. The internal details of the address decoder need not be shown.

You may use the bus notation X[n:m] to indicate a subset of the signals of X consisting of bits n through m. For example, the following diagram shows that D2 connects to Q6 and D3 connects to Q7:

Question 2

Draw the schematic of a memory system using RAM and EPROM for a 16-bit CPU using two 128k by 8 SRAMs and two 32k by 8 EPROMs. Assume the CPU always accesses memory 16 bits at a time and has a 20-bit address bus (A1 to A19), a 16-bit data bus (D0 to D15) and RD* and WR* read/write signals. The CPU uses byte addressing. Each memory chip has eight bi-directional data in/out pins (Q0 to Q7), address inputs (A0, A1, ...) and an active-high chip-select signal (CS). The RAMs also have active-low write strobes (W*). The CS pins should be driven from an address decoding circuit and W* should be driven from the CPU's WR* signal. You may assume all memory chips' outputs are tri-stated when the CS is not asserted. Show all connections between the CPU and the memory chip pins. You may use the bus notation described above. The details of the address decoder need not be shown.

Question 3

Design two address decoders for each of the two circuits described above (a total of 4 designs). The first design should use an (optional) 8-input AND gate and a 3 to 8 decoder and the second should be a synthesizable circuit description in VHDL. The decoders for the first question should place the RAM starting at memory location 0. The decoders for the second question should place the RAM starting at memory location 0 and the EPROM at memory location F8000H. Both decoders should fully decode CPU addresses.

For the designs that use a 3 to 8 decoder draw a schematic showing how the inputs and outputs are connected to the address bus and to the memory chip's CS inputs. The 3-to-8 decoder also has an enable input (E) which must be asserted for any of the outputs to be asserted. Label the decoder inputs D0 to D2 (D0 being the LS input) and the outputs Q0 to Q7 (Q0 asserted when D0=D1=D2=0=L and Q7 asserted when D0=D1=D2=1=H).

For the VHDL-based designs write an entity and an architecture. Use a bit_vector-type input signal named A with an appropriate downto range and as many active-high bit-type output signals named CSn (n=0,1,...) as are required by your design. Use comments to describe the purpose of each chip select output. Synthesize the circuit using Synopsys Design Compiler and the 'class' target technology (not Xilinx FPGA). Hand in listings and plots of the synthesized schematics. Your schematics should not have flip-flops. You need not simulate your design.