Assignment 4

Due October 14, 1996

The first question in this assignment asks you to select the appropriate PLD for various tasks. The other two questions ask you to verify the timing requirements of two combinations of microprocessors and memory/peripheral chips.

Question 1

Select the type of PLD (PAL, CPLD or FPGA) that you would most likely use for each of the following purposes and briefly explain your choice.

1. A device to implement the following on the same chip: a keypad scanning circuit (a combinational circuit requiring 12 i/o pins), a multiplexed 4-digit LED display driver (a sequential circuit using a 40 kHz clock, 4-bit counter, 16 bits of display memory and 11 i/o pins), and a 100 kHz 24-bit timer with a 16-bit CPU bus interface and internal configuration registers (a sequential circuit with two state machines for control and 56 bits of state for registers).

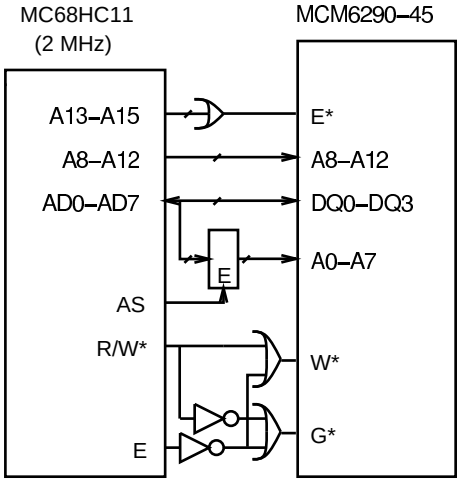
2. A wait-state generator requiring two enable signals and a 3-bit counter.

3. A mailbox circuit that allows a 16-bit value to be exchanged between two independent CPUs. This requires one 16-bit register and a simple (4 i/o pin) combinational circuit to coordinate accesses to the register.

4. An address decoder with 8 address inputs, 2 chip select outputs and a requirement for a 10 ns maximum propagation delay

Question 2

The following diagram shows the schematic of the interface between a Motorola MC68HC11 microprocessor and a Motorola MCM6290-45 16kB$\times$4 static RAM.



The RAM has an enable (E*) which is driven by an address decoder whose details are not relevant.

The 68HC11's address and data buses are multiplexed and a latch is used to demultiplex the address and data. The exact details are not relevant.

The RAM has write enable (W*) and output enable (G*) inputs. The two enables are driven by OR gates that ensure that W* is only enabled during a write cycle and G* is only enabled during a read cycle. The OR gates are also driven by the 68HC11's inverted E signal. This ensures these two enables are only active during the second half of a memory cycle – when E is high.

The timing diagram and timing specifications for the 68HC11 and are given in Figures **??** and **??**.

The timing diagram and timing specifications for the MCM6290-45 RAM are given below.

Assume that all the external logic devices (address decoder, latch, inverters and gates) have zero propagation delay. You should also assume that the rise and fall time (parameter 4) is zero.

The table below shows nine timing requirements that need to be met for the system to operate properly. Obtain expressions for these requirements in terms of the symbols for the timing specifications given in the

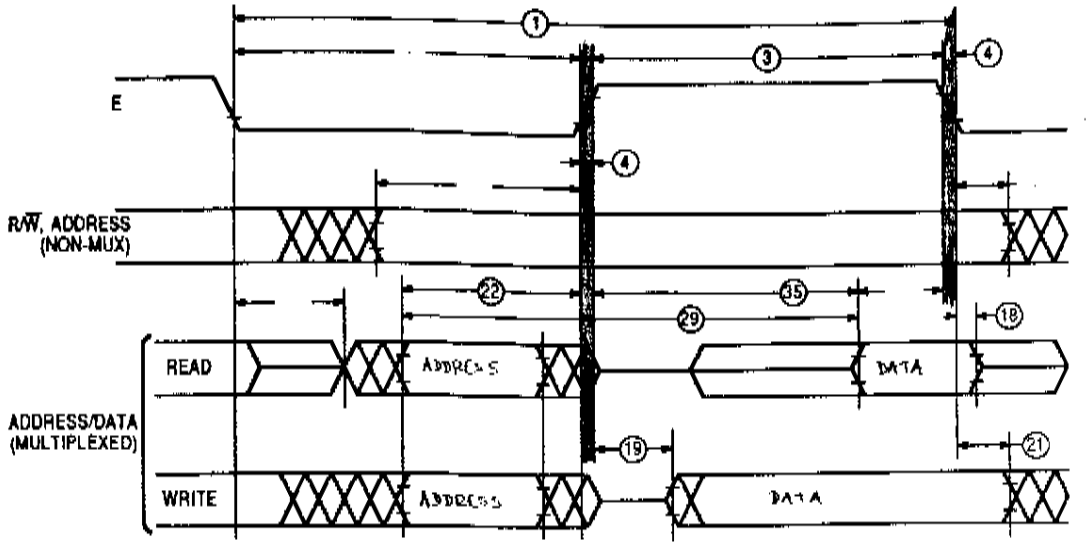


Figure 1: 68HC11 Timing Diagram.

No.	Characteristic	Symbol	Min	Max	Unit
1	Cycle Time	t_{cyc}	500	500	ns
3	Pulse Width, E high	PW_{EH}	222	—	ns
18	Read Data Hold Time	t_{DHR}	10	83	ns
19	Write Data Delay Time	t_{DDW}	—	128	ns
21	Write Data Hold Time	t_{DHW}	33	—	ns
22	Muxed Address Valid Time to E Rise	t_{AVM}	84	—	ns
29	MPU Address Access Time	t_{ACCA}	—	296	ns
35	MPU Access Time	t_{ACCE}	—	192	ns

Figure 2: 68HC11 Timing Specifications.

data sheets. Obtain values for these expressions in nanoseconds. Find the amount by which the requirement is exceeded (in nanoseconds) and state whether the requirement is met or not (Y[es] or N[o]). Give your answer in the form of a table as shown below.

Iportant: Note that the first two requirements are maximum allowable access times and have been derived from the data setup time specification. All other requirements are minimums (setup times, pulse widths, hold times, etc).

Some specifications have been removed from the timing diagrams and tables.

Read Cycle

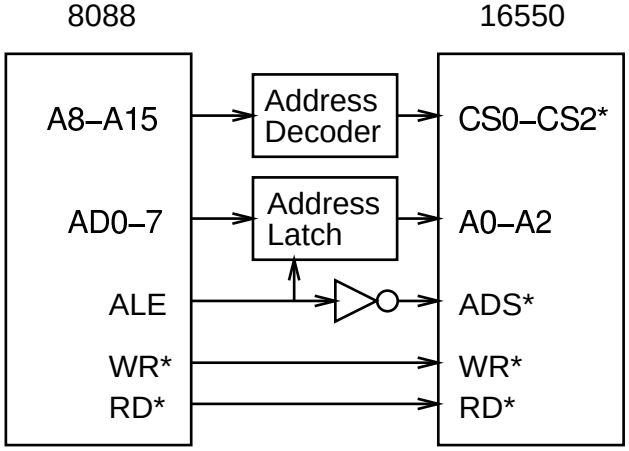
Requirement		Guaranteed		Margin	Met
Symbol	Value	Expression	Value		(Y/N)
MC68HC11 (2MHz) Requirements					
t_{ACCE} (35)	192				
t_{ACCA} (29)	296				
t_{DHR} (18)	10				
6290-45 Requirements					
t_{AVAV}	45				

Write Cycle

Requirement		Guaranteed		Margin	Met
Symbol	Value	Expression	Value		(Y/N)
MCM6290-45 Requirements					
t_{AVWL}	0				
t_{AVWH}	35				
t_{WLWH}	35				
t_{DVWH}	20				
t_{WHDX}	0				

Question 3

Attached are the timing diagrams and timing specifications for a a National 16550 serial interface chip and the timing specifications for an Oki 8088 CPU in minimum mode. The timing diagram for the 8088 was provided in the lecture on the 8088 processor bus. All times are in nanoseconds. The devices are connected as follows:



As in the previous question, you must determine if the above circuit will operate reliably by computing the margins for the timing requirements of both devices during both read and write cycles.

Prepare tables similar to those in the previous question that show the relevant timing requirements, the equations for each requirement in terms of the other device's guaranteed responses, the margin for each requirement and whether that requirement is met or not.

In this case *you* must decide which of the specifications are requirements and also which ones are relevant for read or write cycles.

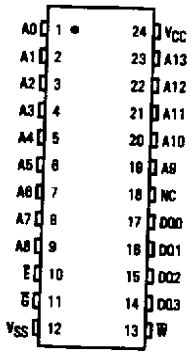
You may assume that:

- the CPU is a 5 MHz device and the CPU clock frequency is exactly 5 MHz
- the propagation delay through the address decoder, T_{PD} is a maximum of 15 ns
- there is no propagation delay through the address latch and you need not verify that its setup and hold time requirements will be met
- wait states are not inserted (the READY lines are always asserted) and the CPU bus is never requested (HOLD is always false).

You will probably find it useful draw new timing diagrams that include only the relevant signals appearing at the two devices and at the address decoder.

PIN NAMES	
A0-A13 . . . . . Address Input	$\overline{E}$ . . . . . Chip Enable
DQ0-DQ3 . . Data Input/Output	NC . . . . . No Connection
$\overline{W}$ . . . . . Write Enable	V_{CC} . . . . +5 V Power Supply
$\overline{G}$ (MCM6290) . . Output Enable	V_{SS} . . . . . Ground

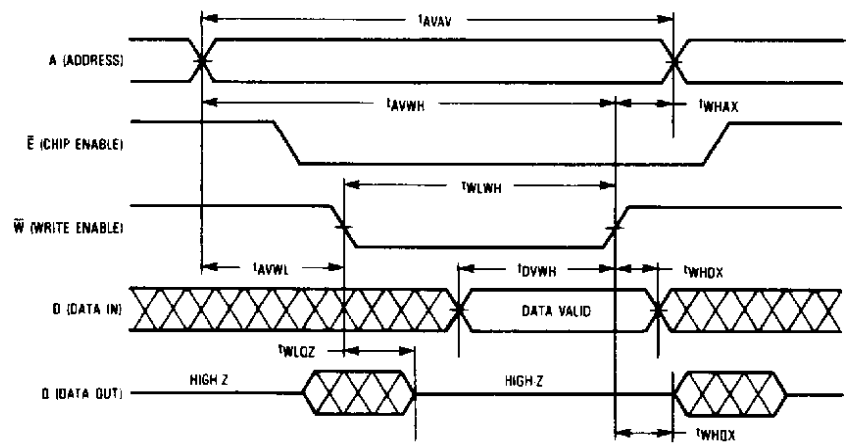
MCM6290



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 6)

Parameter	Symbol		MCM6288-25 MCM6290-25		MCM6288-30 MCM6290-30		MCM6288-35 MCM6290-35		MCM6288-45 MCM6290-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	–	30	–	35	–	45	–	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	–	25	–	30	–	35	–	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	20	–	25	–	30	–	35	–	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	–	12	–	15	–	20	–	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	0	–	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	10	0	12	0	15	0	15	ns	3,4,5,6
Write High to Output Active	t_{WHQX}	t_{OW}	5	–	5	–	5	–	5	–	ns	3,4,5
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	0	–	0	–	ns	

NOTES: 1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. Parameter is sampled and not 100% tested.
5. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.
6. MCM6290, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.



AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

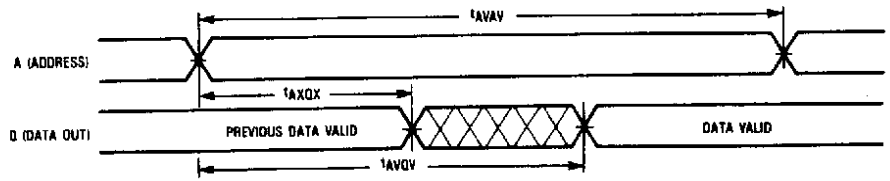
Output Timing Measurement Reference Level 1
Output Load . . . . . Figure 1A Unless Otherwise N

READ CYCLE (See Note 1)

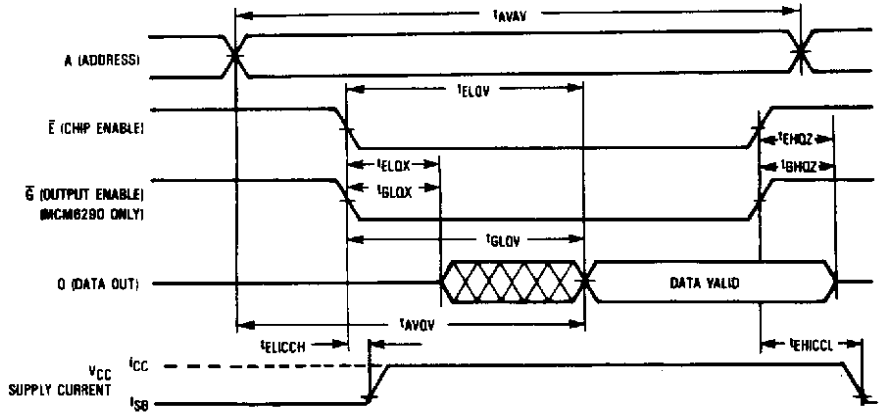
Parameter		Symbol		MCM6288-25 MCM6290-25		MCM6288-30 MCM6290-30		MCM6288-35 MCM6290-35		MCM6288-45 MCM6290-45		Unit	No
		Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time		t_{AVAV}	t_{RC}	25	–	30	–	35	–	45	–	ns	2
Address Access Time		t_{AVQV}	t_{AA}	–	25	–	30	–	35	–	45	ns	
Enable Access Time		t_{ELQV}	t_{ACS}	–	25	–	30	–	35	–	45	ns	3
Output Hold from Address Change		t_{AXQX}	t_{OH}	5	–	5	–	5	–	5	–	ns	
Output Enable Access Time	MCM6290	t_{GLQV}	t_{OE}	–	12	–	15	–	15	–	20	ns	
Output Enable Low to Output Active	MCM6290	t_{GLQX}	t_{LZ}	0	–	0	–	0	–	0	–	ns	4,5
Output Enable High to Output High-Z	MCM6290	t_{GHQZ}	t_{HZ}	0	10	0	12	0	15	0	15	ns	4,6
Enable Low to Output Active		t_{ELQX}	t_{LZ}	5	–	5	–	5	–	5	–	ns	4,5
Enable High to Output High-Z		t_{EHQZ}	t_{HZ}	0	10	0	12	0	15	0	15	ns	4,6
Power Up Time		t_{ELICCH}	t_{PU}	0	–	0	–	0	–	0	–	ns	
Power Down Time		t_{EHICCL}	t_{PD}	–	25	–	30	–	30	–	40	ns	

NOTES: 1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}) and $\overline{G}$ = V_{IL} (MCM6290 only).

READ CYCLE 1 (See Note 7 Above)

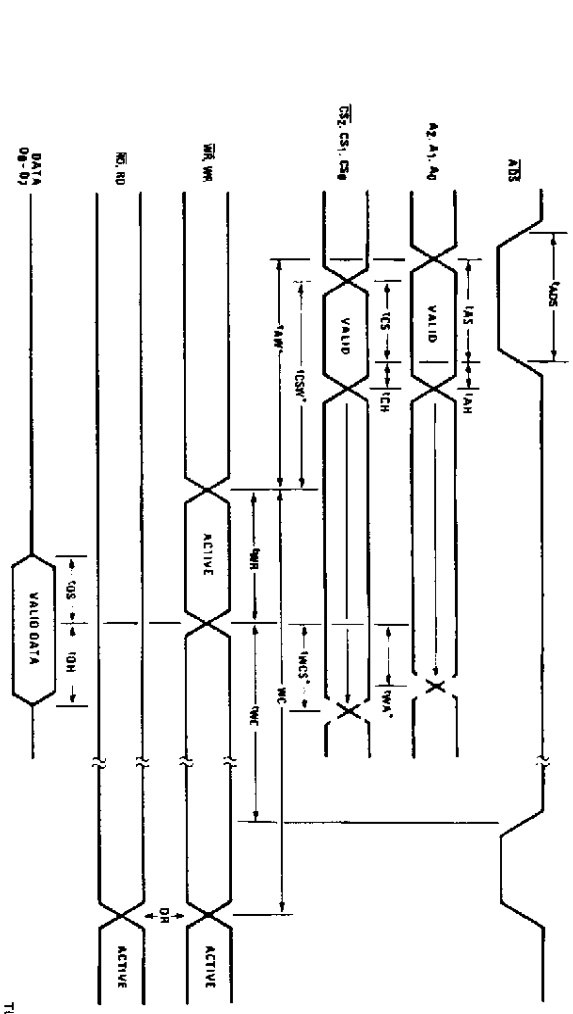


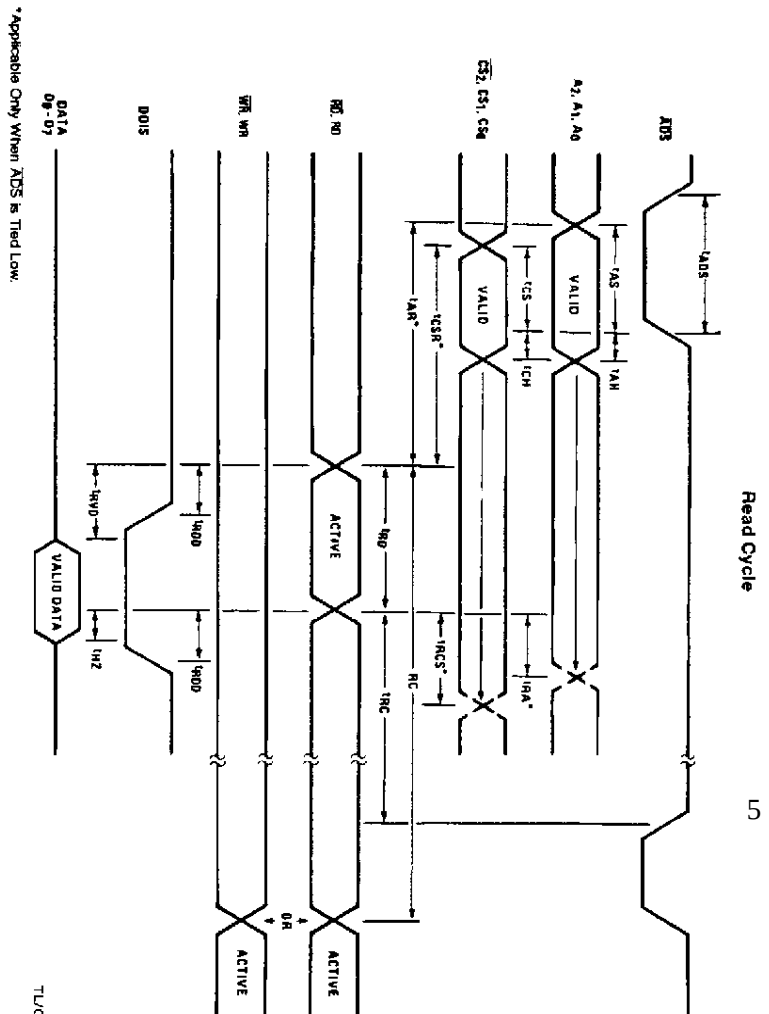
READ CYCLE 2 (See Note 3 Above)



3.0 AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$

Symbol	Parameter	Conditions	Min	Max	Units
t_{ADS}	Address Strobe Width		60		ns
t_{AH}	Address Hold Time		0		ns
t_{AR}	$\overline{RD}$, RD Delay from Address	(Note 1)	30		ns
t_{AS}	Address Setup Time		60		ns
t_{AW}	$\overline{WR}$, WR Delay from Address	(Note 1)	30		ns
t_{CH}	Chip Select Hold Time		0		ns
t_{CS}	Chip Select Setup Time		60		ns
t_{CSR}	$\overline{RD}$, RD Delay from Chip Select	(Note 1)	30		ns
t_{CSW}	$\overline{WR}$, WR Delay from Select	(Note 1)	30		ns
t_{DH}	Data Hold Time		30		ns
t_{DS}	Data Setup Time		30		ns
t_{HZ}	$\overline{RD}$, RD to Floating Data Delay	@100 pF loading (Note 3)	0	100	ns
t_{MR}	Master Reset Pulse Width		5000		ns
t_{RA}	Address Hold Time from $\overline{RD}$, RD	(Note 1)	20		ns
t_{RC}	Read Cycle Delay		125		ns
t_{RCS}	Chip Select Hold Time from $\overline{RD}$, RD	(Note 1)	20		ns
t_{RD}	$\overline{RD}$, RD Strobe Width		125		ns
t_{RDD}	$\overline{RD}$, RD to Driver Enable/Disable	@100 pF loading (Note 3)		60	ns
t_{RVD}	Delay from $\overline{RD}$, RD to Data	@100 pF loading		60	ns
t_{WA}	Address Hold Time from $\overline{WR}$, WR	(Note 1)	20		ns
t_{WC}	Write Cycle Delay		150		ns
t_{WCS}	Chip Select Hold Time from $\overline{WR}$, WR	(Note 1)	20		ns
t_{WR}	$\overline{WR}$, WR Strobe Width		100		ns
t_{XH}	Duration of Clock High Pulse	External Clock (8, Max.)	55		ns
t_{XL}	Duration of Clock Low Pulse	External Clock (8, Max.)	55		ns
RC	Read Cycle = $t_{AR} + t_{RD} + t_{RC}$		280		ns
WC	Write Cycle = $t_{AW} + t_{WR} + t_{WC}$		280		ns





Minimum Mode System Timing Requirements

Parameter	Symbol	5 MHz Spec. V_{CC} = 4.5 V to 5.5 V Ta = -40 to +85°C	
		Min.	Max.
CLK Cycle Period	T_{CLCL}	200	DC
CLK Low Time	T_{CLCH}	118	—
CLK High Time	T_{CHCL}	69	—
CLK Rise Time (From 1.0 V to 3.5 V)	T_{CH1CH2}	—	10
CLK Fall Time (From 3.5 V to 1.0 V)	T_{CL2CL1}	—	10
Data in Setup Time	T_{DVCL}	30	—
Data in Hold Time	T_{CLDX}	10	—
RDY Setup Time into MSM 82C84A-2 (See Notes 1, 2)	T_{R1VCL}	35	—
RDY Hold Time into MSM 82C84A-2 (See Notes 1, 2)	T_{CLR1X}	0	—
READY Setup Time into MSM80C88A-10	T_{RYHCH}	118	—
READY Hold Time into MSM80C88A-10	T_{CHRYX}	30	—
READY inactive to CLK (See Note 3)	T_{RYLCL}	-8	—
HOLD Setup Time	T_{HVCH}	35	—
INTR, NMI, $\overline{TEST}$ Setup Time (See Note 2)	T_{INVCH}	30	—
Input Rise Time (Except CLK) (From 0.8 V to 2.0 V)	T_{ILIH}	—	15
Input Fall Time (Except CLK) (From 2.0 V to 0.8 V)	T_{IHIL}	—	15

Timing Responses

Parameter	Symbol	5 MHz Spec. V_{CC} = 4.5 V to 5.5 V Ta = -40 to +85°C	
		Min.	Max.
Address Valid Delay	t_{CLAV}	10	110
Address Hold Time	t_{CLAX}	10	—
Address Float Delay	t_{CLAZ}	t_{CLAX}	80
ALE Width	t_{LHLL}	t_{CLCH}-20	—
ALE Active Delay	t_{CLLH}	—	80
ALE Inactive Delay	t_{CHLL}	—	85
Address Hold Time to ALE Inactive	t_{LLAX}	t_{CLCH}-10	—
Data Valid Delay	t_{CLDV}	10	110
Data Hold Time	t_{CHDX}	10	—
Data Hold Time after $\overline{WR}$	t_{WHDX}	t_{CLCH}-30	—
Control Active Delay 1	t_{CVCTV}	10	110
Control Active Delay 2	t_{CHCTV}	10	110
Control Inactive Delay	t_{CVCTX}	10	110
Address Float to $\overline{RD}$ Active	t_{AZRL}	0	—
$\overline{RD}$ Active Delay	t_{CLRL}	10	165
$\overline{RD}$ Inactive Delay	t_{CLRH}	10	150
$\overline{RD}$ Inactive to Next Address Active	t_{RHAV}	t_{CLCH}-45	—
HLDA Valid Delay	t_{CLHAV}	10	160
$\overline{RD}$ Width	t_{RLRH}	$2t_{CLCL}$-75	—
$\overline{WR}$ Width	t_{WLWH}	$2t_{CLCL}$-60	—
Address Valid to ALE Low	t_{AVAL}	t_{CLCH}-60	—
Ouput Rise Time (From 0.8 V to 2.0 V)	t_{OLOH}	—	15
Output Fall Time (From 2.0 V to 0.8 V)	t_{OHOL}	—	15

Notes: 1. Signals at MSM82C84A-2 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next C
3. Applies only to T_2 state. (8 ns into T_3)