Assignment 2

Due September 26, 1996

In this assignment you'll design a 4-bit counter using VHDL, simulate your design to test its behaviour and synthesize it

You will also write a simple 8088 assembly language program that prints out a sequence of characters.

Question 1

On the course Web page you will find partial data sheets from several manufacturers for the 74'191 4-bit counter.

Write a VHDL description for this device using an entity name of LS161 and the same port signal names as used in the data sheets:

Note that the pe, and mr inputs are active low (assume active true logic – low is '0'). All other signals are active-high.

Follow the instructions on the course Web page and simulate the operation of the counter. Use the test bench in the file ~elec464/asg2tb.vhd.

Once you have determined that your design operates properly, synthesize it using the same method as in Assignment 1.

The following table shows the test vectors and might be useful in determining the cause of errors.

Hand in a listing of your VHDL description, the output of the simulation run and the schematic of the synthesized circuit.

Question 2

Using the example in the lecture notes as a model, write an 8088 assembly-language program that prints the upper-case version of a string stored in memory. Note that in ASCII lower-case letters range in value from 061H to 07AH inclusive. A lower-case letter can be converted to upper case by subtracting 020H.

The string stored in memory (using the db directive) should be the string 'AZaz' followed by your name and student number.

Use the INT 21H function to call the DOS character output routine as shown in the lecture notes.

Instructions on using a free 8088 assembler are available on the course Web page.

Assemble the program and make sure it works properly. When the program runs correctly, write its output to a file (asg2 >asg2.out).

Hand in a listing of your program and the output.

CEP	CET	CP	PE*	MR*	D	Q	TC	Comment
1	1	1	1	0	0000	0000	0	reset
1	1	1	1	1	0000	0001	0	count up
1	1	1	1	1	0000	0010	0	
0	1	1	1	1	0000	0010	0	disable count
1	0	1	1	1	0000	0010	0	
0	0	0	0	1	1110	0010	0	sync load
0	0	1	0	1	1110	1110	0	
1	1	1	1	1	0000	1111	1	reach terminal count

Note that your design must conform to the specification in the data sheets and not simply meet the given test vectors.