Assignment 9 - Solutions

Question 1

For a high-level output the noise immunities are computed as follows:

Input Type	Output Type	V_{OH}	V_{IH}	V_{OH} $-V_{IH}$
LS-TTL	LS-TTL	2.7	2.0	0.7
CMOS	CMOS	5.0	3.5	1.5
LS-TTL	CMOS	2.7	3.5	-0.8
CMOS	LS-TTL	5.0	2.0	3.0

For a low-level output the noise immunities are computed as follows:

Input Type	Output Type	V_{OL}	V_{IL}	V_{OL} $-V_{IL}$
LS-TTL	LS-TTL	0.8	0.5	0.3
CMOS	CMOS	1.5	0.01	1.4
LS-TTL	CMOS	0.8	0.01	0.8
CMOS	LS-TTL	1.5	0.5	1.0

The best noise immunity (3V) at a high level is by driving an LS-TTL input from a CMOS output. The best noise immunity (1.4V) at low level is from driving a CMOS input from a CMOS output. Driving an LS-TTL input from a CMOS output will not work reliably because the LS-TTL output outputs a minimum of 2.7 volts and the CMOS input requires a minimum of 3.5 volts.

Question 2

A DTB slave needs access to the following signals that make up the DTB: the address bus (A01 to A31, A17 to A31 optional), the data bus (D00 to D31, D16 to D31 optional), address strobe (AS*), transfer width information (LWORD* (optional), DS1*, DS0*), read/write (WRITE*), transfer acknowledge (DTACK*), and bus cycle type (AM0 to AM5, optional).

A DTB master needs access to the data transfer bus signals described above plus some signals from the DTB arbitration bus: at least one of the bus request (BR0*-BR3*) and corresponding bus grant daisy chaining (BG0IN*-BG3IN* and BG0OUT*-BG3OUT*) signals, plus the bus busy (BBSY*) and bus clear (BCLR*) signals.

An interrupter needs access to a few of the DTB signals listed above (A0 to A3, D0 to D7, AS*, DS0*, and DTACK*) to respond with the interrupt number as well as the interrupt request (IRQ1 to IRQ7), and interrupt acknowledge daisy chain (IACKIN* and IACKOUT*) signals.

All three types of modules may need access to some of the signals on the utility bus (clock, reset, etc).

Question 3

If the peripheral's wait-state generating logic was slow compared to the bus cycle period it might not be able to meet the setup time requirements of an 80x86-family READY input. In this case a wait state would not be inserted and the memory access would not work properly. On a 68000 system, the failure to meet the DTACK setup requirements would simply result in an additional wait state being generated so this approach is preferable.