Assignment 3
Solutions

Question 1

EPROM read cycles

The following 8051 requirements need to be met:

t_{AVIV}
address valid to instruction valid
302 ns required at 12 MHz
= t_{ACC}, 450 ns guaranteed
requirement not met by 148 ns

for variable clock frequency:
t_{AVIV} = 5 t_{CLCL} - 115 = 450 ns
2 t_{CLCL} = (450 + 115) / 5 = 113 ns
maximum clock frequency is 8.85 MHz

t_{PXIX}
PSEN* to instruction not valid
0 ns required at 12 MHz
= t_{OH}, 0 ns guaranteed
requirement met by 0 ns

t_{PXIZ}
instruction float from end of write
63 ns max required at 12 MHz
= t_{DF}, 130 ns guaranteed
requirement not met by 67 ns

for variable clock frequency:
t_{PXIZ} = t_{CLCL} - 20 = 130 ns
t_{CLCL} = 130 + 20 = 150 ns
maximum clock frequency is 6.66 MHz

t_{PLIV}
PSEN* to instruction valid
125 ns required at 12 MHz
= t_{OE}, 150 ns guaranteed
requirement not met by 25 ns

for variable clock frequency:
3 t_{CLCL} - 125 = 150
maximum clock period:
t_{CLCL} = (150 + 125) / 3 = 91 ns
maximum clock frequency is 10.9 MHz.

t_{LLIV}
ALE low to instruction valid
233 ns required at 12 MHz

This particular timing requirement would apply directly if the address latch were edge-triggered. In this case the 8 LS address bits would not appear on the latch outputs until the falling edge of ALE. We would then have to ensure that t_{ACC} was less than t_{LLIV} (it isn't).

However, the latch we use is transparent and as soon as ALE goes high the address is available to the EPROM. Since the latch goes high before the address becomes valid we need not worry about the timing of the rising edge of ALE.

Unfortunately, from the information given it does not seem possible to verify t_{LLIV} for this particular design.

We would need to know, for example, the maximum value for t_{LLPL} (see t_{LLRL} below).

RAM read cycles

The following 8051 requirements need to be met:

t_{RLDV}
read low to data valid
250 ns required at 12 MHz
= t_{OE}, 65 ns guaranteed
requirement met by 185 ns

t_{RHDX}
data hold time
0 ns required at 12 MHz
= t_{OH}, 0 ns guaranteed [1]
requirement met by 0 ns

t_{RHDZ}
OE* disable to data hi-impedance
97 ns required at 12 MHz
= t_{OHZ}, 65 ns guaranteed
requirement met by 32 ns

[1] There is a mistake in the diagram for t_{OH}. t_{OH} should actually extend from from OE* high to data out invalid, not to CE* high.

t_{LLDV}
ALE low to data valid in
517 ns required at 12 MHz

This requirement is similar to t_{LLIV} but now we are given additional guaranteed timing (maximum t_{LLWL}) that allows us to verify that the requirement will be met.

$= t_{LLWL} + t_{OE} = 300 + 65 = 365$ ns, guaranteed
requirement met by 152 ns

t_{AVDV}
address valid to data valid
585 ns required at 12 MHz
$= t_{ACC}$, 200 ns guaranteed
requirement met by 385 ns

RAM write cycles

The following 2128 RAM requirements need to be met:

t_{RC}
read cycle time
200 ns required
$= t_{CY}$, 1000 ns guaranteed at 12 MHz
requirement met by 800 ns

t_{WC}
same as t_{RC}.

t_{CW}
chip select to end of write
200 ns required
$= t_{AVWL} + t_{WLWH} = 203 + 400 = 603$ ns guaranteed at 12 MHz
requirement met by 403 ns

t_{AS}
address setup
0 ns required
$= t_{AVWL}$, 203 ns guaranteed at 12 MHz
requirement met by 203 ns

t_{WP}
write pulse width
100 ns required
$= t_{WLWH}$, 400 ns guaranteed at 12 MHz
requirement met by 300 ns

t_{AW}
address valid to end of write
200 ns required
$= t_{AVWL} + t_{WLWH} = 203 + 400 = 603$ ns guaranteed at 12 MHz
requirement met by 403 ns

t_{WR}
write recovery time
0 ns required
not specified, will be at least the larger of t_{WHQX} or t_{WHLH}
requirement met by at least 43 ns (t_{WHLH})

t_{DS}
data setup time
65 ns required
$= t_{QVWH}$, 433 ns guaranteed at 12 MHz
requirement met by 368 ns

t_{DH}
RAM data hold time
0 ns required
$= t_{WHQX}$, 33 ns guaranteed at 12 MHz
requirement met by 33 ns