ELEC 464 : MICROCOMPUTER SYSTEM DESIGN
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Intel 8088 CPU Interface

Unlike the Motorola 68000, the Intel 8088 multiplexes its address, data and CPU state signals and requires external hardware to support features such as prioritized interrupts. This lecture describes the Intel 8088 CPU chip and the associated logic required to support the CPU.

The 8088 CPU Signals

Utility Bus

Vcc (power), ground (GND), clock (CLK) and RESET (input only) signals work as on the 68000. Unlike the 6800 (where a reset is an exception) an 8088 a reset causes IP and all segment registers except CS to be set to 0, CS to be set to 0FFFFH.

Exercise: Where would execution begin after a reset? Should there be an instruction or vector at that location? What is an advantage of this approach compared to the 68000's reset exception vector?

As discussed previously, if the READY pin de-asserted the 8088 will insert wait states between bus states T3 and T4.

Most 8088 system make use of an 8284 clock generator chip. This chip includes a crystal-controlled oscillator that generates the CPU clock signal (with a 33% duty cycle) and also synchronizes the READY and RESET inputs to meet the CPU's timing requirements.

Address and Data Buses

The 8088 has an 8-bit data bus, and a 20-bit address bus. However, the least significant 8 address and data bus signals are multiplexed. On the 8086 the LS 16 bits of the address bus are also used as the data bus. These signals output the address during the first part of a bus cycle and read/write the data during the latter part.

The CPU's ALE (address latch enable) signal is used to latch the address into an external 8 (or 16) bit latch during the first part of the bus cycle.

The multiplexing of the address/data buses (and the off-loading of various functions to external chips) allowed the 8086 and 8088 to be packaged in a 40-pin chip (compared to the 68000's 64 pin package).

Minimum and Maximum Modes

The 8088 can be configured to operate in two different modes depending on the level of a MiN/MaX* input. The minimum mode is designed for simple systems that don't require CPU state information or sophisticated control over the address and data busses. In minimum mode chip control signals such as RD*, WR* and ALE are available directly. When the CPU is set up to work in maximum mode the CPU state is provided to an external 8288 bus controller chip which decodes these signals and generates the four I/O and memory read and write strobes required to control memory and I/O peripherals.

In maximum mode the CPU state is encoded as three signals (S0* to S2*) similar to the

68000's function code outputs.

Exercise: Which 68000 bus cycles does the 8088 not have? Which 8088 bus cycles does the 68000 not have? Why?

8259 Interrupt Controller

The 68000 has three interrupt request inputs allowing up to seven levels of interrupt to be handled by the CPU. The 8088 only has one input pin for maskable interrupts. Prioritized interrupts must be handled with external logic, usually an Intel 8259 interrupt controller chip. This chip has eight interrupt inputs and one interrupt output. It has configuration registers that can be programmed to enable/disable individual interrupts. It also provides a (programmable) interrupt number to the CPU during the interrupt acknowledge cycle. This eliminates the need to include an interrupt acknowledge circuit on each peripheral. An 8259 can also accept interrupt requests from other 8259s if more than 8 interrupt sources are required.