System Buses

This lecture deals with system buses. These are buses used to interface the CPU with memory and peripherals on PC cards. The VME and ISA buses are used as examples.
Most of this material is covered in Chapter 10 in the text.

Introduction

To increase their flexibility, most general-purpose microcomputers include a system bus that allows printed circuit boards (PCBs) containing memory or i/o devices to be connected to the CPU. This allows microcomputer systems to be customized for different applications. The use of a standard bus also allows manufacturers to produce peripherals that will work properly with other manufacturers' computer systems.

The system bus consists of a number of parallel conductors on a backplane or motherboard. There are a number of connectors ("slots") into which other PCBs containing memory and i/o devices can be plugged in.

In most cases the system bus is an extension of the processor bus. In fact, some simple system buses simply consists of a connector that allows access to all of the pins on the CPU chip. Like the processor bus, the the system bus can be subdivided into an address bus, data bus, control bus and power supply connectors.

Some systems place the CPU and some auxiliary circuits on a PCB (the "motherboard") along with system bus connectors. Other systems use a simple "backplane" type of bus and place the CPU on a separate PCB. The latter has the advantage that the CPU card can be replaced if required. Because the bandwidth required for the RAM interface is much higher than that for most other peripherals, most modern systems use the system bus only for i/o devices and use a proprietary interface for RAM or simply place all of the RAM memory on the same PCB as the CPU.

We will look at two system common buses. The VME bus was commonly used by some high-performance computer systems and a wide range of (relatively expensive) interface cards are available for it. We will study the VME bus because it is commonly used for high-performance 68000 systems and includes features common to other high-performance buses such as arbitration for multiple bus masters.

The ISA bus is used in IBM-PC compatibles and is of interest because it is the most widely-used system bus.

The characteristics of the bus can be described by their mechanical (size, types of connectors, etc), their electrical characteristics (voltage, clock rates, etc), and protocols (read/write cycles, master/slave operation, interrupt acknowledgement, etc).

Connectors

Low-cost consumer-grade buses use card-edge connectors. The plug-in card has contact pads along one edge of the PCB. The motherboard has connectors on the motherboard that contact these pads. This reduces the cost of the peripheral. A typical example of this type of system is the IBM PC (ISA) bus.

Other buses use connectors on both the motherboard and the card. This adds to the cost of the card (about $5-10) but makes for more reliable contacts. A typical example is the 3-row by 32-pin (96-pin) "DIN" connector used by the VME bus.

Electrical Characteristics

The electrical characteristics of bus signals are complicated because logic outputs driving bus signals ("bus drivers") must drive many loads and the conductor runs are relatively long.

In addition, some bus signals need to be driven by different cards and must therefore be switched between input and output. It is also necessary to ensure that only one device drives the bus at any time.

Logic Families

The most common logic families are TTL and CMOS. Within these familes there are a number of sub-families with different power requirements and switching speeds. These families differ in output voltage levels and input thresholds as well as current sink and drive ability. VLSI interface devices (e.g. serial interfaces) are often only available in one logic family so it important to understand when the different families can be mixed.

The input threshold is the voltage where an input is considered two switch between one and zero. This threshold is different for different logic families. TTL inputs are the emiters of NPN transistors. Their input threshold is about 2 V_{be} (1.4 volts). When held low they *source* current (about 1 mA). CMOS inputs are the gates of FETs an are high-impedance sinks. Their input thresholds are at about half the supply voltage (2.5 V).

TTL outputs are about 3 volts high and 300 mV low. CMOS outputs are about 0V low and 5V high. The main problem arises when trying to drive CMOS inputs with TTL outputs as the TTL high-level outputs are not sufficiently high to provide good noise immunity.

Exercise: What is the noise immunity when a TTL high output is connected to a CMOS input (using values given above)? For a TTL low output?

Devices are also limited in the amount of current their outputs can supply ("source") when in the high state or the amount of current they can draw ("sink") when in the low state. These will also vary depending on the logic subfamily.

Bus Drivers and Receivers

Peripheral PC cards often have multiple logic devices that must be driven from the same bus signals (e.g. the clock). If the bus loading exceeds the bus specifications then buffer chips ("bus receivers") must be used. Similarly, if the drive capacity of a chip's logic output is not enough to drive the maximum loading on a bus line, a "bus driver" must be used to buffer output signals.

Bidirectional Buses

Some bus signals can be driven by multiple cards. For example, the data bus will be driven by all peripheral devices as well as the CPU. In this case bi-directional buffers called "bus transceivers" are used. As always, care must be taken in the design to prevent multiple simultaneous outputs on the same bus line (bus conflicts).

Open-Collector (OC) Logic

OC outputs can only sink current, not source it. A pull-up resistor is used to pull that particular bus line to +5. Any device connected to that line can pull the signal low. The resistance of the pull-up resistor must be sufficiently low that the maximum voltage drop across it still provides a valid high logic level and the resistance must be high enough to limit the current through it to a value that will not damage the OC outputs.

The choice of pull-up resistance is also a compromise between rise time and power consumption.

Tri-State Logic

Tri-state logic outputs can controlled to be in a high output, a low output or in a high-impedance mode. They are used to drive bus signals that might be driven by more than one device.

For example, on a system that has multiple bus masters the address data bus must be driven by tri-state outputs and the data bus driven by tri-state bus transceivers.

Dynamic Contention

It should be remembered that tri-state and bidirectional buffers (receivers/drivers/transceivers) take a finite time to switch modes. A detailed timing analysis is necessary to ensure that two outputs will not be enabled simultaneously. This analysis will needs to take into account the CPU timing as well propagation delays for the circuits that control the buffer directions.

Impedance and Termination

To analyze the performance of the bus for the short rise times required in high-speed buses the bus must be treated as a transmission line.

The pulse generated by a bus driver will propagate down the bus. If the bus is not terminated (on both ends) by the characteristic impedance of the bus a portion of the signal will be reflected. The reflections will propagate back and forth along the bus and appear as ringing and noise. In addition, there will be reflections from each tap where a card is connected to the bus.

Typical propagation times for signals on a 10-mil (.01 inch) tracks are on the order of 6 ns/metre. If the rise time of a device is on the same order as the propagation delay there is a potential for reflections caused by improper termination to cause problems.

For the above reasons it is important that high-speed buses be terminated in the characteristic impedance of the bus. The typical characteristic impedance is on the order of 100 to 150 ohms. It is not possible to simply tie a resistor equal to the bus characteristic impedance to ground because this would pull the signal low. Instead, the resistor is connected to a low-impedance voltage source at about half of V_{cc}.

VME Bus

Background

The VME ("Versa Module Europe") system bus was developed by Motorola specifically for 68000-based systems. It has also been adapted to other processors. Unlike the ISA bus the VME bus standard is very precise specified. It includes many advanced features such as complex arbitration mechanisms for multiple bus masters and interrupt sources.

Mechanical

VME bus cards can be single or dual height cards. The dual-height (160x233mm) cards use two 96-connector "DIN" connectors (P1 and P2) to connect to the backplane. Single-height cards (160x100mm) use only one connector (P1). The P1 connector contains a 24-bit address bus, a 16-bit data bus and most of the control bus. The second connector contains additional address bus bits (extending it to 32 bits) and data bus bits (extending it to 32 bits).

The VME bus uses TTL voltage levels.

VME Functional Modules

The VME bus supports the standard read, write and interrupt acknowledge cycles as well as block read and write cycles that allow the CPU to read/write a continguous block of memory. The VME bus also allows a read-modify-write cycle that allows atomic (uninterruptible) memory updates.

The operation of the bus is defined in terms of the operation of functional blocks that may be present on cards. A particular card will contain only those functional blocks that are relevant to its operation. Among the possible functional modules are:

A *master* initiates transfers of data over the DTB (data transfer bus). A *slave* responds to data transfers initiated by a bus master. A *location monitor* decodes addresses to determine when a slave is being accessed. A *interrupter* generates interrupts and responds to interrupt acknowledge cycles. A *requester* is capable of requesting use of the bus. An *arbiter* determines which master will get control of the bus.

Exercise: Which functional modules do you think would be found on a disk controller card? On a memory card? On a CPU card?

VME Data Transfer Bus

The VME bus is very similar to the 68000 processor bus. It uses 31 address lines, and DS0*, DS1* and LWORD* strobes in the same fashion as the 68000 family. The address modifier lines AM0 to AM5 indicate the type of address space (supervisor, interrupt acknowledge, etc) in a similar way as the FC* lines are used on the 68000. There is a 32 bit data bus and unaligned read and write operations are allowed.

The VME DTB is asynchronous and a DTACK* signal is used (as in the 68000 processor bus) to indicate completion of a read/write cycle.

Bus Master and Interrupt Arbitration

The VME bus allows for sophisticated arbitration of multiple requests for bus ownership. A number of possible arbitration mechanism are defined in the bus specification with the implementation depending on the needs of the application. In addition, it is possible for different bus masters to respond to different interrupts by first obtaining bus ownership if required.

IBM PC Bus

Introduction

The bus used for expansion cards by the original IBM PC was designed to support expansion memory and peripherals such as video displays and parallel printer ports. It had the same 8-bit data bus and 20-bit address space as the Intel 8088 processor in the XT. The subsequent PC/AT (ISA) bus used a second card-edge connector to extended the address space to 24 bits and the data bus to 16 bits.

The PC cards are about 4 inches high and up to 13 inches long and use one (PC) or two (AT) card-edge connectors.

Unlike the 68000 family, Intel chips have a separate i/o address space. The bus thus includes both MEMR* and MEMW* and IOR* and IOW* control signals.

The PC bus is synchronous. The CPU performs fixed-length read and write cycles and does not require a signal such as DTACK to complete the cycle. However, a WAIT signal is available on the bus so that slow peripherals can request wait states.

The PC bus has 6 active-low interrupt request lines (IRQ2* to IRQ7*). The PC motherboard has a programmable interrupt controller chip (intel 8259) that arbitrates different levels of interrupt requests and generates an interrupt number in response to the processor's interrupt acknowledge cycle.

The bus also has 3 DMA request (DRQ*) and acknowledge (DACK) lines that can be used by peripherals with DMA capabilities.

The PC/AT (ISA) bus (but not the PC/XT bus) allows for a limited form of external bus mastering.