Timing Analysis

When designing a computer system we must ensure that the timing requirements of all the devices are met or the design may not operate reliably. This lecture covers this rather important topic.

Timing Specifications

Device timing specifications are given in tables in the data sheets published by the device manufacturer. The tables give brief descriptions of each specification, a symbol that identifies it on a timing diagram (e.g. t_{PD}) and minimum and/or maximum values for each specification.

Timing Specification Types

It's useful to understand the underlying reason for each timing specification. Most specifications can be classified as one of the following:

- a *propagation delay* is the time between a transition on an input and the correct value appearing on the output
- latches require a minimum *setup time* and *hold time* and sometimes minimum *pulse widths* for the latch to be set reliably
- when a signal pin can switch between input and output modes the *tri-state mode switch times* will be specified
- memory devices often have minimum *cycle times*
- less common timing specifications include delays between two outputs and more specialized timing specifications (e.g. A/D conversion time)

Exercise: Which of the above specifications would apply to a decoder?

Required versus Guaranteed Timing

Specifications can also be classified as requirements on the inputs or guarantees on the outputs. Timing requirements on the chip's inputs are typically minimums. Guaranteed output specifications are usually relative to some input and can be minimums and/or maximums.

A typical example of an input timing requirement is a setup time. An example of a guaranteed output specification is an output pulse width (the minimum time that the output is active).

Exercise: Is the propagation delay of a NAND gate a timing requirement or a guaranteed output specification?

Timing Diagrams

Timing diagrams clarify the meanings of timing specifications by labeling the times between signal transitions using symbols from the timing specifications tables.

Some conventions used in timing diagrams are:

- high and low levels shown at the same time indicate the signal is fixed but can have either value (e.g. a data signal)
- shading between two levels indicates that the value is allowed to change
- a single line between the two levels indicates that the line is in high-impedance ("tri-state") state
- sloped transitions between levels allow references to the signal reaching a low (V_{OL}/V_{IL}) or high (V_{OH}/V_{IH}) value
- arrows drawn between transitions on different signals show that one signal transition causes or affects another

It is important to understand that timing diagrams are *not* drawn to scale. This allows chips with different specifications to share the same timing diagram, allows small delays to be shown more clearly and also allows the same diagram to refer to both maximum and minimum values. Therefore you shouldn't rely on the timing diagram to show the order in which signal transitions happen.

SRAM Timing Specifications

Tables 4.5 and 4.8 give the read and write specifications for a 6116 SRAM. Figures 4.12 and 4.19 show the corresponding timing diagrams.

For example, for a write the 6116 has data setup (t_{DW}) and hold (t_{DH}) times of 40 and 10 ns, and a minimum write pulse width (t_{WP}) of 90 ns. On a read the access time (t_{AA}) is 200 ns and the output is tri-stated a maximum of 50ns after the chip is de-selected (t_{CHZ}).

Exercise: Try to identify the type of specification (propagation, setup, etc) and whether each of the specifications is a requirement on one of the inputs or a guaranteed timing on an output.

68000 Timing Specifications

Tables 4.4 and 4.7 give the read and write bus cycle timing specifications for a 68000. Figures 4.11 and 4.18 show the corresponding timing diagrams.

For example, during a read the address will be valid at least 30 ns before AS* goes low (t_{AVSL}), the strobe (DS*) width will be a minimum of 240 ns (t_{SL}) and the input data must be valid at least 15 ns before the end of state S6 (t_{DICL}). During a write the data will be valid for at least 30 ns after the strobe goes invalid (t_{SHDOI}), the data strobe will be a minimum of 115 ns ($t_{\mathrm{SL(w)}}$) and DTACK* must go low at least 20 ns before the end of S4 (t_{ASI}).

Exercise: Repeat the previous exercise with these 68000 timing specifications.

Timing Analysis

Timing analysis is an essential part of every microcomputer design. After a preliminary design the designer must evaluate the input timing requirements for each device and ensure that it's specifications are met. This requires knowing the timing delays for any interface circuits (buffers, latches, address decoders, etc) and the output timing specifications of the CPU.

The first step in the analysis is to draw timing diagrams that show the relevant signals and specifications. This may include signals generated by the microprocessor, by memories and by interface circuits such as address decoders and buffers. The diagrams are then used to derive expressions for the timing *requirements* of the devices in terms of the *guaranteed timing specifications* of the other devices. Finally each expressions is evaluated and the result compared to the requirements. If any requirements are not met then the design must be changed.

Typical changes include:

- adding wait states
- using redundant logic gates to add small delays
- latching signals to extend them

Example

Figure 4.14 shows a simple interface between a 68000 and a 6116 SRAM. A complete timing analysis would require evaluating all of the 68000 and 6116 timing requirements based on their specifications and the propagation delays of the interface gates and address decoder. This would take several hours of painstaking work. As an example we will only evaluate the 6116's data setup and data hold timing requirements.

The first step is to draw a timing diagram showing a 68000 write cycle, the signals generated by the interface circuit and the 6116 timing requirements. This is shown in Figure 4.20 in the text.

We then obtain expressions for the data setup (t_{DW}) and hold times (t_{DH}). Using the diagram and the descriptions of the 68000 specifications we can write the requirements for t_{DW} in terms of the guaranteed values t_{DOSL} and $t_{\mathrm{SL(w)}}$: $t_{\mathrm{DW}} = t_{\mathrm{DOSL}} + t_{\mathrm{SL(w)}}$. Similarly $t_{\mathrm{DH}} = t_{\mathrm{SHDOI}}$.

Finally, we substitute guaranteed values at 8 MHz and obtain $t_{\mathrm{DW}} = 145$ns and $t_{\mathrm{DH}} = 30$ns. Since the 6116 requires only 40 and 10 ns respectively our design meets these requirements.