Final Exam Review - Part 2
Solutions

Timing Analysis

All the requirements in this question are minimums.

8088 Read Cycle

Requirement		Guaranteed		Excess	Met
Symbol	Value	Expression	Value	value	(Y/N)
8088 CPU Requirements					
t_{AVDV}	460	t_{AD}	250	10	Y
t_{RLDV}	205	t_{RD}	300	-95	N
8279 Requirements					
t_{AR}	50	t_{CLCL} - $t_{CLAVmax}$ + $t_{CLRLmin}$ = 200 - 100 + 10	100	50	Y
t_{RA}	5	t_{CLCH} - $t_{CLRHmax}$ + $t_{CLLHmin}$ = 118 - 150 + 10	-22	-27	N
t_{RR}	420	t_{RLRH} = 2t_{CLCL} - 75 = 400 - 75	325	-75	N
t_{RCY}	1000	4 t_{CLCL}	800	-200	N

The 8279's t_{RA} requirement is probably to ensure that the data remains valid until t_{DF}. Since the 8088's hold time requirement will always be met (see explanation in the question), meeting this requirement is not critical.

The other requirements would be met by adding one wait state. This would increase t_{AVDV} and t_{RLDV} by 200 ns and increase the guaranteed values for t_{RR} and t_{RCY} by 200 ns.

8088 Write Cycle

Requirement		Guaranteed		Excess	Met
Symbol	Value	Expression	Value	value	(Y/N)
8279 Requirements					
t_{AW}	50	t_{CLCL} - $t_{CLAVmax}$ + $t_{CVCTVmin}$ = 200 - 110 + 10	100	50	Y
t_{WA}	20	$t_{WHDXmin}$ = t_{CLCH} - 30 = 118 - 30	88	68	Y
t_{WA}	20	t_{CLCH} - $t_{CVCTXmax}$ + $t_{CHDXmin}$ = 118 - 110 + 10	18	-2	N
t_{WW}	400	t_{WLWH} = 2t_{CLCL} - 60 = 400 - 60	340	-60	N
t_{DW}	300	2t_{CLCL} - $t_{CLDVmax}$ - $t_{CVCTXmin}$ = 400 - 110 - 10	280	-20	N
t_{WD}	40	t_{WHDX} = t_{CLCH} - 30 = 118 - 30	88	48	Y
t_{WCY}	1000	4t_{CLCL}	800	-200	N

In the expression for t_{WA} note that the timing specifications table states that t_{WHDX} is the *data* hold time, but the read cycle timing diagram shows that the data and address lines remain valid for the same length of time.

The second expression for t_{WA} is probably overly conservative. If, as in this case, you are able to obtain two expressions for the same guaranteed timing parameter you should use the one that will give you the most advantageous guaranteed value. In this case we would use $t_{WHDXmin}$. The rationale for this is explained in detail in section 4.3 (68020 read cycle) of the textbook on page 195.

The t_{WW}, t_{DW} and t_{WCY} timing requirements could all be met by adding one wait state.

Sample Short Answer Questions

1. *68000 Exception Handling:* No. The **Status Register** and **Interrupt Encoding** tables on page 878 show that the device requested an interrupt of level 5 by asserting IPL0* and IPL2* but since the I2/I1/I0 of the SR are set to 101 so only interrupts of level 6 and 7 will be recognized.

2. *Cache:* Using the formula for the no-cache/cache access time ratio, S, in the lecture on Cache Memory (or page 515 of the text) with $H = 0.85$ and $k = 20/80 = 0.25$, we obtain:

$$S = \frac{1}{1 - H(1-k)} = \frac{1}{1 - 0.85(1 - 0.25)} \approx 2.8$$

Sample "Best Match" Question

A	B
1	E
2	F
3	H
4	G
5	J
6	B
7	I
8	D
9	K
10	C
11	A