ELEC 464 : MICROCOMPUTER SYSTEM DESIGN
FALL 1995

Final Exam Review - Part 1
Solutions

State Machine Design

1. The state machine truth table is as follows:

ERROR	BUSY	STROBE*	ACK*	ERROR'	BUSY'
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	0	1
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	1	0	0
0	1	1	0	1	1
0	1	1	1	1	1
1	0	0	0	1	1
1	0	0	1	1	1
1	0	1	0	1	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

2. The CUPL Pin and logic equations required to implement the device using an 18CV8 PAL are:

```
Pin 1 = CLK ;
Pin 2 = ! STROBE ;
Pin 3 = ! ACK ;
Pin 12 = ERROR ;
Pin 13 = BUSY ;

ERROR =
   ! ERROR & ! BUSY & ! STROBE &   ACK #
   ! ERROR & ! BUSY &   STROBE &   ACK #
```

```
    ! ERROR &   BUSY &   STROBE & ! ACK #
    ! ERROR &   BUSY &   STROBE &   ACK #
      ERROR & ! BUSY & ! STROBE & ! ACK #
      ERROR & ! BUSY & ! STROBE &   ACK #
      ERROR & ! BUSY &   STROBE & ! ACK #
      ERROR & ! BUSY &   STROBE &   ACK #
      ERROR &   BUSY & ! STROBE & ! ACK #
      ERROR &   BUSY & ! STROBE &   ACK #
      ERROR &   BUSY &   STROBE & ! ACK #
      ERROR &   BUSY &   STROBE &   ACK ;

BUSY =
    ! ERROR & ! BUSY & ! STROBE &   ACK #
    ! ERROR & ! BUSY &   STROBE & ! ACK #
    ! ERROR & ! BUSY &   STROBE &   ACK #
    ! ERROR &   BUSY & ! STROBE & ! ACK #
    ! ERROR &   BUSY &   STROBE & ! ACK #
    ! ERROR &   BUSY &   STROBE &   ACK #
      ERROR & ! BUSY & ! STROBE & ! ACK #
      ERROR & ! BUSY & ! STROBE &   ACK #
      ERROR & ! BUSY &   STROBE & ! ACK #
      ERROR & ! BUSY &   STROBE &   ACK #
      ERROR &   BUSY & ! STROBE & ! ACK #
      ERROR &   BUSY & ! STROBE &   ACK #
      ERROR &   BUSY &   STROBE & ! ACK #
      ERROR &   BUSY &   STROBE &   ACK ;
```

The conversion from truth table to logic equations is mechanical – write one term per line. For each line in which the LHS variable is asserted substitute '!' for 0 and a space for '1' in front of the appropriate variable.

Note that for this device to operate properly the computer and printer would have to de-assert STROBE*/ACK* as soon as they detected that BUSY had been asserted/deasserted.

Memory System Design

- The number of chips required can be computed as the total memory required divided by the memory contributed per chip. The number of EPROM chips required is 32kB/8kB=4. The number of DRAM chips required is 8MB/0.5MB=16.
- Each "bank" must be 32 bits wide. For the EPROM array, this is 4 chips per bank (32 bits/8 bits/chip) and only one bank of chips is required. For the DRAM array this is 8 chips per bank (32/4) so we need 2 banks.
- The EPROM memory space is 32kB (15 bits) and starts at \$FFFF 8000[1] so the addresss decoder for the EPROM (for

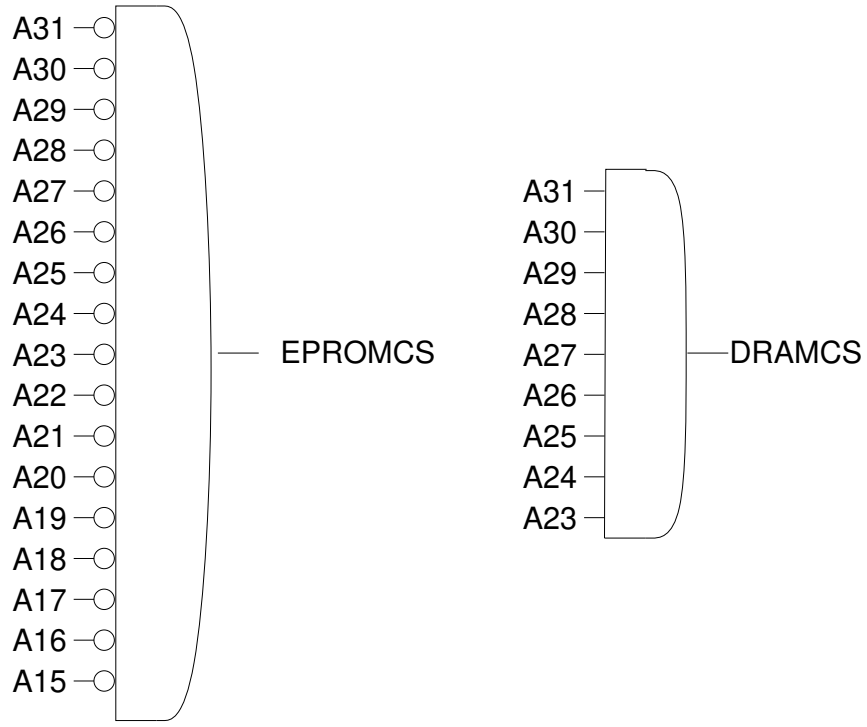
[1] The EPROM starting address given in the question was 64 bits wide - this was an error.

all four chips) would have to decode addresses of the form 1111 1111 1111 1111 1XXX XXXX XXXX XXXX.

The equation for the EPROM decoder is:

$$\text{EPROMCS} = A31 \cdot A30 \cdot A29 \cdot A28 \cdot A27 \cdot A26 \cdot A25 \cdot A24 \cdot A23 \cdot A22 \cdot A21 \cdot A20 \cdot A19 \cdot A18 \cdot A17 \cdot A16 \cdot A15$$

The DRAM memory space is 8MB (23 bits) and starts at $0 so the addresss decoder for the DRAM (for all chips) would have to decode addresses of the form 0000 0000 0XXX XXXX XXXX XXXX XXXX XXXX.

The equation for the DRAM decoder is:

$$\text{DRAMCS} = \overline{\text{A31}} \cdot \overline{\text{A30}} \cdot \overline{\text{A29}} \cdot \overline{\text{A28}} \cdot \overline{\text{A27}} \cdot \overline{\text{A26}} \cdot \overline{\text{A25}} \cdot \overline{\text{A24}} \cdot \overline{\text{A23}}$$