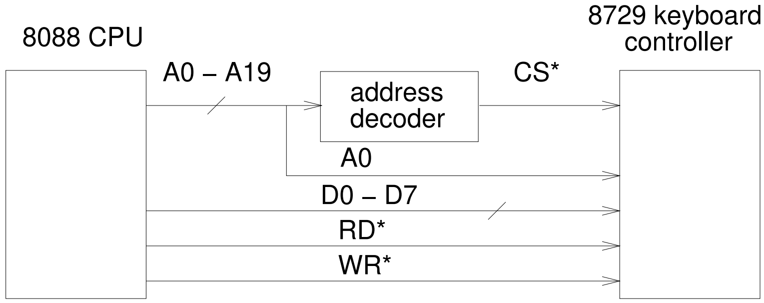
# Final Exam Review - Part 2

## Timing Analysis

The attached data sheets give the timing specifications for the Intel 8088 CPU in minimum mode and an Intel 8279 keyboard/display peripheral interface chip.

The diagram below shows how a 5 MHz ($t_{\text{CLCL}}$ = 200 ns) 8088 (not 8088-2) CPU in minimum mode is interfaced to an 8279 (not 8279-5) peripheral chip. You may assume the address decoder has zero propagation delay.




In the tables below you are to fill in the missing entries:

- an *expression* for the timing requirement in terms of the symbols for the guaranteed specifications of the other device
- the value of the expression (in ns)
- the different between the required value and the guaranteed value
- whether the requirement is met or not (Y[es] or N[o])

### *8088 Read Cycle*

The 8088 read cycle requirements $t_{\text{DVCL}}$ and $t_{\text{CLDX}}$ are specified from the clock going low in T4. Since the peripheral does not have a clock input, we must re-write these as requirements as *new* requirements: from address valid to data valid ($t_{\text{AVDV}}$) and from RD* active to data valid ($t_{\text{RLDV}}$). The expressions and values are:

$$t_{\text{AVDV}} < 3t_{\text{CLCL}} - t_{\text{CLAV}} - t_{\text{DVCL}} = 3 \times 200 - 110 - 30 = 460 \text{ ns} \quad (1)$$

and

$$t_{\text{RLDV}} < 2t_{\text{CLCL}} - t_{\text{CLRL}} - t_{\text{DVCL}} = 2 \times 200 - 165 - 30 = 205 \text{ ns} \quad (2)$$

We don't need to check the hold time requirement ($t_{\text{CLDX}}$, 10ns) – it will always be met since RD* does not go inactive for $t_{\text{CLRH}}$ = 10 ns by which point the hold time requirement has been met.

| Requirement | | Guaranteed | | Excess | Met |
|---|---|---|---|---|---|
| Symbol | Value | Expression | Value | value | (Y/N) |
| 8088 CPU Requirements | | | | | |
| $t_{\text{AVDV}}$ | 460 | | | | |
| $t_{\text{RLDV}}$ | 205 | | | | |
| 8279 Requirements | | | | | |
| $t_{\text{AR}}$ | 50 | | | | |
| $t_{\text{RA}}$ | 5 | | | | |
| $t_{\text{RR}}$ | 420 | | | | |
| $t_{\text{RCY}}$ | 1000 | | | | |

*8088 Write Cycle*

| Requirement | | Guaranteed | | Excess | Met |
|---|---|---|---|---|---|
| Symbol | Value | Expression | Value | value | (Y/N) |
| 8279 Requirements | | | | | |
| $t_{AW}$ | 50 | | | | |
| $t_{WA}$ | 20 | | | | |
| $t_{WW}$ | 400 | | | | |
| $t_{DW}$ | 300 | | | | |
| $t_{WD}$ | 40 | | | | |
| $t_{WCY}$ | 1000 | | | | |

### Sample Short Answer Questions

1. *68000 Exception Handling:* The contents of the SR are $0504 when a peripheral requests an interrupt by asserting IPL0* and IPL2*. Will the the CPU honour the interrupt request? Why or why not?

2. *Cache:* An average of 85 percent of the memory reads in a microcomputer system with cache result in a cache hit. If a main memory read cycle takes 80ns and a cache read cycle takes 20 ns, by what factor does the cache reduce the average memory read time?

### Sample "Best Match" Question

For each term in column "A" select the best matching entry in column "B". Write your answers in numerical order and show the number and the selected letter unambiguously. No penalty for wrong answers.

| A | | B | |
|---|---|---|---|
| 1 | Write-Back Cache | A | has a 32-bit data bus |
| 2 | Direct-Mapped Cache | B | is erased using ultra-violet light |
| 3 | DMA I/O | C | is a type of peripheral bus |
| 4 | interrupt-driven I/O | D | is asserted when a DTE is operational |
| 5 | Dynamic RAM | E | requires "dirty bit" memory |
| 6 | EPROM | F | requires tag RAM |
| 7 | EEPROM | G | would be appropriate for a keyboard interface |
| 8 | DTR | H | would be appropriate for a hard disk interface |
| 9 | RTS | I | retains its contents when power is removed |
| 10 | SCSI | J | typically uses multiplexed row and column addresses |
| 11 | VME | K | is asserted before data is output on RxD |