ELEC 464 : MICROCOMPUTER SYSTEM DESIGN
FALL 1995

Final Exam Review - Part 1

The exam may include any of the material covered in the lectures or assignments. It will include material that was covered in the mid-term.

Due to the need to mark the final exam promptly the exam will contain many short-answer, multiple-choice and best-match types of questions. These will be similar to the short exercises included in the lecture notes. In problem-type questions the format of the answer will be specified.

The following questions are meant as a review of the material in the course and to give an example of the (approximate) format of the questions.

State Machine Design

You will be given a description of a state machine and a partial truth table. You will be asked to complete the truth table and implement the state machine using a PAL.

When filling out the truth table you must:

- use truth values (1=true/asserted)
- don't use don't cares (Xs)
- provide the truth table entries in the order specified

In this example, you will design an handshaking circuit for a parallel port. This port is similar to a Centronics parallel port but in this case the handshaking in both directions is done using strobes. The STROBE* signal from the CPU is used to load a value into the output port and an ACK* strobe from the printer indicates that the value has been read and another character can be printed.

The circuit has a BUSY output that can be read by the CPU (through a separate input port) to test whether the printer is still busy or not.

The CPU should not load a value into the port if the printer is BUSY and the printer should not ACKnowledge a character if one is not available. If either of the latter two conditions occurs an ERROR output is asserted together with BUSY and the device stays in this state indefinitely regardless of what the strobes do.

You can assume a clock signal (CLK) with a period much shorter than the minimum strobe widths.

1. Fill in the missing entries in the following truth table:

ERROR	BUSY	STROBE*	ACK*	ERROR'	BUSY'
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

2. Write out the CUPL Pin and logic equations required to implement the device using an 18CV8 PAL.

Memory System Design

Design a memory decoder for a system with a 32-bit CPU (data lines D0 to D31 and address lines A2 to A31). This CPU accesses all memory as 32-bit values. The system's memory will be built using 8Kx8 EPROMs and 1Mx4 DRAMs. The total memory capacity will be 32 kBytes EPROM and 8 MBytes DRAM.

Answer the following questions:

- How many EPROM chips and how many RAM chips will be required?
- How many banks of EPROM and DRAM chips will be required?
- Assume the EPROM is to appear starting at $FFFF FFFF FFFF 8000 and the RAM at $0. Write out the logic equations for each bank's chip select in terms of the address signals A3 to A31).
- Draw a schematic that implements the above address decoder.