Assignment 9 - System Buses

Due November 23, 1995

Question 1

Using the specifications for the LS TTL and CMOS logic families given in Table 10.1 verify the noise immunities for the four possible combinations of LS TTL and CMOS logic given in Table 10.2. Which combination gives the best high-level noise immunity? The best low-level noise immunity? Which combination(s) won't work reliably?

Question 2

For each of the following VME functional modules, list the minimum subset of VME bus signals that the module would have to use.

- DTB master
- DTB slave
- Interrupter (note that an interrupter must also supply a vector number during an IACK cycle).

Question 3

Consider the difference between the 68000's DTACK* and the ISA bus READY (WAIT*) signal. The 68000 requires DTACK* to be asserted to complete the bus cycle. The 80x86 will complete the bus cycle *unless* WAIT* (actually an input called READY) is asserted (READY de-asserted) before the start of the second clock cycle (T2). If you had to design a peripheral with logic that was slow compared to the CPU clock which method would be preferable? Why?