ELEC 464 : MICROCOMPUTER SYSTEM DESIGN
FALL 1995

Assignment 7 - DMA and Cache Memory

Due November 9, 1995

Question 1

Draw a schematic (using logic gates) for an interrupt acknowledge arbitration circuit using daisy-chaining. The device should have an IACKIN* input and an IACKOUT* output for daisy chaining and an IRQ* open-collector output.

Question 2

Design the read-cycle portion of a cache controller for the simple direct-mapped cache described in the lecture on cache memory.

The inputs to your device are a clock (CLK), a read strobe (RD*) from the CPU, and the output of the address comparator (MISS*). The outputs of your controller are an output to enable the cache RAM data outputs during a cache hit (CACHE*), an output enable to enable the main memory on a cache miss (MAIN*), and a signal that tells the CPU that the value on the data bus is not yet valid (WAIT*). The memory enables should only be asserted while RD* is asserted.

RD* changes state at least 5 ns before the rising edge of CLK. RD* remains asserted until WAIT* is de-asserted. The CPU's address output is valid while RD* is asserted.

The clock frequency is 40 MHz. The cache and tag RAMs have access times of 20 ns. The main memory has an access time of 70 ns. Assume the address comparator has zero propagation delay.

(a) Draw timing diagrams showing the relationships between the inputs and outputs during a read cycle involving a cache hit and a miss.

(b) Design a state machine to implement the controller (read portion only).

(c) Write a CUPL description of the circuit (using an 18CV8-7, setup time = 5 ns) and test it with a simulation that includes a cache hit and a cache miss.