Assignment 5 - Memory Decoding

Due October 17, 1995

Exercises in address decoder design.

Question 1

Consider the address ranges for a 68000 system given in Question 1 of Chapter 5. Instead of contrasting implementations, find the following for each output (RAM1, I/O_1, etc) for both part (a) and (b):

- the size of each memory region
- the number of bits that need to be decoded to fully decode each region
- the logic equations for each output in terms of variables A23, A22, etc. Write the equations[1] using CUPL syntax (e.g. RAM1 = ! A23 & ! A22 & ...).

Question 2

Chapter 5, question 4. The meanings of the function code bits (FC0 – FC2) are given in Table 4.3. Give the boolean logic equation for the decoder output and draw a schematic of an implementation using gates.

Question 3

Chapter 5, question 9. Note that some recent microcontrollers do, in fact, feature on-chip programmable address decoders.

[1] Just the equations, not the other CUPL statements.