ELEC 464 : MICROCOMPUTER SYSTEM DESIGN
FALL 1995

Assignment 3 - Timing Analysis - Part 2

Due October 3, 1995

The purpose of this exercise is to do a complete timing analysis on a simple but realistic microcomputer system.

Question 1

The attached data sheets give the timing specifications and timing diagrams for an 8-bit 12 MHz 8051 microcontroller, a 2716-1 EPROM and a 2128-20 SRAM. These components are connected up to form a simple microcomputer system.

Like many other processors the 8051 multiplexes the least significant 8 bits of the address bus and the 8 bits of the data bus. When used with external memory "port 0" refers to the LS 8 bits of the data and address busses and "port 2" is the MS 8 bits of the address. An external latch (transparent when its control input is high and latched when it goes low) loads the LS 8 address bits during the first part of a read or write cycle and then holds the value during the rest of the cycle (when the data is actually read or written).

The remaining connections are straightforward. RD* drives the RAM's OE* and WR* drives the RAM's WE*. PSEN* drives the EPROM's OE*. Chip selects are driven by address lines (details of address decoding will be discussed later in the course). A15 drives the RAM's CE* and A14 drives the EPROM's CE*. The program that runs on this system is written so that A15 is low only for SRAM access and A14 is low only for EPROM access. Figure 1 shows how the system is set up.

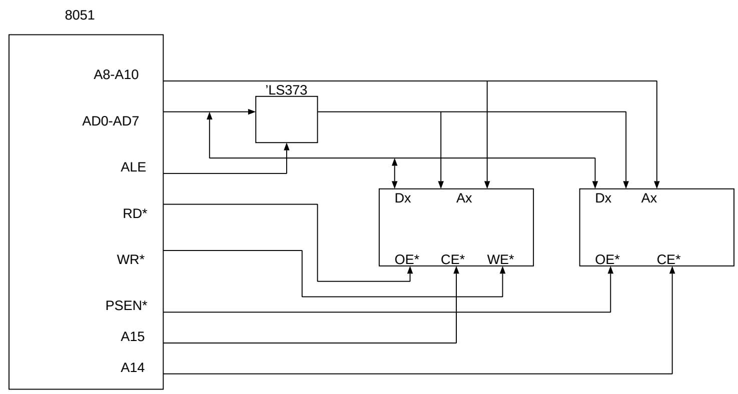

Figure 1: Diagram of 8051 system.

Verify whether this design will meet the timing requirements of the 8051 and the RAM. Obtain an expression for each timing requirement and compute the margin available for each requirement. If any requirements are not met, find the maximum 8051 clock frequency for which each parameter would be met. You should verify that at least the following requirements (plus any others you think need to be evaluated) are met: For the 8051 at 12 MHz: t_{AVIV}, t_{PXIX}, t_{PXIZ}, t_{PLIV}, t_{LLIV}, t_{RLDV}, t_{RHDX}, t_{RHDZ}, t_{LLDV}, and t_{AVDV}. For the 2128-20: t_{RC}, t_{WC}, t_{CW}, t_{AS}, t_{WP}, t_{AW}, t_{WR}, t_{DS}, and t_{DH}.

You can assume the 74LS373 latch timing requirements will be met and that it introduces negligible propagation delay.