Assignment 2 - Timing Analysis

Due September 26, 1995

Question 1

Chapter 4, question 10.

Draw the relevant signals on timing diagram(s) and show how the expressions were obtained. Note: "60000" is a typo, it should be 68000.

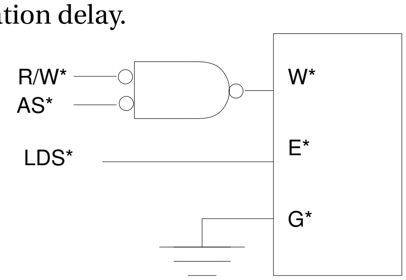
Question 2

Chapter 4, question 11. Note: this is for a *12.5* MHz CPU.

Question 3

A partial data sheet for the Motorola MCM60256A 32k $\times$ 8 static RAM chip is attached.

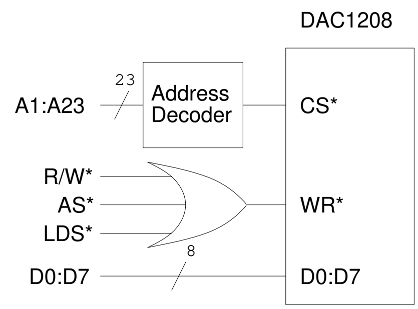
The following schematic shows a portion of the interface circuit used to generate the RAM's W*, E* and G* signals. Assume the gate introduces zero propagation delay.



For the timing specifications given for a write cycle for an 8 MHz MC68000 (page 182/183 in the text) and a MCM60256A-12 RAM (the *third* column in the RAM specifications table), obtain expressions for the following RAM timing requirements as a function of CPU timing specifications and determine whether each requirement is met or not: t_{ELEH}, t_{AVEL}, t_{AVEH}, t_{AVAV}, t_{DVEH}, t_{EHDX}.

Question 4

The schematic below shows a circuit used to interface an 8 MHz Motorola MC68000 microprocessor to a National DAC1208 digital-to-analog converter (DAC). The 68000 writes one byte at at time to the DAC. The DAC WR* (write strobe) signal is generated by a 3-input OR gate that asserts WR* when all of R/W* (write), AS* and LDS* signals from the CPU are true. The DAC CS* signal is generated by an address decoder whose inputs are A1 to A23 (address decoding details not relevant).



The timing diagram for writes to the DAC1208 is shown below along with the DAC1208 specifications for five required minimum times: the write pulse width (t_W), the data setup and hold times (t_{DS}, and t_{DH}), and the chip select setup and hold times (t_{CS}, and t_{CH}).

Parameter		DAC1208 requirement
t_W	Write Pulse Width	50
t_{DS}	Data Setup Time	70
t_{DH}	Data Hold Time	30
t_{CS}	Control Setup Time	60
t_{CH}	Control Hold Time	0

(a) Given the circuit above, give expressions for the five DAC1208 timing requirements in terms of 68000 timing specifications (Table 4.7). Assume the address decoder and the OR gate have zero propagation delay.

(b) Evaluate these expressions using the times guaranteed by a MC68000 CPU at 8 MHz and compare them to the typical values required by the DAC1208 as shown in the table above. State whether each particular requirement is met or not.