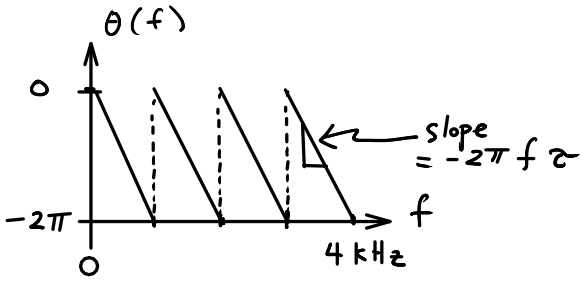
Solutions to Assignment 3

Question 1

(a) If a channel does not cause ISI to a signal transmitted at 8000 symbols/second it must have a non-zero amplitude response to at least 4 kHz and the channel must have a linear phase response. If the channel delays the signal by 1 ms then the slope of the phase response is given by $\theta(f) = -2\pi f\tau$ where $\tau = 10^{-3}$. At DC (zero frequency) the phase shift is zero and at 4 kHz the phase shift is $4 \times 2\pi$. Since phase wraps every 2π we could draw the phase response of the channel as:



We could also have drawn the phase between π and $-\pi$ or 0 to 2π (or not have shown the phase wrapping at all).

(b) If the channel causes no ISI at a symbol rate of 8 kHz then the impulse response must be zero every 125 μs. It must therefore also be zero at intervals of 250 μs and would not cause ISI to a signal with a symbol rate of 4 kHz or to any other symbol rate that is an integer fraction of 8 kHz.

For a signal with a symbol rate of 5 kHz to also have no ISI the impulse response must also be zero at multiples of 200 μs. This would only be possible if there were zero crossing every 25 μs (greatest common divisor of 125 and 200) which would imply a bandwidth of 40 kHz. However the channel has high attenuation above 6 kHz so ISI-free transmission at 5 kHz is not possible.

Question 2

From point A to point B on the mask the 10BASE-T signal increases from 0 to approximately 1 V in approximately 15 ns. From F to G it decreases 1 V in approximately 15 ns. The maximum slew rate is therefore approximately $\frac{+1}{15\times10^{-9}} \approx 67$ V/μs. This is (approximately) the slew rate required for a 10BASE-T line driver.

Question 3

The noise margin is the minimum noise voltage required to cause an error.

If a logic family guarantees a maximum low output voltage of 0.3 V input voltages below 0.8 V are guaranteed to be recognized as low then a noise of +0.5 V could cause an error.

If the a minimum high output voltage is 2.7 V and input voltages above 1.6 V are guaranteed to be recognized as high then noise of -1.1 V could cause an error.

The noise margin for this logic family is the minimum of (the absolute value of) these two values, or 0.5 V.

Question 4

From the datasheet for the Pulse J0011D01BNL Ethernet jack with magnetics:

(a) The maximum insertion loss from 1-65 MHz is 1dB.

(b) The transformer only has two transformers for two pairs. Thus it cannot be used it for 1000Base-T Ethernet which requires four pairs (although the frequency ranges are the same).

(c) The maximum voltage (Hi Potential) rating is 2250 VDC.

(d) The table on page 1 of the datasheet show the L/R (left/right) LED colors are G/Y (green/yellow) so the green LED is on the left. Page 6 of the datasheet says pin numbers 9 and 10 are for the left LED. Thus the green LED is connected to pins 9 and 10.

Question 5

ADSL systems use OFDM to transmit data to telephone company subscribers over twisted-pair cables.

(a) The symbol period is the inverse of the subcarrier spacing or $\frac{1}{4.3125}\mu$s. At sampling rate of 2.208 MHz each symbol would thus have $\frac{2208}{4.3125} = 512$ samples.

(b) A bridge tap with a length of 1450 m and a propagation velocity of 200 m/μs would cause an echo with a delay of $\frac{2\times1450}{200} = 14.5\mu$s. For the cyclic prefix between symbols to prevent ISI its length must be $\geq 14.5 \times 2.208 \approx 32$ samples.

Question 6

(a) The MLT-3 line code is polarity insensitive because 1's are encoded as voltage changes regardless of the signal polarity.

(b) The long-term average (DC) value should be zero because the signal should be at +1 V as often as it will be at -1 V.

(c) You could mark the end of an MLT-3-encoded signal by reversing the direction of voltage changes after a single voltage change instead of after two. This would cause, for example +1, 0..., +1 (or -1, 0..., -1) to be transmitted which is not normally possible.

Question 7

(a) A bit sequence consisting of continous ones results in the most overhead added by HDLC framing. Every fifth bit requires zero stuffing to be done.

(b) To transmit a frame of 240 bits would require bit stuffing to be done $\frac{240}{5} = 48$ times. This would require transmitting 288 bits plus 8 bits for the inter-frame flag for 240 data bits. The throughput is thus $\frac{240}{296} \approx 81\%$.

Question 8

SLIP requires a 0xc0 (END) byte at the end of a frame but if this value appears in the frame then the pair 0xdb 0xdc are sent. If the value 0xdb (ESC) appears in the frame the the value 0xdb 0xdd is sent.

The bytes in the frame are converted as follows:

```
0x00 -> 0x00
0xdb -> 0xdb 0xdd
0xaa -> 0xaa
0xc0 -> 0xdb 0xdc
0x1b -> 0x1b
        0xc0
```

So the sequence transmitted is: 0x00, 0xdb, 0xdd, 0xaa, 0xdb, 0xdc, 0x1b, 0xc0.

Question 9

You want to transmit the bits 10011 using the generator polynomial 1011 to compute the CRC.

(a) The CRC is computed as the remainder after appending 3 zeros:

```
     _________
1011 |10011000
      1011
      ----
       0101
       ----
        1010
        1011
        ----
         0010
         ----
          0100
 ----
  100
```

The CRC is thus 100 and the message plus CRC is 10011100.

(b) Adding two zero bits at the start of the message results in a zero remainder:

```
     _________
1011 |0010011100
      ----
       0100
       ----
        1001
        1011
        ----
         0101
         ----
          1011
          1011
          ----
           0000
           ----
            0000
            ----
             000
```

so the receiver is not able to detect zero bits added (or removed) at the start of the message.

(c) To be able to detect prepended zero bits we can invert the leading data bits at the transmitter and again at the receiver before computing the CRC.

We would thus transmit 01101100 as the message plus CRC. The receiver would invert the first four bits to 10011100 and would obtain the same remainder (zero) as before.

However, if we prepended two zero bits resulting in 00 1001 1100, the receiver would invert the first four received bits and compute the remainder of 11 01011 100:

```
     _________
1011 |1101011100
      1011
      ----
       1100
       1011
       ----
        1111
        1011
        ----
         1001
         1011
         ----
          0101
          ----
           1010
           1011
           ----
            0010
            ----
             010
```

So now the remainder is 001 and the error (prependended zeros) would be detected.

(d) Appending two zeros to the CRC does not change the CRC because the remainder remains zero. The detect this we can transmit the inverse of the CRC. The remainder will not be zero, but if there are no errors it will be a fixed value that depends only on the generator polynomial.