APSC 380 : INTRODUCTION TO MICROCOMPUTERS
1998/99 WINTER SESSION TERM 2

Lab 5 - PAL-based Game

Introduction

You will design, assemble and test an electronic game based on a programmable logic device (PLD). The device must operate according to the specifications given below. You will be supplied with a GAL16V8 PAL that you will use to build the system on a prototyping board in the lab. You will use the CUPL logic design language to generate the fuse map for the PAL and program the device using the same device programmer you used in Lab 4. You will demonstrate your device to the TA and hand in a listing of the CUPL code.

Specifications

The purpose of the game is to guess a hidden number in as few guesses as possible. For each guess the game will show you the number of differences between the bits in the hidden number and the number you enter.

Inputs and Outputs

The game has three slide switches to allow you to enter a guess (in binary), one pushbutton switch to compute a new hidden number and one pushbutton to display the number of differences between the hidden number and the guess.

The game has two LED outputs which are used to display the number of bit positions in error between the two numbers.

Behaviour

Each time the first pushbutton (“randomize”) is pressed the game computes a new 3-bit number. The numbers are generated by a pseudo-random number generator implemented as a 3-bit shift register. Each time the button is pushed the shift register is shifted right and a new bit is shifted in on left which is the exclusive-or of the previous left-most and right-most bits in the register. As long as the register is initialized with a non-zero value, this procedure will generate a periodic pseudo-random (“hard for most people to predict”) sequence of period 7.

Each time the second pushbutton (“show differences”) is pushed the game will compute the number of bits that are different between the hidden number and the guess and display that number (in binary) on two outputs (to drive LEDs).

The GAL16V8

You will be supplied with a GAL16V8 PAL which must be returned to the TA in the lab at the end of the lab period (there aren’t enough devices for the whole class). This device’s configuration is stored in EE (electrically erasable) programmable memory.

This PAL is an example of simple PLD. It has 8 outputs capable of computing 8 sum-of-product functions from 8 inputs, the 8 outputs and either complements (a maximum of 32 variables in each product term). The equation for each output is limited to a maximum of eight product terms (i.e. only 8 of the 2^{16} possible inputs can result in a ’1’ output). Each of the 8 outputs can be configured as a flip-flop if desired (clocked from an external clock input). This PAL’s outputs are set to 1’s when the device is first powered up. You may want to use some unused outputs as “temporary variables” to get around the limit on the number of product terms per output.

Circuit Description

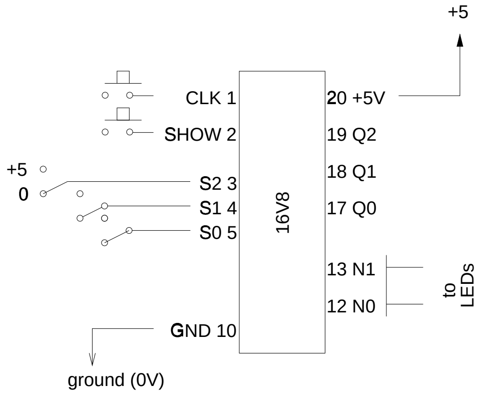
You should connect the switch and LEDs to the pins indicated below.

You will wire up your interface circuit on the same “DigiDesigner” prototyping unit used for the previous lab.

Please observe the warnings given in the previous lab concerning the susceptibility of the devices to incorrect voltages and static.

Assembling the Circuit

A schematic of the circuit is given below:



- Plug the chip into the breadboard.
- Connect pin 10 to the ground (0V) power supply output.
- Connect pin 20 to the +5 volt power supply output.
- Connect the first (“randomize”) pushbutton to pin 1 (the clock input).
- Connect the second (“count differences”) pushbutton to pin 2.
- Connect the slide switch outputs to pins 3 through 5.
- Connect the LEDs to pins 12 through 13.
- Make sure the chip is properly connected to both +5 V and ground rails. Reverse biasing the chip or it’s inputs will destroy the chip. Double check your connections before applying power.

Compiling your Design

You will use a free version of a CUPL “compiler” that runs under Windows 3.1 on the PCs in the lab. If want to run CUPL on another PC you can download the file from the Logical Devices Web page (`http://logicaldevices.com/cupl/startkit.html`) and install it. A tutorial manual is available at (`http://logicaldevices.com/cupl/starter.htm`) although the lecture notes and on-line help will probably be enough.

Enter the Design

Run WinCUPL and use *File—New* to create a template file. Fill in the comments section at the beginning with appropriate values. Fill in the pin definition section with mnemonic pin names for the signals listed above. Enter the appropriate logic equations into the section for logic equations. Save your design file using *File—Save.*

“Compile”

Check the Options dialog box to make sure a JEDEC file and a listing file will be generated. Use the *Run—Device Specific Compile* to generate the file into a fuse map in “JEDEC” format that can be used by the device programmer. Copy the resulting file (e.g. `lab4.jed`) to a floppy and use it to program the chip as described below.

Programming the PLD

You will use the same device programmer as in the previous lab. Please use this computer only for programming the devices. Type `ACCESS` to run the device programmer software. The device programmer software is menu-driven. Select the following options:

Device	PAL
MFR	Lattice
Type	GAL16V8A

This will start a second program that is specific to PAL devices. First select the option to “Load File”. Enter the name of your file (e.g. `lab4.jed`). Then select the option to automatically erase, blank check, program and verify.

It will take a few seconds for the device to be programmed. You may remove the device when the LED on the programmer goes on.

Submitting The Lab

Once your device is working properly print a program listing (e.g. `lab4.lst`) and demonstrate its operation to the TA. Return the chip to the TA at the end of the lab. You must return the part to get a mark for the assignment.